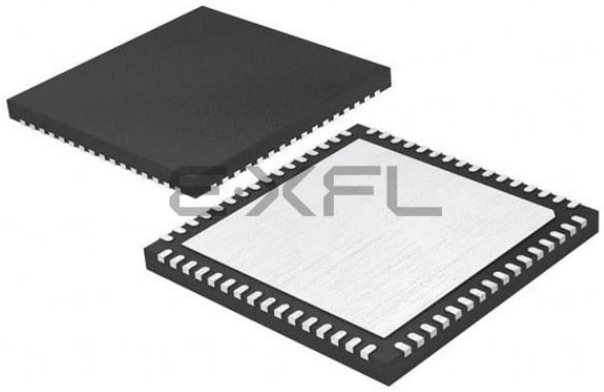

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Details	
Product Status	Obsolete
Core Processor	PIC
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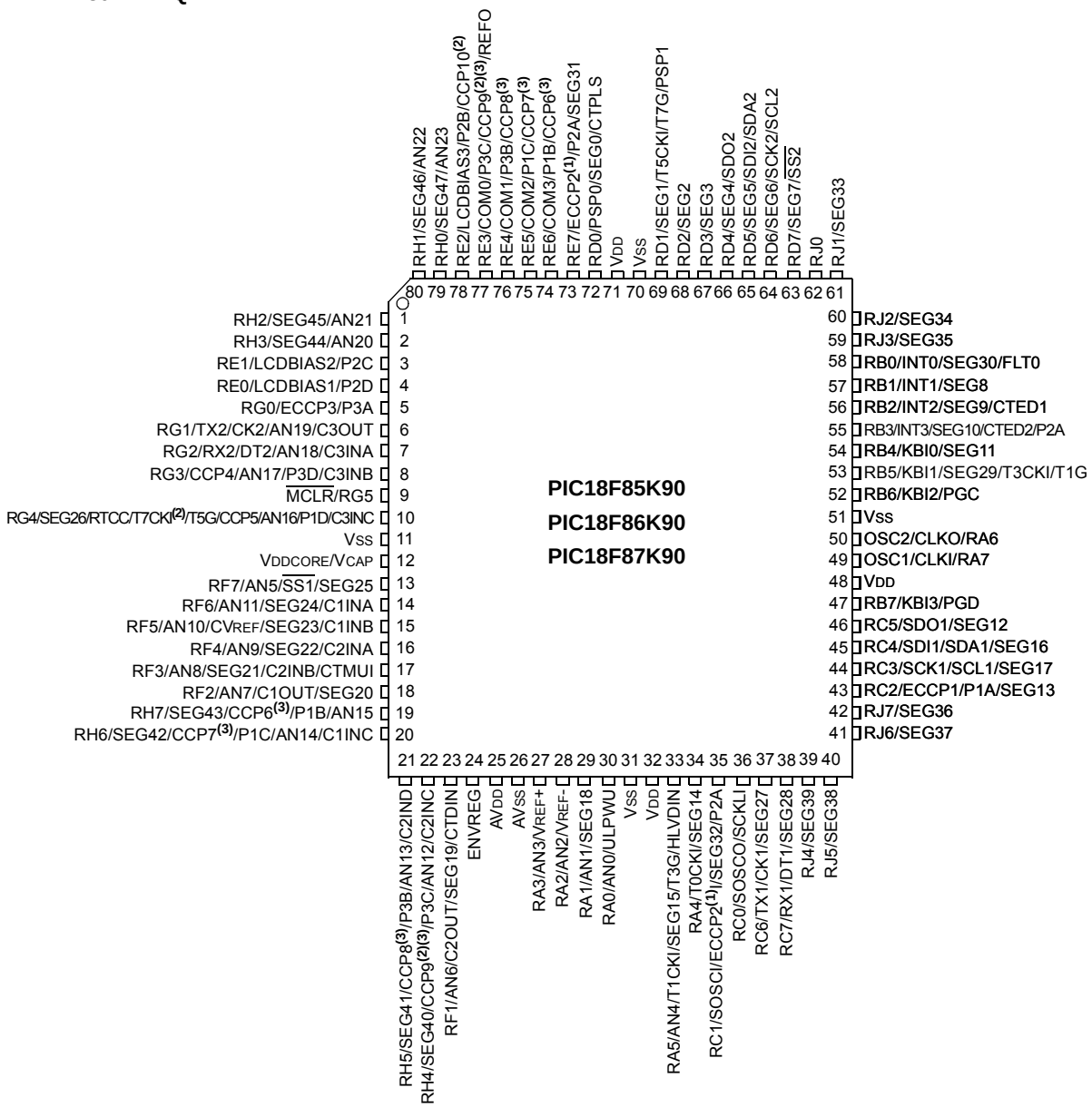
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f66k90t-i-mrrsl

Pin Diagrams – PIC18F8XK90

80-Pin TQFP



Note 1: The ECCP2 pin placement depends on the CCP2MX Configuration bit setting.

2: Not available on the PIC18F65K90 and PIC18F85K90.

3: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting

TABLE 1-3: PIC18F6XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	QFN/TQFP			
				PORTF is a bidirectional I/O port.
RF1/AN6/C2OUT/SEG19/CTDIN	17			
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog Input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
CTDIN		I	ST	CTMU pulse delay input.
RF2/AN7/C1OUT/SEG20	16			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog Input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21/C2INB/CTMUI	15			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog Input 8.
SEG21		O	Analog	SEG21 output for LCD.
C2INB		I	Analog	Comparator 2 Input B.
CTMUI		O	—	CTMU pulse generator charger for the C2INB comparator input.
RF4/AN9/SEG22/C2INA	14			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog Input 9.
SEG22		O	Analog	SEG22 output for LCD
C2INA		I	Analog	Comparator 2 Input A.
RF5/AN10/CVREF/SEG23/C1INB	13			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog Input 10.
CVREF		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
C1INB		I	Analog	Comparator 1 Input B.
RF6/AN11/SEG24/C1INA	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog Input 11.
SEG24		O	Analog	SEG24 output for LCD
C1INA		I	Analog	Comparator 1 Input A.
RF7/AN5/$\overline{SS1}$/SEG25	11			
RF7		I/O	ST	Digital I/O.
AN5		O	AnalogT	Analog Input 5.
$\overline{SS1}$		I	TL	SPI1 slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTE is a bidirectional I/O port.
RE0/LCDBIAS1/P2D	4			
RE0		I/O	ST	Digital I/O.
LCDBIAS1		I	Analog	BIAS1 input for LCD.
P2D		O	—	ECCP2 PWM Output D.
RE1/LCDBIAS2/P2C	3			
RE1		I/O	ST	Digital I/O.
LCDBIAS2		I	Analog	BIAS2 input for LCD.
P2C		O	—	ECCP2 PWM Output C.
RE2/LCDBIAS3/P2B/CCP10	78			
RE2		I/O	ST	Digital I/O.
LCDBIAS3		I	Analog	BIAS3 input for LCD.
P2B		O	ST	ECCP2 PWM Output B.
CCP10(3)		I/O	ST	Capture 10 input/Compare 10 output/PWM10 output.
RE3/COM0/P3C/CCP9/REFO	77			
RE3		I/O	ST	Digital I/O.
COM0		O	Analog	COM0 output for LCD.
P3C		O	—	ECCP3 PWM Output C.
CCP9(3,4)		I/O	S/T	Capture 9 input/Compare 9 output/PWM9 output.
REFO		O	—	Reference clock out.
RE4/COM1/P3B/CCP8	76			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
P3B		O	—	ECCP4 PWM Output B.
CCP8(4)		I/O	ST	Capture 8 input/Compare 8 output/PWM8 output.
RE5/COM2/P1C/CCP7	75			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
P1C		O	—	ECCP1 PWM Output C.
CCP7(4)		I/O	ST	Capture 7 input/Compare 7 output/PWM7 output.
RE6/COM3/P1B/CCP6	74			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
P1B		O	—	ECCP1 PWM Output B.
CCP6(4)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
RE7/ECCP2/P2A/SEG31	73			
RE7		I/O	ST	Digital I/O.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A		O	—	ECCP2 PWM Output A.
SEG31		O	Analog	SEG31 output for LCD.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

4.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode provides controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. To maintain software compatibility with future devices, it is recommended that SCS0 also be cleared, though its value is ignored. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the SLEEP instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value, or the INTSRC/MFIOSEL bit is set, the INTOSC output is enabled. The HFIOFS/MFIOFS bits become set, after the INTOSC output becomes stable after an interval of TIOBST (Parameter 38, Table 31-10). (For information on the HFIOFS/MFIOFS bits, see Table 4-3.)

Clocks to the peripherals continue while the INTOSC source stabilizes. The HFIOFS/MFIOFS bits will remain set if the IRCF bits were previously at a non-zero value or if INTSRC was set before the SLEEP instruction was executed and the INTOSC source was already stable. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the HFIOFS/MFIOFS bits will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TCSD (Parameter 38, Table 31-10), following the wake event, the CPU begins executing code clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

4.5 Selective Peripheral Module Control

Idle mode allows users to substantially reduce power consumption by stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what this mode does not provide: the allocation of power resources to the CPU, processing with minimal power consumption from the peripherals.

PIC18F87K90 family devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- Peripheral Enable bit, generically named XXXEN – Located in the respective module's main control register
- Peripheral Module Disable (PMD) bit, generically named XXXMD – Located in one of the PMDx Control registers (PMD0, PMD1, PMD2 or PMD3)

Disabling a module by clearing its XXXEN bit disables the module's functionality, but leaves its registers available to be read and written to. This reduces power consumption, but not by as much as the second approach.

Most peripheral modules have an enable bit.

In contrast, setting the PMD bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral are also disabled, so writes to those registers have no effect and read values are invalid. Many peripheral modules have a corresponding PMD bit.

There are four PMD registers in the PIC18F87K90 family devices: PMD0, PMD1, PMD2 and PMD3. These registers have bits associated with each module for disabling or enabling a particular peripheral.

TABLE 6-2: PIC18F87K90 FAMILY REGISTER FILE SUMMARY (CONTINUED)

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F24h	ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8	1111 1111
F25h	ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0	1111 1111
F26h	—	—	—	—	—	—	—	—	—	—
F27h	ODCON3	U2OD	U1OD	—	—	—	—	—	CTMUDS	00-- ---0
F28h	ODCON2	CCP10OD(3)	CCP9OD(3)	CCP8OD	CCP7OD	CCP6OD	CCP5OD	CCP4OD	CCP3OD	0000 0000
F29H	ODCON1	SSP1OD	CCP2OD	CCP1OD	—	—	—	—	SSP2OD	000- ---0
F2Ah	REFOCON	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	0-00 0000
F2Bh	CCPTMRS2	—	—	—	C10TSEL0	—	C9TSEL0	C8TSEL1	C8TSEL0	---0 -000
F2Ch	CCPTMRS1	C7TSEL1	C7TSEL0	—	C6TSEL0	—	C5TSEL0	C4TSEL1	C4TSEL0	00-0 -000
F2Dh	CCPTMRS0	C3TSEL1	C3TSEL0	C2TSEL2	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0	0000 0000
F2Eh	CM3CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	0001 1111
F2Fh	CM2CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	0001 1111
F30h	T12CON	—	T12OUTPS3	T12OUTPS2	T12OUTPS1	T12OUTPS0	TMR12ON	T12CKPS1	T12CKPS0	-000 0000
F31h	PR12	Timer12 Period Register								1111 1111
F32h	TMR12	TMR12 Register								0000 0000
F33h	T10CON(3)	—	T10OUTPS3	T10OUTPS2	T10OUTPS1	T10OUTPS0	TMR10ON	T10CKPS1	T10CKPS0	-000 0000
F34h	PR10	Timer10 Period Register								1111 1111
F35h	TMR10	TMR10 Register								0000 0000
F36h	T8CON	—	T8OUTPS3	T8OUTPS2	T8OUTPS1	T8OUTPS0	TMR8ON	T8CKPS1	T8CKPS0	-000 0000
F37h	PR8	Timer8 Period Register								1111 1111
F38h	TMR8	Timer8 Register								0000 0000
F39H	T6CON	—	T6OUTPS3	T6OUTPS2	T6OUTPS1	T6OUTPS0	TMR6ON	T6CKPS1	T6CKPS0	-000 0000
F3Ah	PR6	Timer6 Period Register								1111 1111
F3Bh	TMR6	Timer6 Register								0000 0000
F3Ch	T7GCON(3)	TMR7GE	T7GPOL	T7GTM	T7GSPM	T7GGO/$\overline{\text{T7DONE}}$	T7GVAL	T7GSS1	T7GSS0	0000 0x00
F3Dh	T7CON(3)	TMR7CS1	TMR7CS0	T7CKPS1	T7CKPS0	—	$\overline{\text{T7SYNC}}$	RD16	TMR7ON	0000 0x00
F3Eh	TMR7L(3)	Timer7 Register Low Byte								xxxx xxxx
F3Fh	TMR7H(3)	Timer7 Register High Byte								xxxx xxxx
F40h	CCP10CON(3)	—	—	DC10B1	DC10B0	CCP10M3	CCP10M2	CCP10M1	CCP10M0	--00 0000
F41h	CCPR10L(3)	Capture/Compare/PWM Register 10 Low Byte								xxxx xxxx
F42h	CCPR10H(3)	Capture/Compare/PWM Register 10 High Byte								xxxx xxxx
F43h	CCP9CON(3)	—	—	DC9B1	DC9B0	CCP9M3	CCP9M2	CCP9M1	CCP9M0	--00 0000
F44h	CCPR9L(3)	Capture/Compare/PWM Register 9 Low Byte								xxxx xxxx
F45h	CCPR9H(3)	Capture/Compare/PWM Register 9 High Byte								xxxx xxxx
F46h	CCP8CON	—	—	DC8B1	DC8B0	CCP8M3	CCP8M2	CCP8M1	CCP8M0	--00 0000
F47h	CCPR8L	Capture/Compare/PWM Register 8 Low Byte								xxxx xxxx
F48h	CCPR8H	Capture/Compare/PWM Register 8 High Byte								xxxx xxxx
F49h	CCP3CON	P3M1	P3M0	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	0000 0000
F4Ah	CCPR3L	Capture/Compare/PWM Register 3 Low Byte								xxxx xxxx
F4Bh	CCPR3H	Capture/Compare/PWM Register 3 High Byte								xxxx xxxx
F4Ch	ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	0000 0000
F4Dh	ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	0000 0000
F4Eh	CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	0000 0000
F4Fh	CCPR2L	Capture/Compare/PWM Register 2 Low Byte								xxxx xxxx

Note 1: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.
2: Unimplemented in 64-pin devices (PIC18F6XK90).
3: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

6.3.5 STATUS REGISTER

The STATUS register, shown in Register 6-2, contains the arithmetic status of the ALU. The STATUS register can be the operand for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the write to these five bits is disabled.

These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended. For example, `CLRF STATUS` will set the Z bit but leave the other bits unchanged. The STATUS register then reads back as '`000u u1uu`'.

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF`, `MOVFF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions not affecting any Status bits, see the instruction set summaries in Table 29-2 and Table 29-3.

Note: The C and DC bits operate in subtraction, as borrow and digit borrow bits, respectively.

REGISTER 6-2: STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	N	OV	Z	DC(1)	C(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **N:** Negative bit

This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative (ALU MSB = 1).
1 = Result was negative
0 = Result was positive

bit 3 **OV:** Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude which causes the sign bit (bit 7) to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 2 **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit(1)

For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(2)

For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand.

2: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand.

15.0 TIMER3/5/7 MODULES

The Timer3/5/7 timer/counter modules incorporate these features:

- Software-selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMRxH and TMRxL)
- Selectable clock source (internal or external) with device clock or SOSC oscillator internal options
- Interrupt-on-overflow
- Module Reset on ECCP Special Event Trigger

Timer7 is unimplemented for devices with a program memory of 32 Kbytes (PIC18FX5K90).

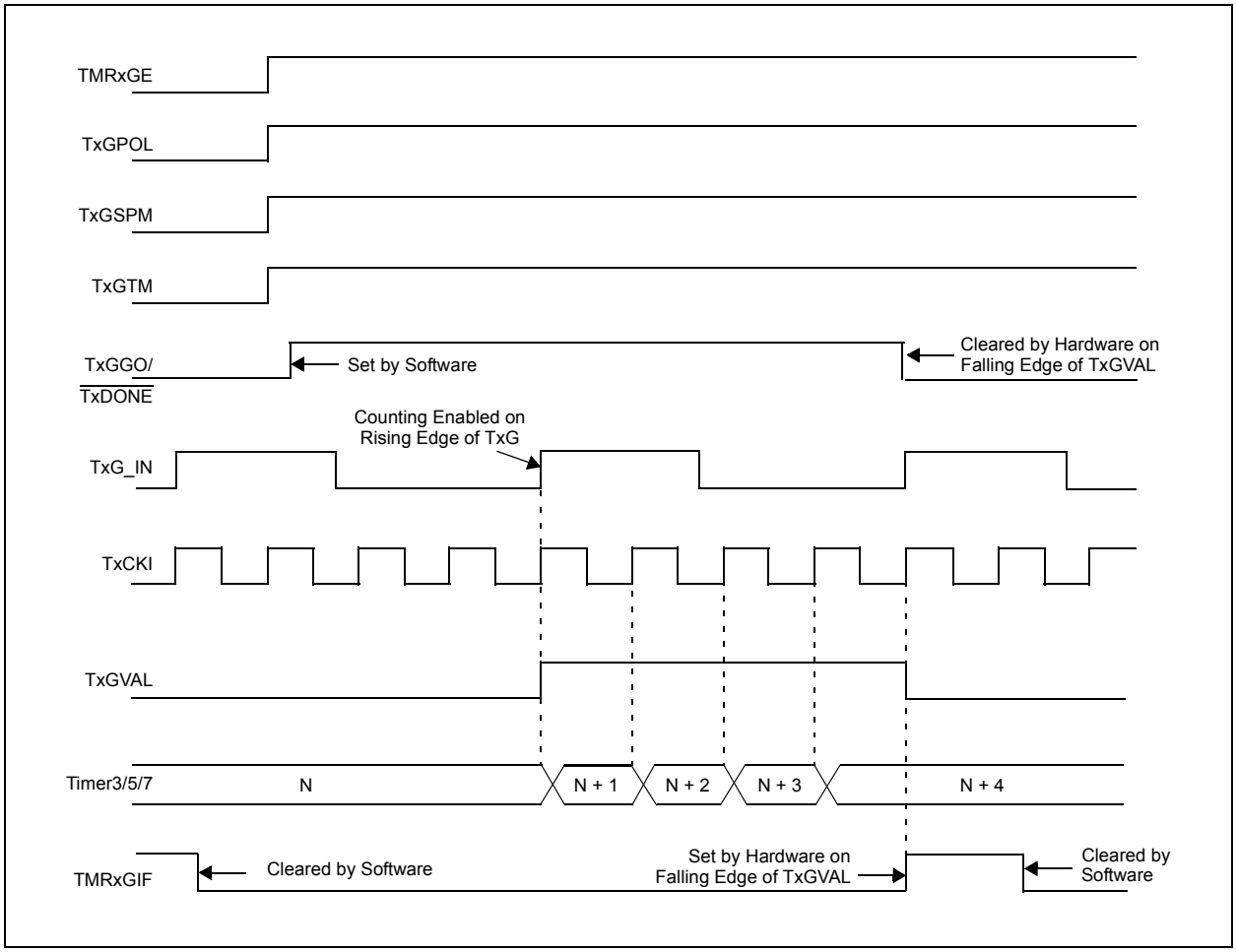
Note: Throughout this section, generic references are used for register and bit names that are the same, except for an 'x' variable that indicates the item's association with the Timer3, Timer5 or Timer7 module. For example, the control register is named TxCON and refers to T3CON, T5CON and T7CON.

A simplified block diagram of the Timer3/5/7 module is shown in Figure 15-1.

The Timer3/5/7 module is controlled through the TxCON register (Register 15-1). It also selects the clock source options for the ECCP modules. (For more information, see **Section 19.1.1 "ECCP Module and Timer Resources"**.)

The FOSC clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

FIGURE 15-5: TIMER3/5/7 GATE SINGLE PULSE AND TOGGLE COMBINED MODE



15.5.5 TIMER3/5/7 GATE VALUE STATUS

When Timer3/5/7 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the TxGVAL bit (TxGCON<2>). The TxGVAL bit is valid even when the Timer3/5/7 gate is not enabled (TMRxGE bit is cleared).

15.5.6 TIMER3/5/7 GATE EVENT INTERRUPT

When the Timer3/5/7 gate event interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of TxGVAL occurs, the TMRxGIF flag bit in the PIRx register will be set. If the TMRxGIE bit in the PIEx register is set, then an interrupt will be recognized.

The TMRxGIF flag bit operates even when the Timer3/5/7 gate is not enabled (TMRxGE bit is cleared).

15.6 Timer3/5/7 Interrupt

The TMRx register pair (TMRxH:TMRxL) increments from 0000h to FFFFh and overflows to 0000h. The Timerx interrupt, if enabled, is generated on overflow and is latched in the interrupt flag bit, TMRxIF. Table 15-3 gives each module's flag bit.

TABLE 15-3: TIMER3/5/7 INTERRUPT FLAG BITS

Timer Module	Flag Bit
3	PIR2<1>
5	PIR5<1>
7	PIR5<3>

This interrupt can be enabled or disabled by setting or clearing the TMRxIE bit, respectively. Table 15-4 gives each module's enable bit.

TABLE 15-4: TIMER3/5/7 INTERRUPT ENABLE BITS

Timer Module	Flag Bit
3	PIE2<1>
5	PIE5<1>
7	PIE5<3>

15.7 Resetting Timer3/5/7 Using the ECCP Special Event Trigger

If the ECCP modules are configured to use Timerx and to generate a Special Event Trigger in Compare mode (CCPxM<3:0> = 1011), this signal will reset Timerx. The trigger from ECCP2 will also start an A/D conversion if the A/D module is enabled. (For more information, see **Section 19.3.4 "Special Event Trigger"**.)

The module must be configured as either a timer or synchronous counter to take advantage of this feature. When used this way, the CCPRxH:CCPRxL register pair effectively becomes a Period register for Timerx.

If Timerx is running in Asynchronous Counter mode, the Reset operation may not work.

In the event that a write to Timerx coincides with a Special Event Trigger from an ECCP module, the write will take precedence.

Note:	The Special Event Triggers from the ECCPx module will only clear the TMR3 register's content, but not set the TMR3IF interrupt flag bit (PIR1<0>).

Note:	The CCP and ECCP modules use Timers, 1 through 8, for some modes. The assignment of a particular timer to a CCP/ECCP module is determined by the Timer to CCP enable bits in the CCPTMRSx registers. For more details, see Register 19-2, Register 18-2 and Register 18-3.

19.3 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against either the TMR1 or TMR3 register pair value. When a match occurs, the ECCPx pin can be:

- Driven high
- Driven low
- Toggled (high-to-low or low-to-high)
- Unchanged (that is, reflecting the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCPxM<3:0>). At the same time, the interrupt flag bit, CCPxIF, is set.

19.3.1 ECCP PIN CONFIGURATION

Users must configure the ECCPx pin as an output by clearing the appropriate TRIS bit.

Note:	Clearing the CCPxCON register will force the ECCPx compare output latch (depending on device configuration) to the default low level. This is not the PORTx I/O data latch.

19.3.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode if the ECCP module is using the compare feature. In Asynchronous Counter mode, the compare operation will not work reliably.

19.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the ECCPx pin is not affected; only the CCPxIF interrupt flag is affected.

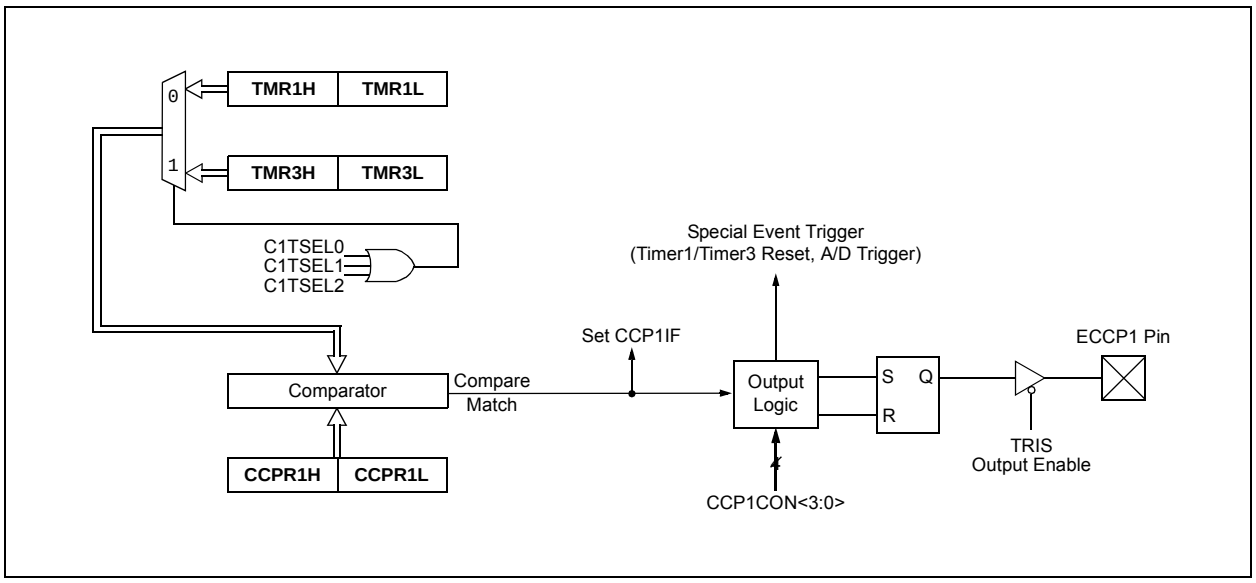
19.3.4 SPECIAL EVENT TRIGGER

The ECCP module is equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

The Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a programmable Period register for either timer.

The Special Event Trigger can also start an A/D conversion. In order to do this, the A/D Converter must already be enabled.

FIGURE 19-2: COMPARE MODE OPERATION BLOCK DIAGRAM

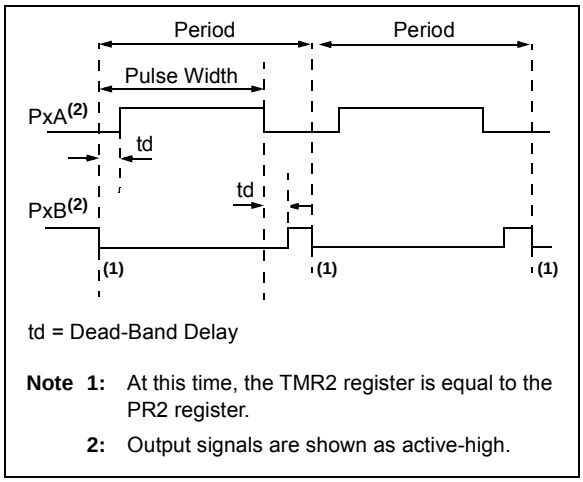


19.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In half-bridge applications, where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on and the other turned off), both switches may be on for a short period until one switch completely turns off. During this brief interval, a very high current (shoot-through current) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. For an illustration, see Figure 19-14. The lower seven bits of the associated ECCPxDEL register (Register 19-4) set the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

FIGURE 19-14: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

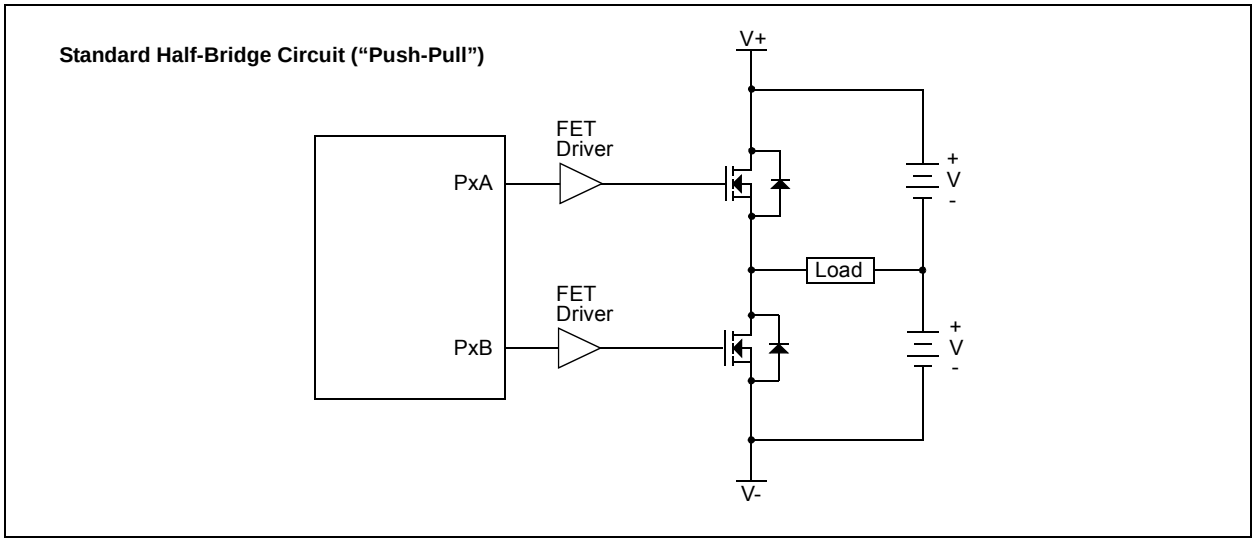


td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.

FIGURE 19-15: EXAMPLE OF HALF-BRIDGE APPLICATIONS



REGISTER 19-4: ECCPxDEL: ENHANCED PWM CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxRSEN	PxDC6	PxDC5	PxDC4	PxDC3	PxDC2	PxDC1	PxDC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PxRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPxASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPxASE must be cleared by software to restart the PWM

bit 6-0 **PxDC<6:0>:** PWM Delay Count bits

PxDCn = Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it does transition active.

19.4.7 PULSE STEERING MODE

In Single Output mode, pulse steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can simultaneously be available on multiple pins.

Once the Single Output mode is selected (CCPxM<3:2> = 11 and PxM<1:0> = 00 of the CCPxCON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STR<D:A> bits (PSTRxCON<3:0>), as provided in Table 19-3.

Note:	The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin.

While the PWM Steering mode is active, the CCPxM<1:0> bits (CCPxCON<1:0>) select the PWM output polarity for the Px<D:A> pins.

The PWM auto-shutdown operation also applies to the PWM Steering mode, as described in **Section 19.4.4 "Enhanced PWM Auto-shutdown mode"**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

21.4.3.2 Address Masking Modes

Masking an address bit causes that bit to become a "don't care". When one address bit is masked, two addresses will be Acknowledged and cause an interrupt. It is possible to mask more than one address bit at a time, which greatly expands the number of addresses Acknowledged.

The I^2C slave behaves the same way whether address masking is used or not. However, when address masking is used, the I^2C slave can Acknowledge multiple addresses and cause interrupts. When this occurs, it is necessary to determine which address caused the interrupt by checking the SSPxBUF.

The PIC18F87K90 family of devices is capable of using two different Address Masking modes in I^2C slave operation: 5-Bit Address Masking and 7-Bit Address Masking. The Masking mode is selected at device configuration using the MSSPMSK Configuration bit. The default device configuration is 7-Bit Address Masking.

Both Masking modes, in turn, support address masking of 7-bit and 10-bit addresses. The combination of Masking modes and addresses provide different ranges of Acknowledgable addresses for each combination.

While both Masking modes function in roughly the same manner, the way they use address masks are different.

21.4.3.3 5-Bit Address Masking Mode

As the name implies, 5-Bit Address Masking mode uses an address mask of up to 5 bits to create a range of addresses to be Acknowledged, using bits, 5 through 1, of the incoming address. This allows the module to Acknowledge up to 31 addresses when using 7-bit addressing, or 63 addresses with 10-bit addressing (see Example 21-2). This Masking mode is selected when the MSSPMSK Configuration bit is programmed ('0').

The address mask in this mode is stored in the SSPxCON2 register, which stops functioning as a control register in I^2C Slave mode (Register 21-6). In 7-Bit Address Masking mode, address mask bits, ADMSK<5:1> (SSPxCON2<5:1>), mask the corresponding address bits in the SSPxADD register. For any ADMSK bits that are set (ADMSK<n> = 1), the corresponding address bit is ignored (SSPxADD<n> = x). For the module to issue an address Acknowledge, it is sufficient to match only on addresses that do not have an active address mask.

In 10-Bit Address Masking mode, bits, ADMSK<5:2>, mask the corresponding address bits in the SSPxADD register. In addition, ADMSK1 simultaneously masks the two LSbs of the address (SSPxADD<1:0>). For any ADMSK bits that are active (ADMSK<n> = 1), the corresponding address bit is ignored (SPxADD<n> = x). Also note, that although in 10-Bit Address Masking mode, the upper address bits reuse part of the SSPxADD register bits. The address mask bits do not interact with those bits; they only affect the lower address bits.

Note 1: ADMSK1 masks the two Least Significant bits of the address.

2: The two Most Significant bits of the address are not affected by address masking.

EXAMPLE 21-2: ADDRESS MASKING EXAMPLES IN 5-BIT MASKING MODE

7-Bit Addressing:

SSPxADD<7:1>= A0h (1010000) (SSPxADD<0> is assumed to be '0')

ADMSK<5:1> = 00111

Addresses Acknowledged: A0h, A2h, A4h, A6h, A8h, AAh, ACh, AEh

10-Bit Addressing:

SSPxADD<7:0> = A0h (10100000) (The two MSb of the address are ignored in this example, since they are not affected by masking)

ADMSK<5:1> = 00111

Addresses Acknowledged: A0h, A1h, A2h, A3h, A4h, A5h, A6h, A7h, A8h, A9h, AAh, ABh, ACh, ADh, AEh, AFh

FIGURE 21-29: BUS COLLISION DURING START CONDITION (SCLx = 0)

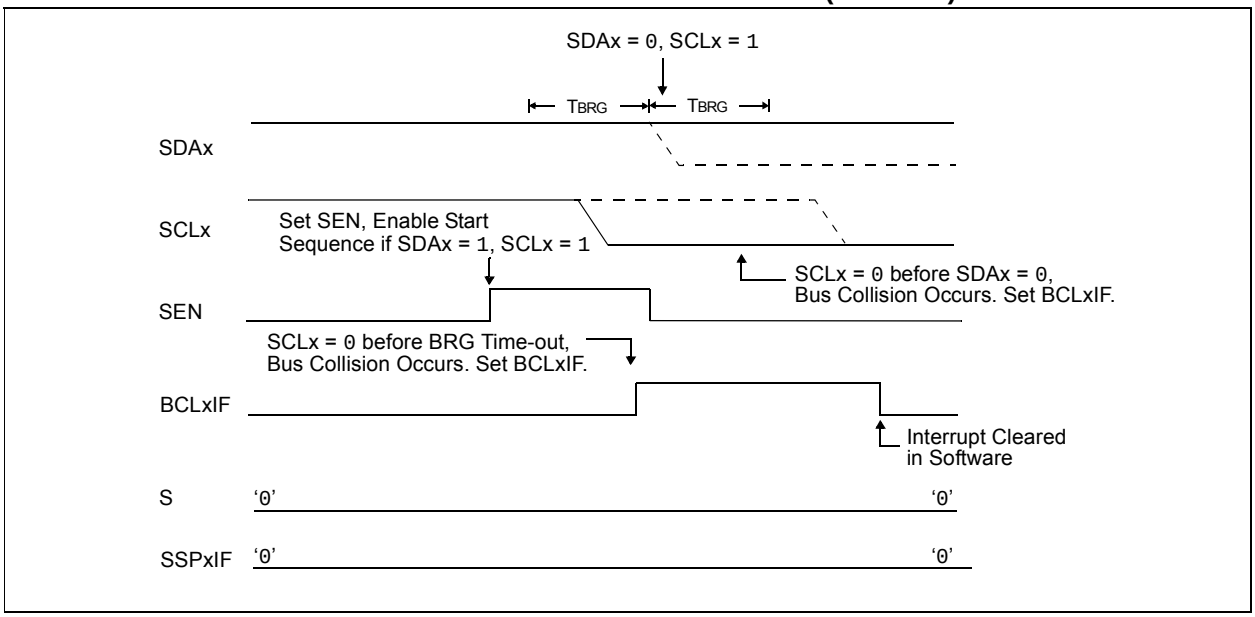


FIGURE 21-30: BRG RESET DUE TO SDAx ARBITRATION DURING START CONDITION

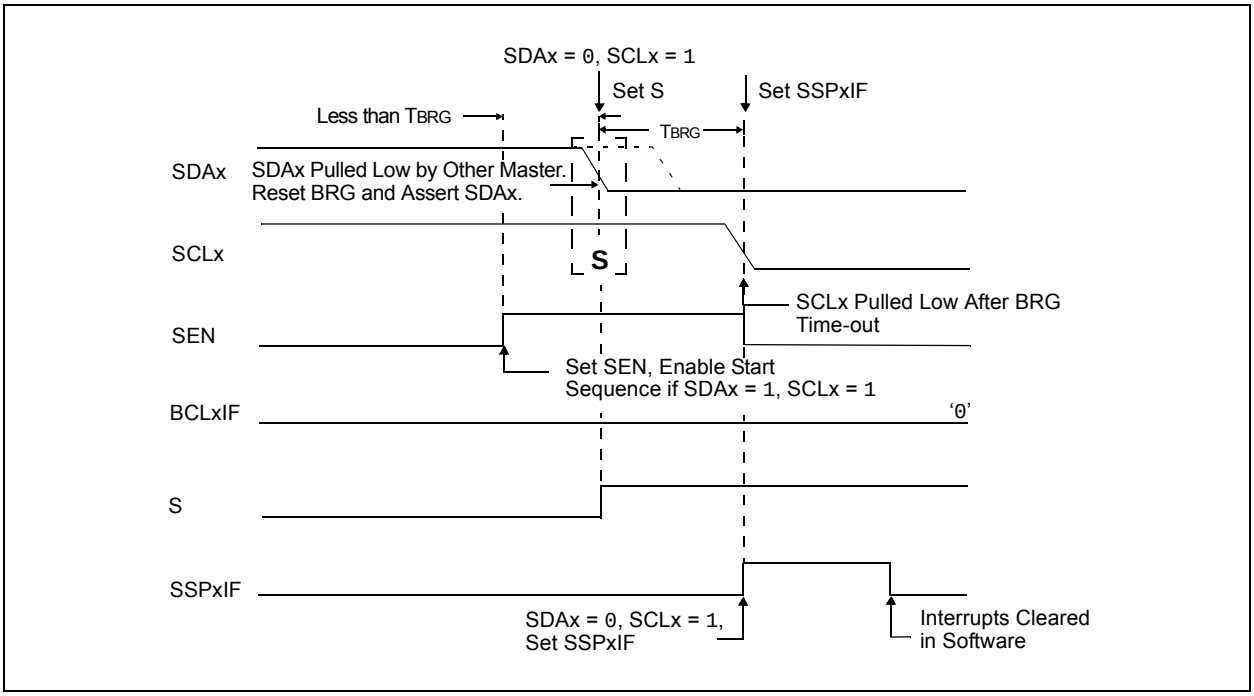


FIGURE 22-4: ASYNCHRONOUS TRANSMISSION

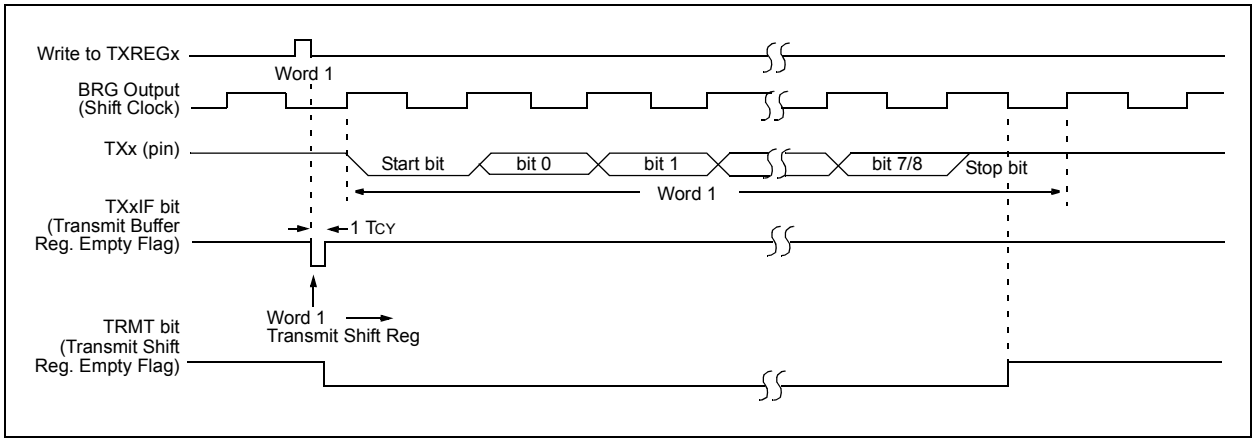
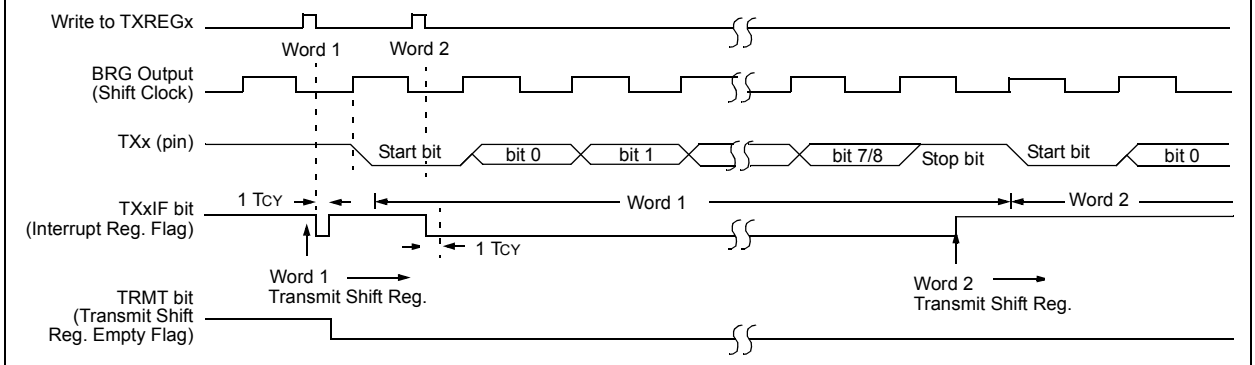


FIGURE 22-5: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

26.2 HLVD Setup

To set up the HLVD module:

1. Select the desired HLVD trip point by writing the value to the HLVDL<3:0> bits.
2. Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
3. Enable the HLVD module by setting the HLVDEN bit.
4. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
5. If interrupts are desired, enable the HLVD interrupt by setting the HLVDIE and GIE bits (PIE2<2> and INTCON<7>, respectively).

   An interrupt will not be generated until the IRVST bit is set.

Note:	Before changing any module settings (VDIRMAG, HLVDL<3:0>), first disable the module (HLVDEN = 0), make the changes and re-enable the module. This prevents the generation of false HLVD events.

26.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and consume static current. The total current consumption, when enabled, is specified in electrical specification Parameter D022B (Table 31-10).

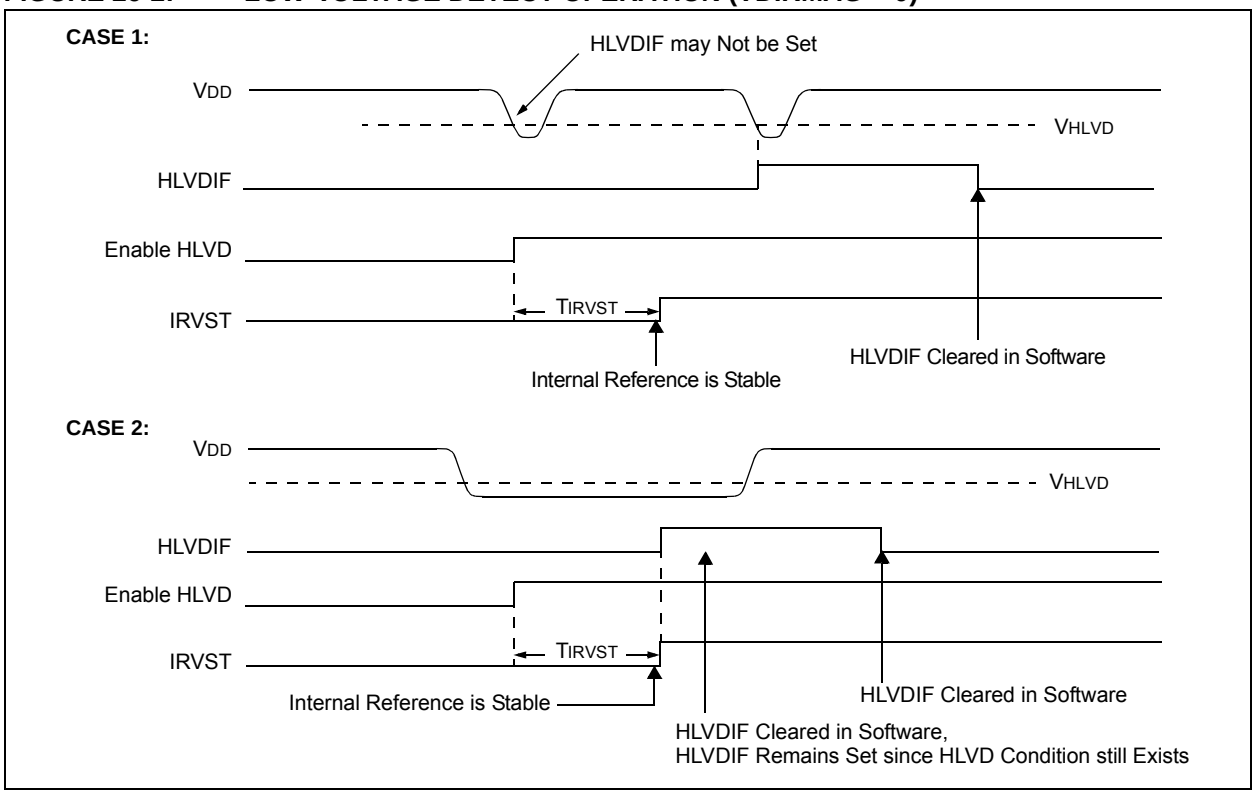
Depending on the application, the HLVD module does not need to operate constantly. To reduce current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After such a check, the module could be disabled.

26.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification Parameter 37 (**Section 31.0 "Electrical Characteristics"**), may be used by other internal circuitry, such as the programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification Parameter 36 (Table 31-10).

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (see Figure 26-2 or Figure 26-3).

FIGURE 26-2: LOW-VOLTAGE DETECT OPERATION (VDIRMAG = 0)



28.2.1 CONTROL REGISTER

Register 28-16 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to override the WDT Enable Configuration bit, but only if the Configuration bit has disabled the WDT.

REGISTER 28-16: WDTCON: WATCHDOG TIMER CONTROL REGISTER

R/W-0	U-0	R-x	R/W-0	U-0	R/W-0	R/W-0	R/W-0
REGSLP	—	ULPLVL(3)	SRETEN(2)	—	ULPEN	ULPSINK(3)	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **REGSLP:** Regulator Voltage Sleep Enable bit
1 = Regulator goes into Low-Power mode when device's Sleep mode is enabled
0 = Regulator stays in normal mode when device's Sleep mode is activated

bit 6 **Unimplemented**: Read as '0'

bit 5 **ULPLVL:** Ultra Low-Power Wake-up Output bit(3)
1 = Voltage on RA0 > ~0.5V
0 = Voltage on RA0 < ~0.5V

bit 4 **SRETEN:** Regulator Voltage Sleep Disable bit(2)
1 = If $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0 and the regulator is enabled, the device goes into Ultra Low-Power mode in Sleep
0 = The regulator is on when the device's Sleep mode is enabled and the Low-Power mode is controlled by REGSLP

bit 3 **Unimplemented**: Read as '0'

bit 2 **ULPEN:** Ultra Low-Power Wake-up (ULPWU) Module Enable bit
1 = Ultra Low-Power Wake-up module is enabled; ULPLVL bit indicates a comparator output
0 = Ultra Low-Power Wake-up module is disabled

bit 1 **ULPSINK:** Ultra Low-Power Wake-up Current Sink Enable bit(3)
1 = Ultra Low-Power Wake-up current sink is enabled
0 = Ultra Low-Power Wake-up current sink is disabled

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit(1)
1 = Watchdog Timer is on
0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bits, WDTEN<1:0>, are enabled.
2: This bit is only available when ENVREG = 1 and $\overline{\text{RETEN}}$ = 0.
3: This bit is not valid unless ULPEN = 1.

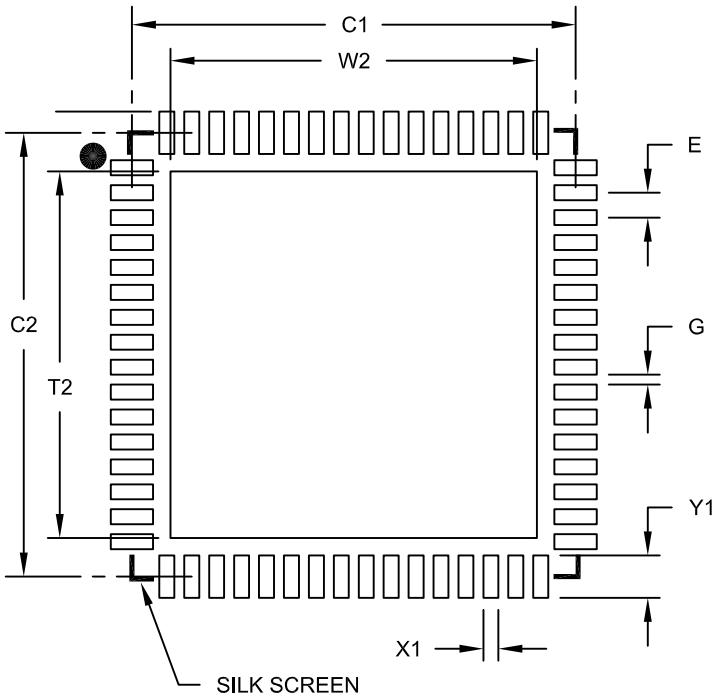
TABLE 28-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
RCON	IPEN	SBOREN	$\overline{\text{CM}}$	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	76
WDTCON	REGSLP	—	ULPLVL	SRETEN	—	ULPEN	ULPSINK	SWDTEN	76

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

RC3/SCK1/SCL1/SEG17 ..... 17, 26
RC4/SDI1/SDA1/SEG16 ..... 17, 26
RC5/SDO1/SEG12 ..... 17, 26
RC6/TX1/CK1/SEG27 ..... 17, 26
RC7/RX1/DT1/SEG28 ..... 17, 26
RD0/SEG0/CTPLS 18, 27
RD1/SEG1/T5CKI/T7G 18, 27
RD2/SEG2 ..... 18, 27
RD3/SEG3 ..... 18, 27
RD4/SEG4/SDO2 ..... 18, 27
RD5/SEG5/SDI2/SDA2 ..... 18, 27
RD6/SEG6/SCK2/SCL2 ..... 18, 27
RD7/SEG7/SS2 ..... 18, 27
RE0/LCDBIAS1/P2D 19, 28
RE1/LCDBIAS2/P2C 19, 28
RE2/LCDBIAS3/P2B/CCP10 ..... 19, 28
RE3/COM0/P3C/CCP9/REFO 19, 28
RE4/COM1/P3B/CCP8 ..... 19, 28
RE5/COM2/P1C/CCP7 ..... 19, 28
RE6/COM3/P1B/CCP6 ..... 19, 28
RE7/ECCP2/P2A/SEG31 28
RE7/ECCP2/SEG31/P2A 19
RF1/AN6/C2OUT/SEG19/CTDIN 20, 29
RF2/AN7/C1OUT/SEG20 20
RF2/AN7/C1OUT/SEG20/CTMUI 29
RF3/AN8/SEG21/C2INB 29
RF3/AN8/SEG21/C2INB/CTMUI 20
RF4/AN9/SEG22/C2INA 20, 29
RF5/AN10 20
RF5/AN10/CVREF/SEG23/C1INB 29
RF6/AN11/SEG24/C1INA 20, 29
RF7/AN5/SS1/SEG25 ..... 20, 29
RG0/ECCP3/P3A 21, 30
RG1/TX2/CK2/AN19/C3OUT 21, 30
RG2/RX2/DT2/AN18/C3INA 21, 30
RG3/CCP4/AN17/P3D/C3INB 21, 30
RG4/SEG26/RTCC/T7CKI/T5G/CCP5/AN16/P1D/C3INC 21, 30
RH0/SEG47/AN23 31
RH1/SEG46/AN22 31
RH2/SEG45/AN21 31
RH3/SEG44/AN20 31
RH4/SEG40/CCP9/P3C/AN12/C2INC 31
RH5/SEG41/CCP8/P3B/AN13/C2IND 31
RH6/SEG42/CCP7/P1C/AN14/C1INC 31
RH7/SEG43/CCP6/P1B/AN15 32
RJ0 33
RJ1/SEG33 33
RJ2/SEG34 33
RJ3/SEG35 33
RJ4/SEG39 33
RJ5/SEG38 33
RJ6/SEG37 33
RJ7/SEG36 33
VDD 22, 33
VDDCORE/VCAP 22, 33
VSS 22, 33
Pinout I/O Descriptions
PIC18F6XK90 14
PIC18F8XK90 22
PIR5 Register
TMR12IF Bit 138
PLL 48
HSPLL and ECPLL Oscillator Modes 48
Use with HF-INTOSC 49
POP 480
POR. *See* Power-on Reset.
PORTA
Associated Registers 159
LATA Register 157
PORTA Register 157
TRISA Register 157
PORTB
Associated Registers 162
LATB Register 160
PORTB Register 160
RB7:RB4 Interrupt-on-Change Flag (RBIF Bit) 160
TRISB Register 160
PORTC
Associated Registers 165
LATC Register 163
PORTC Register 163
TRISC Register 163
PORTD
Associated Registers 168
LATD Register 166
PORTD Register 166
TRISD Register 166
PORTE
Associated Registers 171
LATE Register 169
Pins Available in Different LCD Drives 169
PORTE Register 169
TRISE Register 169
PORTF
Associated Registers 174
LATF Register 172
PORTF Register 172
TRISF Register 172
PORTG
Associated Registers 176
LATG Register 175
PORTG Register 175
TRISG Register 175
PORTH
Associated Registers 179
LATH Register 177
PORTH Register 177
TRISH Register 177
PORTJ
Associated Registers 181
LATJ Register 180
PORTJ Register 180
TRISJ Register 180
Power-Managed Modes 53
and PWM Operation 271
and SPI Operation 311
Clock Transitions and Status Indicators 54
Entering 53
Exiting Idle and Sleep Modes 65
by Interrupt 65
by Reset 65
by WDT Time-out 65
Without an Oscillator Start-up Delay 65
Idle Modes 58
PRI_IDLE 59
RC_IDLE 60
SEC_IDLE 59

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