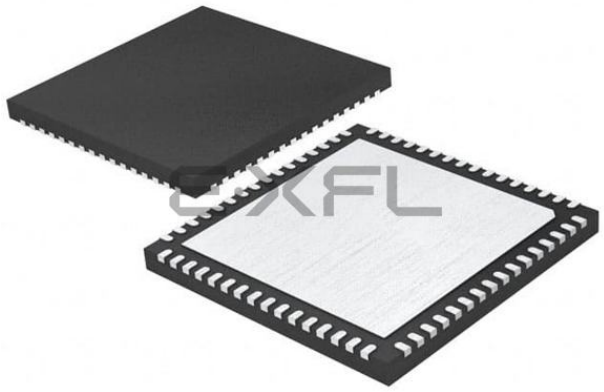


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f67k90-i-mrrsl

TABLE 1-3: PIC18F6XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	QFN/TQFP			
				PORTE is a bidirectional I/O port.
RE0/LCDBIAS1/P2D	2			
RE0		I/O	ST	Digital I/O.
LCDBIAS1		I	Analog	BIAS1 input for LCD.
P2D		O	—	EECP2 PWM Output D.
RE1/LCDBIAS2/P2C	1			
RE1		I/O	ST	Digital I/O.
LCDBIAS2		I	Analog	BIAS2 input for LCD.
P2C		O	—	ECCP2 PWM Output C.
RE2/LCDBIAS3/P2B/CCP10	64			
RE2		I/O	ST	Digital I/O.
LCDBIAS3		I	Analog	BIAS3 input for LCD.
P2B		O	—	ECCP2 PWM Output B.
CCP10(3)		I/O	S/T	Capture 10 input/Compare 10 output/PWM10 output.
RE3/COM0/P3C/CCP9/REFO	63			
RE3		I/O	ST	Digital I/O.
COM0		O	Analog	COM0 output for LCD.
P3C		O	—	ECCP3 PWM Output C.
CCP9(3)		I/O	S/T	Capture 9 input/Compare 9 output/PWM9 output.
REFO		O	—	Reference clock out.
RE4/COM1/P3B/CCP8	62			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
P3B		O	—	ECCP3 PWM Output B.
CCP8		I/O	S/T	Capture 8 input/Compare 8 output/PWM8 output.
RE5/COM2/P1C/CCP7	61			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
P1C		O	—	ECCP1 PWM Output C.
CCP7		I/O	S/T	Capture 7 input/Compare 7 output/PWM7 output.
RE6/COM3/P1B/CCP6	60			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
P1B		O	—	ECCP1 PWM Output B.
CCP6		I/O	S/T	Capture 6 input/Compare 6 output/PWM6 output.
RE7/ECCP2/SEG31/P2A	59			
RE7		I/O	ST	Digital I/O.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 Output for LCD.
P2A		O	—	ECCP2 PWM Output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/SEG47/AN23	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
AN23		I	Analog	Analog Input 23.
RH1/SEG46/AN22	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
AN22		I	Analog	Analog Input 22.
RH2/SEG45/AN21	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
AN21		I	Analog	Analog Input 21.
RH3/SEG44/AN20	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
AN20		I	Analog	Analog Input 20.
RH4/SEG40/CCP9/P3C/AN12/C2INC	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
CCP9(3,4)		I/O	ST	Capture 9 input/Compare 9 output/PWM9 output.
P3C		O	—	ECCP3 PWM Output C.
AN12		I	Analog	Analog Input 12.
C2INC		I	Analog	Comparator 2 Input C.
RH5/SEG41/CCP8/P3B/AN13/C2IND	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
CCP8(4)		I/O	ST	Capture 8 input/Compare 8 output/PWM8 output.
P3B		O	—	ECCP3 PWM Output B.
AN13		I	Analog	Analog Input 13.
C2IND		I	Analog	Comparator 1 Input D.
RH6/SEG42/CCP7/P1C/AN14/C1INC	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
CCP7(4)		I/O	ST	Capture 7 input/Compare 7 output/PWM7 output.
P1C		O	—	ECCP1 PWM Output C.
AN14		I	Analog	Analog Input 14.
C1INC		I	Analog	Comparator 1 Input C.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

3.6.2 INTPLL MODES

The 4x Phase Locked Loop (PLL) can be used with the HF-INTOSC to produce faster device clock speeds than are normally possible with the internal oscillator sources. When enabled, the PLL produces a clock speed of 32 MHz or 64 MHz.

PLL operation is controlled through software. The control bit, PLLEN (OSCTUNE<6>) is used to enable or disable its operation. Additionally, the PLL will only function when the selected HF-INTOSC frequency is either 8 MHz or 16 MHz (OSCCON<6:4> = 111 or 110).

Like the INTIO modes, there are two distinct INTPLL modes available:

- In INTPLL1 mode, the OSC2 pin outputs FOSC/4, while OSC1 functions as RA7 for digital input and output. Externally, this is identical in appearance to INTIO1 (Figure 3-8).
- In INTPLL2 mode, OSC1 functions as RA7 and OSC2 functions as RA6, both for digital input and output. Externally, this is identical to INTIO2 (Figure 3-9).

3.6.3 INTERNAL OSCILLATOR OUTPUT FREQUENCY AND TUNING

The internal oscillator block is calibrated at the factory to produce an INTOSC output frequency of 16 MHz. It can be adjusted in the user's application by writing to TUN<5:0> (OSCTUNE<5:0>) in the OSCTUNE register (Register 3-3).

When the OSCTUNE register is modified, the INTOSC (HF-INTOSC and MF-INTOSC) frequency will begin shifting to the new frequency. The oscillator will require some time to stabilize. Code execution continues during this shift and there is no indication that the shift has occurred.

The LF-INTOSC oscillator operates independently of the HF-INTOSC or the MF-INTOSC source. Any changes in the HF-INTOSC or the MF-INTOSC source, across voltage and temperature, are not necessarily reflected by changes in LF-INTOSC or vice versa. The frequency of LF-INTOSC is not affected by OSCTUNE.

3.6.4 INTOSC FREQUENCY DRIFT

The INTOSC frequency may drift as VDD or temperature changes and can affect the controller operation in a variety of ways. It is possible to adjust the INTOSC frequency by modifying the value in the OSCTUNE register. Depending on the device, this may have no effect on the LF-INTOSC clock source frequency.

Tuning INTOSC requires knowing when to make the adjustment, in which direction it should be made, and in some cases, how large a change is needed. Three compensation techniques are shown here.

3.6.4.1 Compensating with the EUSART

An adjustment may be required when the EUSART begins to generate framing errors or receives data with errors while in Asynchronous mode. Framing errors indicate that the device clock frequency is too high. To adjust for this, decrement the value in OSCTUNE to reduce the clock frequency. On the other hand, errors in data may suggest that the clock speed is too low. To compensate, increment OSCTUNE to increase the clock frequency.

3.6.4.2 Compensating with the Timers

This technique compares device clock speed to some reference clock. Two timers may be used; one timer is clocked by the peripheral clock, while the other is clocked by a fixed reference source, such as the SOSC oscillator.

Both timers are cleared, but the timer clocked by the reference source generates interrupts. When an interrupt occurs, the internally clocked timer is read and both timers are cleared. If the internally clocked timer value is much greater than expected, then the internal oscillator block is running too fast. To adjust for this, decrement the OSCTUNE register.

3.6.4.3 Compensating with the CCP Module in Capture Mode

A CCP module can use free-running Timer1 (or Timer3), clocked by the internal oscillator block and an external event with a known period (i.e., AC power frequency). The time of the first event is captured in the CCPRxH:CCPRxL registers and is recorded for use later. When the second event causes a capture, the time of the first event is subtracted from the time of the second event. Since the period of the external event is known, the time difference between events can be calculated.

If the measured time is much greater than the calculated time, the internal oscillator block is running too fast. To compensate, decrement the OSCTUNE register. If the measured time is much less than the calculated time, the internal oscillator block is running too slow. To compensate, increment the OSCTUNE register.

© 2009-2011 Microchip Technology Inc.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
TOSU	PIC18F6XK90	PIC18F8XK90	---0 0000	---0 0000	---0 uuuu(1)
TOSH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu(1)
TOSL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu(1)
STKPTR	PIC18F6XK90	PIC18F8XK90	00-0 0000	uu-0 0000	uu-u uuuu(1)
PCLATU	PIC18F6XK90	PIC18F8XK90	---0 0000	---0 0000	---u uuuu
PCLATH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PCL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
TBLPTRH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TABLAT	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PRODH	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	PIC18F6XK90	PIC18F8XK90	0000 000x	0000 000u	uuuu uuuu(3)
INTCON2	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu(3)
INTCON3	PIC18F6XK90	PIC18F8XK90	1100 0000	1100 0000	uuuu uuuu(3)
INDF0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTINC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTDEC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PREINC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PLUSW0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
FSR0H	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu
FSR0L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTINC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTDEC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PREINC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PLUSW1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
FSR1H	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu
FSR1L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

TABLE 6-2: PIC18F87K90 FAMILY REGISTER FILE SUMMARY

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
EF4h	LCDCON	LCDEN	SLPEN	WERR	—	CS1	CS0	LMUX1	LMUX0	000- 0000
EF5h	LCDPS	WFT	BIASMD	LCDA	WA	LP3	LP2	LP1	LP0	0000 0000
EF6h	LCDSE0	SE07	SE06	SE05	SE04	SE03	SE02	SE01	SE00	0000 0000
EF7h	LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	0000 0000
EF8h	LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000
EF9h	LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000
EFAh	LCDSE4	SE39	SE38	S37	SE36	SE35	SE34	SE33	SE32	0000 0000
EFBh	LCDSE5(2)	SE47	SE46	SE45	SE44	SE43	SE42	SE41	SE40	0000 0000
EFCh	LCDRL	LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0	0000 -000
EFDh	LCDREF	LCDIRE	LCDIRS	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE	0000 0000
EFEh	SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000
EFFh	SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
F00h	SSP2STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000
F01h	SSP2ADD	MSSP Address Register in I^{2}C™ Slave Mode. SSP1 Baud Rate Reload Register in I^{2}C Master Mode								0000 0000
F02h	SSP2BUF	MSSP Receive Buffer/Transmit Register								xxxx xxxx
F03h	T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000
F04h	PR4	Timer4 Period Register								0000 0000
F05h	TMR4	Timer4 Register								1111 1111
F06h	CCP7CON	—	—	DC7B1	DC7B0	CCP7M3	CCP7M2	CCP7M1	CCP7M0	--00 0000
F07h	CCPR7L	Capture/Compare/PWM Register 7 Low Byte								xxxx xxxx
F08h	CCPR7H	Capture/Compare/PWM Register7 High Byte								xxxx xxxx
F09h	CCP6CON	—	—	DC6B1	DC6B0	CCP6M3	CCP6M2	CCP6M1	CCP6M0	--00 0000
F0Ah	CCPR6L	Capture/Compare/PWM Register 6 Low Byte								xxxx xxxx
F0Bh	CCPR6H	Capture/Compare/PWM Register6 High Byte								xxxx xxxx
F0Ch	CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	--00 0000
F0Dh	CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx
F0Eh	CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx
F0Fh	CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000
F10h	CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx
F11h	CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx
F12h	T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/$\overline{T5DONE}$	T5GVAL	T5GSS1	T5GSS0	0000 0000
F13h	T5CON	TMR5CS1	TMR5CS0	T5CKPS1	T5CKPS0	SOSCEN	$\overline{T5SYNC}$	RD16	TMR5ON	0000 0000
F14h	TMR5L	Timer5 Register Low Byte								0000 0000
F15h	TMR5H	Timer5 Register High Byte								xxxx xxxx
F16h	PMD3	CCP10MD(3)	CCP9MD(3)	CCP8MD	CCP7MD	CCP6MD	CCP5MD	CCP4MD	TMR12MD(3)	0000 0000
F17h	PMD2	TMR10MD(3)	TMR8MD	TMR7MD(3)	TMR6MD	TMR5MD	CMP3MD	CMP2MD	CMP1MD	0000 0000
F18h	PMD1	—	CTMUMD	RTCCMD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	—	-000 000-
F19h	PMD0	CCP3MD	CCP2MD	CCP1MD	UART2MD	UART1MD	SSP2MD	SSP1MD	ADCMD	0000 0000
F1Ah	PSTR3CON	CMPL1	CMPL0	—	STRSYNC	STRD	STRC	STRB	STRA	00-0 0001
F1Bh	PSTR2CON	CMPL1	CMPL0	—	STRSYNC	STRD	STRC	STRB	STRA	00-0 0001
F1Ch	TXREG2	Transmit Data FIFO								xxxx xxxx
F1Dh	RCREG2	Receive Data FIFO								0000 0000
F1Eh	SPBRG2	USART2 Baud Rate Generator Low Byte								0000 0000
F1Fh	SPBRGH2	USART2 Baud Rate Generator High Byte								0000 0000
F20h	BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	0100 0-00
F21h	TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010
F22h	RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x
F23h	ANCON2	ANSEL23	ANSEL22	ANSEL21	ANSEL20	ANSEL19	ANSEL18	ANSEL17	ANSEL16	1111 1111

Note 1: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.
2: Unimplemented in 64-pin devices (PIC18F6XK90).
3: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

EXAMPLE 7-3: WRITING TO FLASH PROGRAM MEMORY

```
                MOVLW   SIZE_OF_BLOCK          ; number of bytes in erase block
                MOVWF   COUNTER
                MOVLW   BUFFER_ADDR_HIGH       ; point to buffer
                MOVWF   FSR0H
                MOVLW   BUFFER_ADDR_LOW
                MOVWF   FSR0L
                MOVLW   CODE_ADDR_UPPER        ; Load TBLPTR with the base
                MOVWF   TBLPTRU                ; address of the memory block
                MOVLW   CODE_ADDR_HIGH
                MOVWF   TBLPTRH
                MOVLW   CODE_ADDR_LOW
                MOVWF   TBLPTRL
READ_BLOCK
                TBLRD*+                        ; read into TABLAT, and inc
                MOVF    TABLAT, W              ; get data
                MOVWF   POSTINC0               ; store data
                DECFSZ  COUNTER                ; done?
                BRA     READ_BLOCK             ; repeat
MODIFY_WORD
                MOVLW   DATA_ADDR_HIGH         ; point to buffer
                MOVWF   FSR0H
                MOVLW   DATA_ADDR_LOW
                MOVWF   FSR0L
                MOVLW   NEW_DATA_LOW           ; update buffer word
                MOVWF   POSTINC0
                MOVLW   NEW_DATA_HIGH
                MOVWF   INDF0
ERASE_BLOCK
                MOVLW   CODE_ADDR_UPPER        ; load TBLPTR with the base
                MOVWF   TBLPTRU                ; address of the memory block
                MOVLW   CODE_ADDR_HIGH
                MOVWF   TBLPTRH
                MOVLW   CODE_ADDR_LOW
                MOVWF   TBLPTRL
                BSF     EECON1, EEPGD          ; point to Flash program memory
                BCF     EECON1, CFGS           ; access Flash program memory
                BSF     EECON1, WREN           ; enable write to memory
                BSF     EECON1, FREE           ; enable Row Erase operation
                BCF     INTCON, GIE            ; disable interrupts
                MOVLW   0x55
Required        MOVWF   EECON2                 ; write 55h
Sequence        MOVLW   0xAA
                MOVWF   EECON2                 ; write 0AAh
                BSF     EECON1, WR             ; start erase (CPU stall)
                BSF     INTCON, GIE            ; re-enable interrupts
                TBLRD*-                        ; dummy read decrement
                MOVLW   BUFFER_ADDR_HIGH       ; point to buffer
                MOVWF   FSR0H
                MOVLW   BUFFER_ADDR_LOW
                MOVWF   FSR0L
WRITE_BUFFER_BACK
                MOVLW   SIZE_OF_BLOCK          ; number of bytes in holding register
                MOVWF   COUNTER
WRITE_BYTE_TO_HREGS
                MOVFF   POSTINC0, WREG         ; get low byte of buffer data
                MOVWF   TABLAT                 ; present data to table latch
                TBLWT+*                        ; write data, perform a short write
                                               ; to internal TBLWT holding register.
                DECFSZ  COUNTER                ; loop until buffers are full
                GOTO    WRITE_BYTE_TO_HREGS
```


© 2009-2011 Microchip Technology Inc.

REGISTER 10-11: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIE	—	SSP2IE	BCL2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIE:** Oscillator Fail Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **SSP2IE:** Master Synchronous Serial Port 2 Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 4 **BCL2IE:** Bus Collision Interrupt Enable bit
1 = Enables the bus collision interrupt
0 = Disables the bus collision interrupt

bit 3 **BCL1IE:** Bus Collision Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **TMR3IE:** TMR3 Overflow Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **TMR3GIE:** Timer3 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

11.6 PORTE, TRISE and LATE Registers

PORTE is an 8-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISE and LATE.

All pins on PORTE are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. The RE7 pin is also configurable for open-drain output when ECCP2 is active on this pin. Open-drain configuration is selected by setting the CCP2OD control bit (ODCON1<6>)

Note:	These pins are configured as digital inputs on any device Reset.

Each of the PORTE pins has a weak internal pull-up. A single control bit can turn off all the pull-ups. This is performed by clearing bit, REPU (PADCFG1<6>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on any device Reset.

Pins, RE<6:3>, are multiplexed with the LCD common drives. I/O port functions are available only on those PORTE pins according to which commons are active. The configuration is determined by the LMUX<1:0> control bits (LCDCON<1:0>). The availability is summarized in Table 11-9.

TABLE 11-9: PORTE PINS AVAILABLE IN DIFFERENT LCD DRIVE CONFIGURATIONS(1)

LCDCON <1:0>	Active LCD Commons	PORTE Pins Available for I/O
00	COM0	RE6, RE5, RE4
01	COM0, COM1	RE6, RE5
10	COM0, COM1 and COM2	RE6
11	All (COM0 through COM3)	None

Note 1: If the LCD bias voltages are generated using the internal resistor ladder, the LCDBIASx pins are also available as I/O ports (RE0, RE1 and RE2).

Pins, RE2, RE1 and RE0, are multiplexed with the functions of LCDBIAS3, LCDBIAS2 and LCDBIAS1. When LCD bias generation is required (in any application where the device is connected to an external LCD), these pins cannot be used as digital I/O. These pins can be used as digital I/O, however, when the internal resistor ladder is used for bias generation.

PORTE is also multiplexed with the Enhanced PWM Outputs B and C for ECCP1 and ECCP3, and Outputs B, C and D for ECCP2. For all devices, their default assignments are on PORTE<6:0>. On 80-pin devices, the multiplexing for the outputs of ECCP1 and ECCP3 is controlled by the ECCPMX Configuration bit. Clearing this bit reassigns the P1B/P1C and P3B/P3C outputs to PORTH.

RE7 is multiplexed with the LCD segment drive (SEG31) that is controlled by the LCDSE3<7> bit. I/O port function is only available when the segment is disabled. RE7 can also be configured as the alternate peripheral pin for the ECCP2 module. This is done by clearing the CCP2MX Configuration bit.

RE3 can also be configured as the Reference Clock Output (REFO) from the system clock. For further details, refer to **Section 3.7 “Reference Clock Output”**.

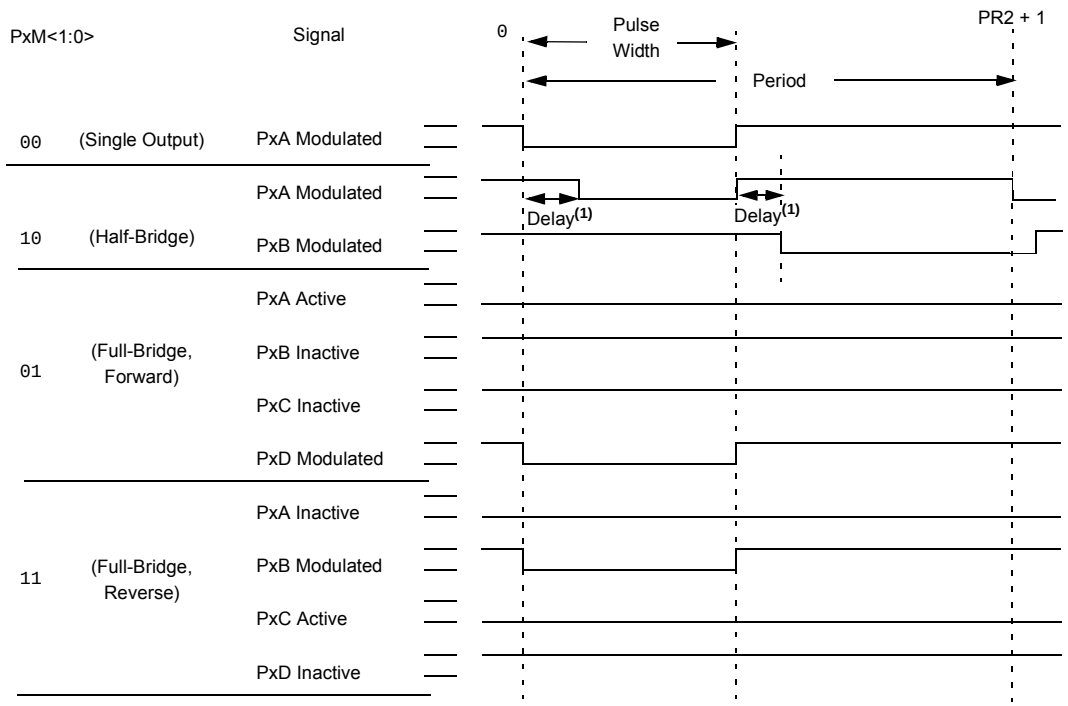
EXAMPLE 11-5: INITIALIZING PORTE

```
CLRF    PORTE   ; Initialize PORTE by
                ; clearing output
                ; data latches
CLRF    LATE    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   03h     ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISE   ; Set RE<1:0> as inputs
                ; RE<7:2> as outputs
```

NOTES:

© 2009-2011 Microchip Technology Inc.

FIGURE 19-5: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



Relationships:

- Period = 4 * TOSC * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = TOSC * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * TOSC * (ECCPxDEL<6:0>)

Note 1: Dead-band delay is programmed using the ECCP1DEL register (see **Section 19.4.6 "Programmable Dead-Band Delay Mode"**).

20.3.2 INTERNAL RESISTOR BIASING

This mode does not use external resistors, but rather internal resistor ladders that are configured to generate the bias voltage.

The internal reference ladder actually consists of three separate ladders. Disabling the internal reference ladder disconnects all of the ladders, allowing external voltages to be supplied.

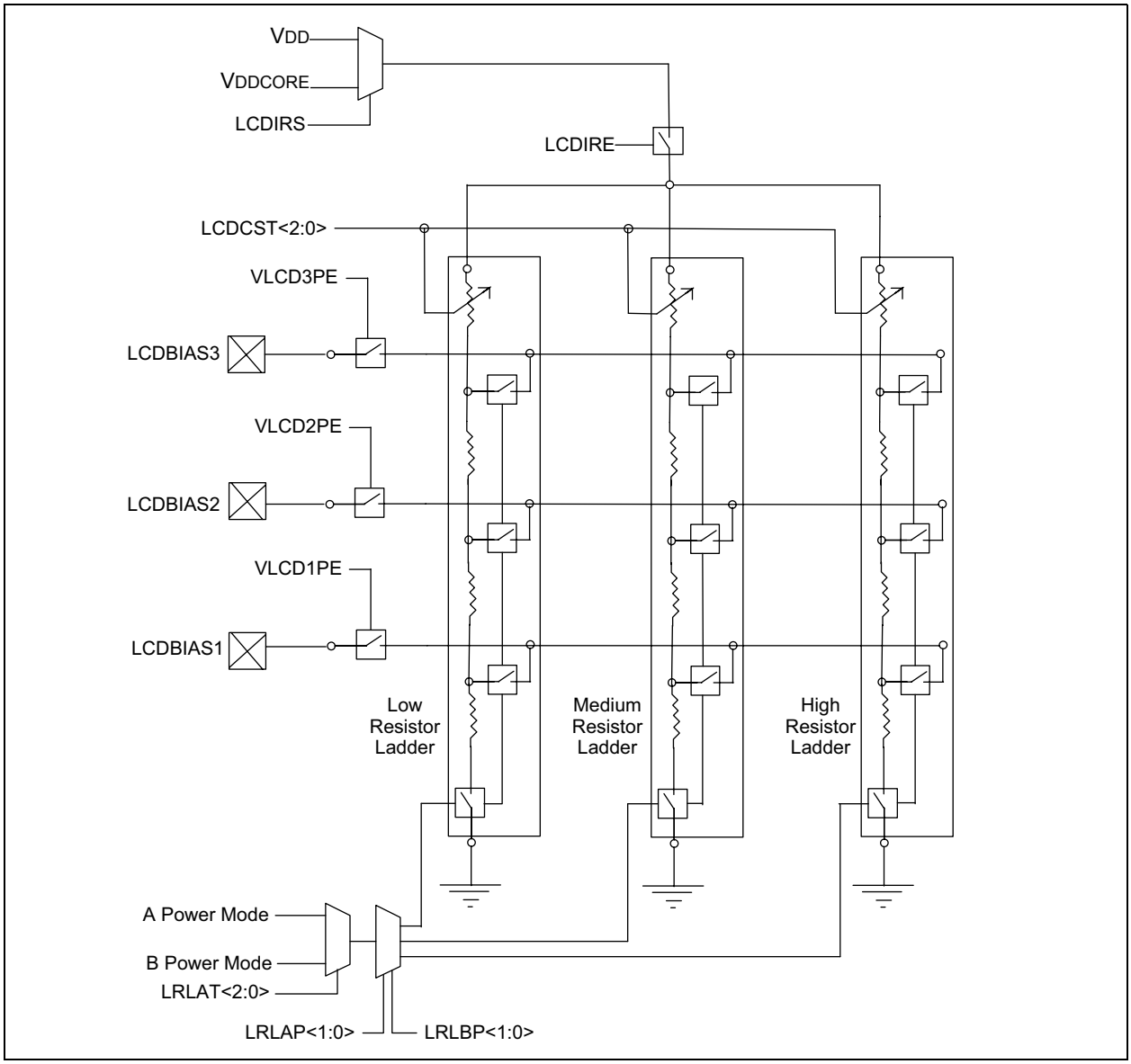
Depending on the total resistance of the resistor ladders, the biasing can be classified as low, medium or high power.

Table 20-3 shows the total resistance of each of the ladders. Figure 20-4 shows the internal resister ladder connections. When the internal resistor ladder is selected, the bias voltage can either be from VDD or from VDDCORE, depending on the LCDIRS setting.

TABLE 20-3: INTERNAL RESISTANCE LADDER POWER MODES

Power Mode	Nominal Resistance of Entire Ladder	IDD
Low	3 MΩ	1 μA
Medium	300 kΩ	10 μA
High	30 kΩ	100 μA

FIGURE 20-4: LCD BIAS INTERNAL RESISTOR LADDER CONNECTION DIAGRAM



© 2009-2011 Microchip Technology Inc.

FIGURE 21-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

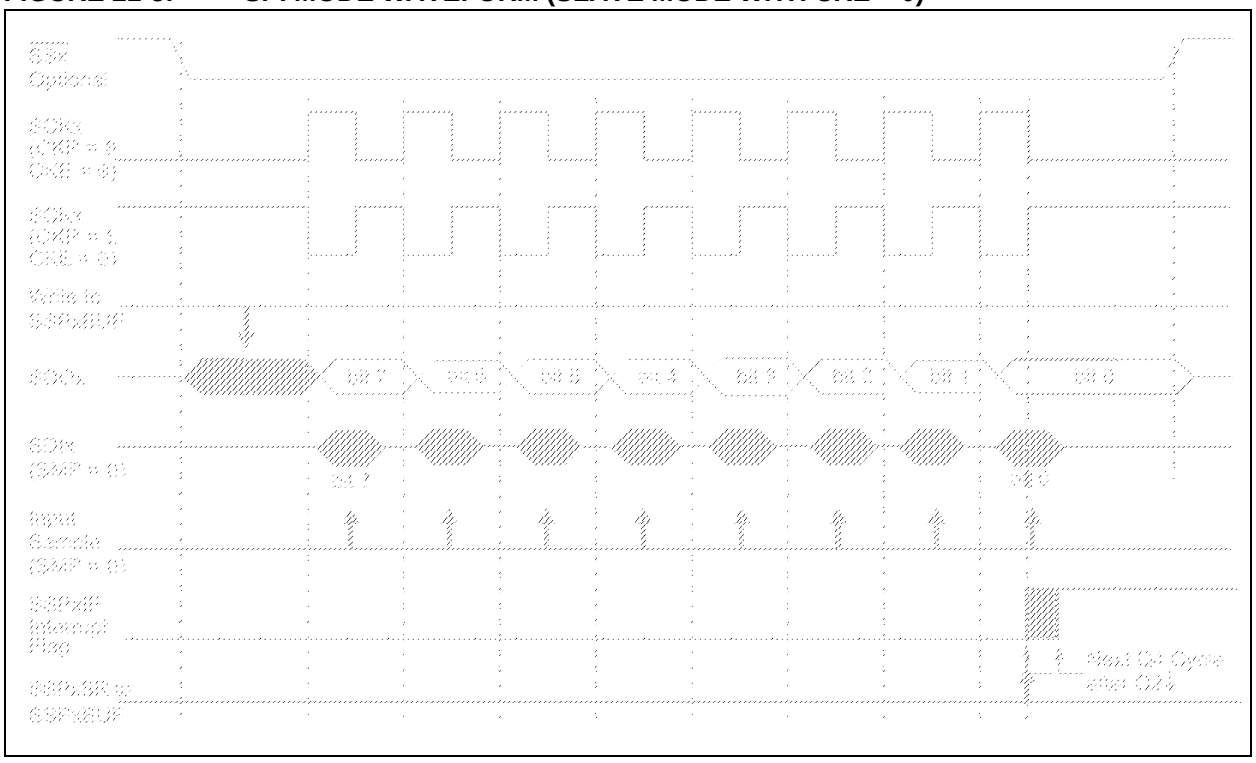
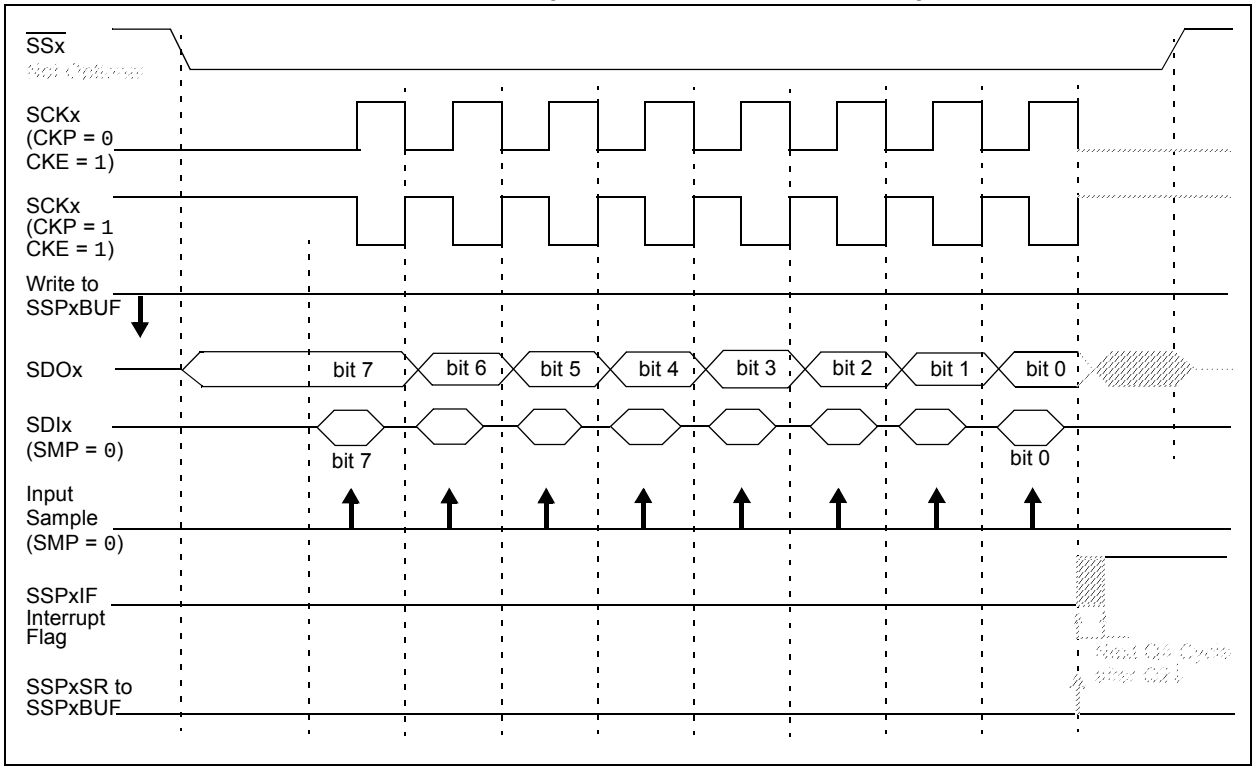


FIGURE 21-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



© 2009-2011 Microchip Technology Inc.

21.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPxCON1 and by setting the SSPEN bit. In Master mode, the SCLx and SDAx lines are manipulated by the MSSP hardware if the TRIS bits are set.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is Idle, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I^2C bus operations based on Start and Stop bit conditions.

Once Master mode is enabled, the user has six options.

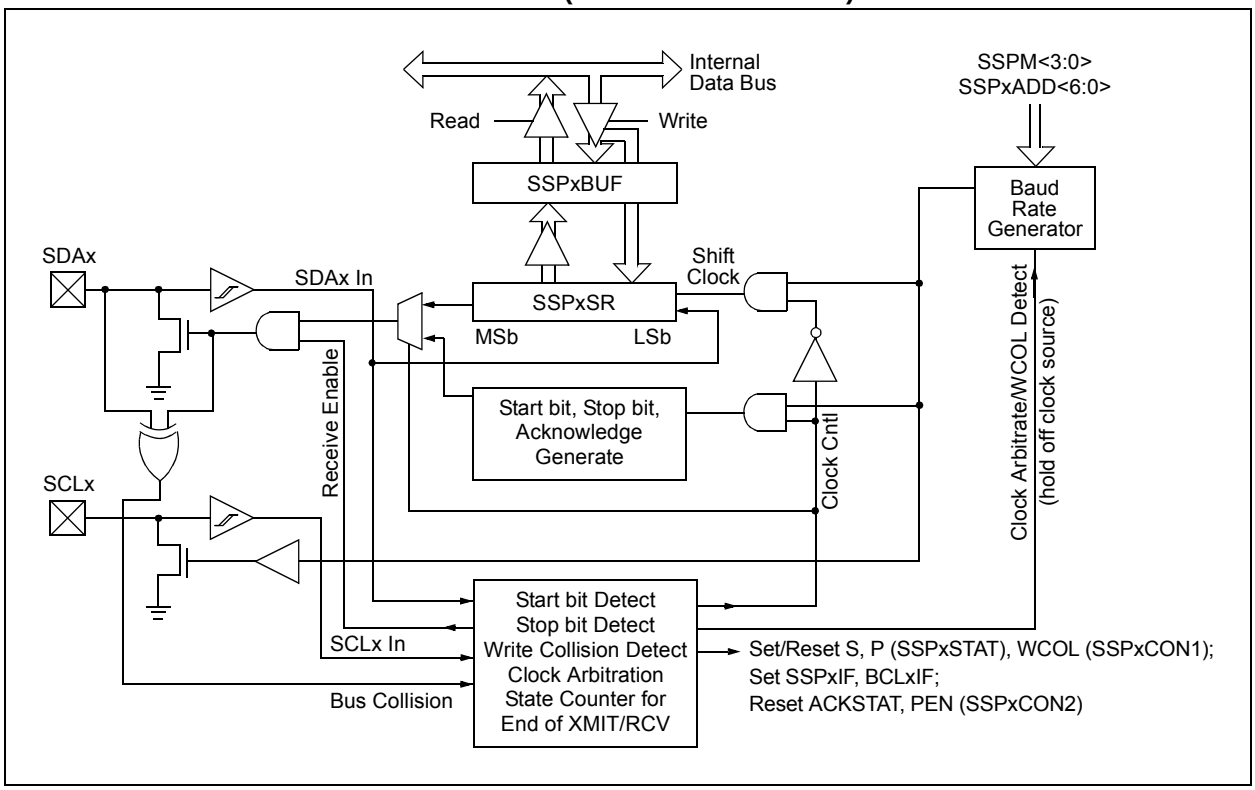
1. Assert a Start condition on SDAx and SCLx.
2. Assert a Repeated Start condition on SDAx and SCLx.
3. Write to the SSPxBUF register, initiating transmission of data/address.
4. Configure the I^2C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a Stop condition on SDAx and SCLx.

Note: The MSSPx module, when configured in I^2C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur.

The following events will cause the MSSPx Interrupt Flag bit, SSPxIF, to be set (and MSSP interrupt, if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received
- Acknowledge transmitted
- Repeated Start

FIGURE 21-18: MSSP BLOCK DIAGRAM (I^2C™ MASTER MODE)



The module is enabled by setting the HLVDEN bit (HLVDCON<4>). Each time the HLVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit (HLVDCON<5>) is a read-only bit used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set.

The VDIRMAG bit (HLVDCON<7>) determines the overall operation of the module. When VDIRMAG is cleared, the module monitors for drops in VDD below a predetermined set point. When the bit is set, the module monitors for rises in VDD above the set point.

26.1 Operation

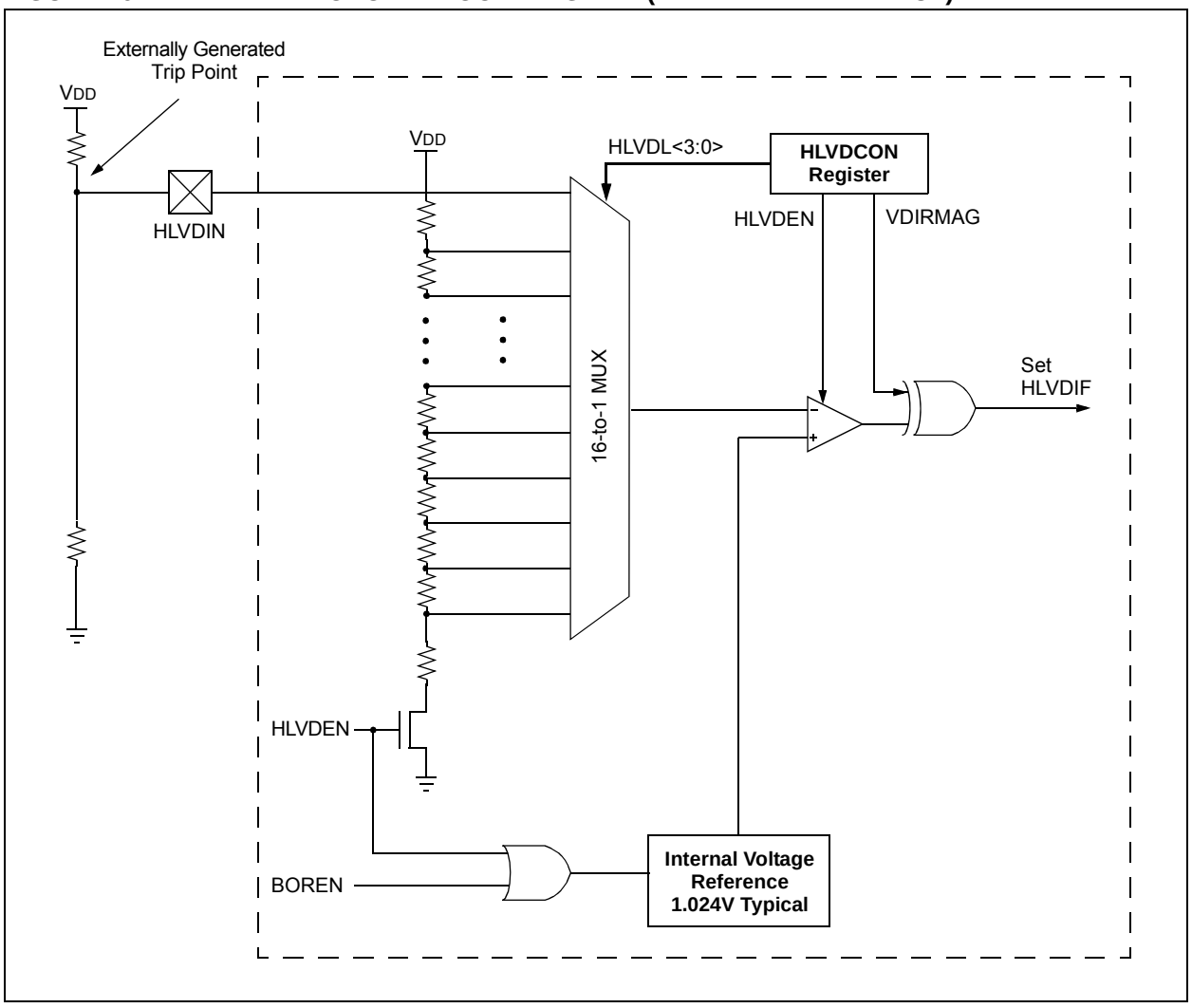
When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module.

When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any of 16 values. The trip point is selected by programming the HLVDL<3:0> bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL<3:0>, are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users the flexibility of configuring the High/Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 26-1: HLVD MODULE BLOCK DIAGRAM (WITH EXTERNAL INPUT)



© 2009-2011 Microchip Technology Inc.

EXAMPLE 27-3: CAPACITANCE CALIBRATION ROUTINE

```
#include "p18cxxx.h"

#define COUNT 25                        //@ 8MHz INTFRC = 62.5 us.
#define ETIME COUNT*2.5                 //time in uS
#define DELAY for(i=0;i<COUNT;i++)
#define ADSCALE 1023                    //for unsigned conversion 10 sig bits
#define ADREF 3.3                       //Vdd connected to A/D Vr+
#define RCAL .027                       //R value is 4200000 (4.2M)
                                        //scaled so that result is in
                                        //1/100th of uA

int main(void)
{
    int i;
    int j = 0;                          //index for loop
    unsigned int Vread = 0;
    float CTMUISrc, CTMUCap, Vavg, VTot, Vcal;

//assume CTMU and A/D have been setup correctly
//see Example 25-1 for CTMU & A/D setup
setup();

CTMUCONHbits.CTMUEN = 1;                //Enable the CTMU
    for(j=0;j<10;j++)
    {
        CTMUCONHbits.IDISSEN = 1;       //drain charge on the circuit
        DELAY;                          //wait 125us
        CTMUCONHbits.IDISSEN = 0;       //end drain of circuit

        CTMUCONLbits.EDG1STAT = 1;      //Begin charging the circuit
                                        //using CTMU current source
        DELAY;                          //wait for 125us
        CTMUCONLbits.EDG1STAT = 0;      //Stop charging circuit

        PIR1bits.ADIF = 0;              //make sure A/D Int not set
        ADCON0bits.GO=1;                //and begin A/D conv.
        while(!PIR1bits.ADIF);          //Wait for A/D convert complete


        Vread = ADRES;                  //Get the value from the A/D
        PIR1bits.ADIF = 0;              //Clear A/D Interrupt Flag
        VTot += Vread;                  //Add the reading to the total
    }

    Vavg = (float)(VTot/10.000);        //Average of 10 readings
    Vcal = (float)(Vavg/ADSCALE*ADREF);
    CTMUISrc = Vcal/RCAL;               //CTMUISrc is in 1/100ths of uA
    CTMUCap = (CTMUISrc*ETIME/Vcal)/100;
}
```

NOTES:

© 2009-2011 Microchip Technology Inc.

REGISTER 28-7: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/P-1	U-0	U-0	R/P-0	U-0	R/P-0	U-0	R/P-1
$\overline{\text{DEBUG}}$	—	—	BBSIZ0	—	—	—	STVREN
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Background debugger is disabled, RB6 and RB7 are configured as general purpose I/O pins
0 = Background debugger is enabled, RB6 and RB7 are dedicated to In-Circuit Debug

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **BBSIZ<0>:** Boot Block Size Select bit
1 = 2 kW boot block size
0 = 1 kW boot block size

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **STVREN:** Stack Full/Underflow Reset Enable bit
1 = Stack full/underflow will cause a Reset
0 = Stack full/underflow will not cause a Reset

© 2009-2011 Microchip Technology Inc.

28.3.2 OPERATION OF REGULATOR IN SLEEP

The difference in the two regulators' operation arises with Sleep mode. The ultra low-power regulator gives the device the lowest current in the Regulator Enabled mode.

The on-chip regulator can go into a lower power mode, when the device goes to Sleep, by setting the REGSLP bit (WDTCON<7>). This puts the regulator in a standby mode so that the device consumes much less current.

The on-chip regulator can also go into the Ultra Low-Power mode, which consumes the lowest current possible with the regulator enabled. This mode is controlled by the $\overline{\text{RETEN}}$ bit (CONFIG1L<0>) and SRETEN bit (WDTCON<4>).

The various modes of regulator operation are shown in Table 28-3.

When the ultra low-power regulator is in Sleep mode, the internal reference voltages in the chip will be shut off and any interrupts referring to the internal reference will not wake up the device. If the BOR or LVD is enabled, the regulator will keep the internal references on and the lowest possible current will not be achieved.

When using the ultra low-power regulator in Sleep mode, the device will take about 250 μs, typical, to start executing the code after it wakes up.

TABLE 28-3: SLEEP MODE REGULATOR SETTINGS(1)

Regulator	Power Mode	VREGSLP WDTCON<7>	SRETEN WDTCON<4>	$\overline{\text{RETEN}}$ CONFIG1L<0>
Enabled	Normal Operation (Sleep)	0	x	1
Enabled	Low-Power mode (Sleep)	1	x	1
Enabled	Normal Operation (Sleep)	0	0	x
Enabled	Low-Power mode (Sleep)	1	0	x
Enabled	Ultra Low-Power mode (Sleep)	x	1	0

Note 1: x = Indicates that VIT status is invalid.

31.0 ELECTRICAL CHARACTERISTICS

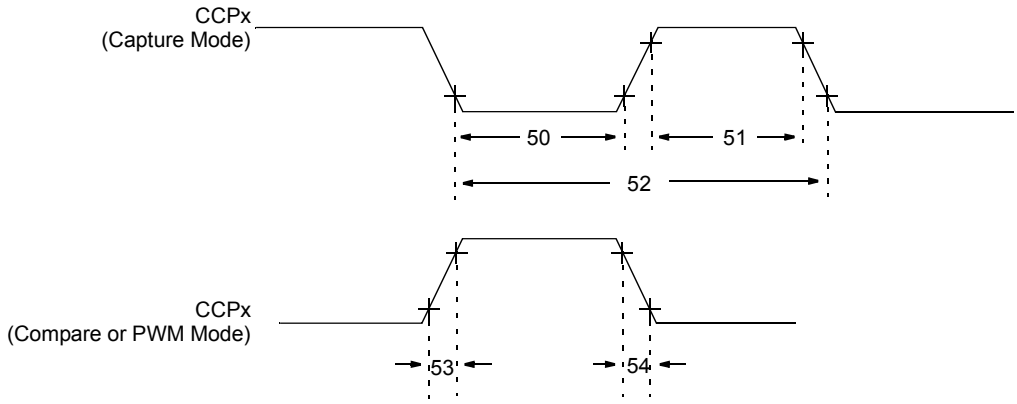
Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on any digital only I/O pin with respect to V_{SS} (except V_{DD}) ..... -0.3V to 7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... -0.3V to +9.0V
Voltage on any combined digital and analog pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on V_{DD} with respect to V_{SS} (regulator enabled) ..... -0.3V to 5.5V
Voltage on V_{DD} with respect to V_{SS} (regulator disabled) ..... -0.3V to 3.6V
Total power dissipation **(Note 1)** 1W
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by PORTA<7:6> and any PORTB and PORTC I/O pins ..... 25 mA
Maximum output current sunk by any PORTD, PORTE and PORTJ I/O pins ..... 8 mA
Maximum output current sunk by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins ..... 2 mA
Maximum output current sourced by PORTA<7:6> and any PORTB and PORTC I/O pins ..... 25 mA
Maximum output current sourced by any PORTD, PORTE and PORTJ I/O pins ..... 8 mA
Maximum output current sourced by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins ..... 2 mA
Maximum current sunk by all ports combined ..... 200 mA

Note 1: Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 31-10: CAPTURE/COMPARE/PWM TIMINGS (ECCP1, ECCP2 MODULES)



Note: Refer to Figure 31-3 for load conditions.

TABLE 31-13: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP1, ECCP2 MODULES)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
51	TccH	CCPx Input High Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
52	TccP	CCPx Input Period		$\frac{3\ T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		—	25	ns	
54	TccF	CCPx Output Fall Time		—	25	ns	

© 2009-2011 Microchip Technology Inc.