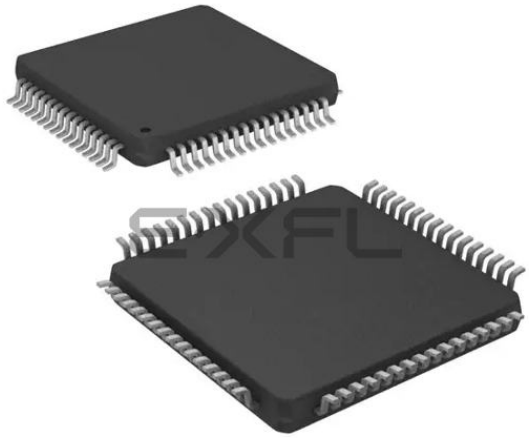

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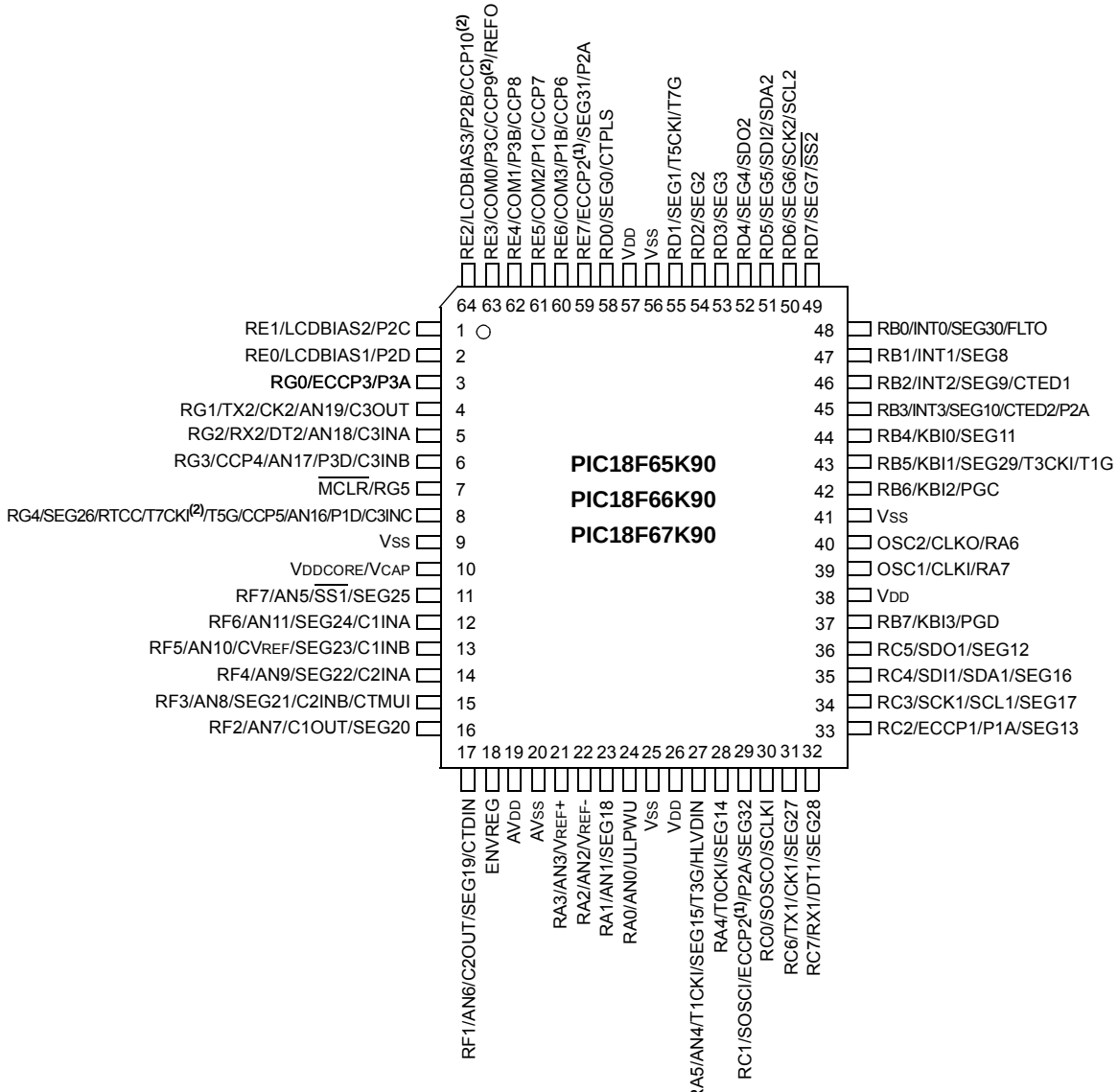
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f67k90-i-ptrsl

Pin Diagrams – PIC18F6XK90

64-Pin QFN(3), TQFP



Note 1: The ECCP2 pin placement depends on the CCP2MX Configuration bit setting.

2: Not available on the PIC18F65K90 and PIC18F85K90.

3: For the QFN package, it is recommended that the bottom pad be connected to VSS.

TABLE 1-3: PIC18F6XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	QFN/TQFP			
				PORTE is a bidirectional I/O port.
RE0/LCDBIAS1/P2D	2			
RE0		I/O	ST	Digital I/O.
LCDBIAS1		I	Analog	BIAS1 input for LCD.
P2D		O	—	EECP2 PWM Output D.
RE1/LCDBIAS2/P2C	1			
RE1		I/O	ST	Digital I/O.
LCDBIAS2		I	Analog	BIAS2 input for LCD.
P2C		O	—	ECCP2 PWM Output C.
RE2/LCDBIAS3/P2B/CCP10	64			
RE2		I/O	ST	Digital I/O.
LCDBIAS3		I	Analog	BIAS3 input for LCD.
P2B		O	—	ECCP2 PWM Output B.
CCP10(3)		I/O	S/T	Capture 10 input/Compare 10 output/PWM10 output.
RE3/COM0/P3C/CCP9/REFO	63			
RE3		I/O	ST	Digital I/O.
COM0		O	Analog	COM0 output for LCD.
P3C		O	—	ECCP3 PWM Output C.
CCP9(3)		I/O	S/T	Capture 9 input/Compare 9 output/PWM9 output.
REFO		O	—	Reference clock out.
RE4/COM1/P3B/CCP8	62			
RE4		I/O	ST	Digital I/O.
COM1		O	Analog	COM1 output for LCD.
P3B		O	—	ECCP3 PWM Output B.
CCP8		I/O	S/T	Capture 8 input/Compare 8 output/PWM8 output.
RE5/COM2/P1C/CCP7	61			
RE5		I/O	ST	Digital I/O.
COM2		O	Analog	COM2 output for LCD.
P1C		O	—	ECCP1 PWM Output C.
CCP7		I/O	S/T	Capture 7 input/Compare 7 output/PWM7 output.
RE6/COM3/P1B/CCP6	60			
RE6		I/O	ST	Digital I/O.
COM3		O	Analog	COM3 output for LCD.
P1B		O	—	ECCP1 PWM Output B.
CCP6		I/O	S/T	Capture 6 input/Compare 6 output/PWM6 output.
RE7/ECCP2/SEG31/P2A	59			
RE7		I/O	ST	Digital I/O.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG31		O	Analog	SEG31 Output for LCD.
P2A		O	—	ECCP2 PWM Output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
ECCP1DEL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
CCPR1H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PIR5	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PIE5	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu(1)
IPR4	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
PIR4	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu(1)
PIE4	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
CVRCON	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
CMSTAT	PIC18F6XK90	PIC18F8XK90	111- ----	111- ----	uuu- ----
TMR3H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
T3CON	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0x00	0000 0x00
T3GCON	PIC18F6XK90	PIC18F8XK90	0000 0x00	0000 0x00	uuuu uuuu
SPBRG1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
RCREG1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TXREG1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TXSTA1	PIC18F6XK90	PIC18F8XK90	0000 0010	0000 0010	uuuu uuuu
RCSTA1	PIC18F6XK90	PIC18F8XK90	0000 000x	0000 000x	uuuu uuuu
T1GCON	PIC18F6XK90	PIC18F8XK90	0000 0x00	0000 0x00	uuuu uuuu
IPR6	PIC18F6XK90	PIC18F8XK90	---1 -111	---1 -111	---u -uuu
HLVDCON	PIC18F6XK90	PIC18F8XK90	0000 0101	0000 0101	uuuu uuuu
PIR6	PIC18F6XK90	PIC18F8XK90	---0 -000	---0 -000	---u -uuu
IPR3	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
PIR3	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PIE3	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
IPR2	PIC18F6XK90	PIC18F8XK90	1-11 1111	1-11 1111	u-uu uuuu
PIR2	PIC18F6XK90	PIC18F8XK90	0-00 0000	0-00 0000	u-uu uuuu
PIE2	PIC18F6XK90	PIC18F8XK90	0-00 0000	0-00 0000	u-uu uuuu
IPR1	PIC18F6XK90	PIC18F8XK90	-111 1111	-111 1111	-uuu uuuu
PIR1	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
PIE1	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

REGISTER 8-1: EECON1: DATA EEPROM CONTROL REGISTER 1

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR(1)	WREN	WR	RD
bit 7							bit 0

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEPGD:** Flash Program or Data EEPROM Memory Select bit
1 = Access Flash program memory
0 = Access data EEPROM memory

bit 6 **CFGS:** Flash Program/Data EEPROM or Configuration Select bit
1 = Access Configuration registers
0 = Access Flash program or data EEPROM memory

bit 5 **Unimplemented:** Read as '0'

bit 4 **FREE:** Flash Row Erase Enable bit
1 = Erase the program memory row addressed by the TBLPTR on the next WR command (cleared by completion of an erase operation)
0 = Perform write-only

bit 3 **WRERR:** Flash Program/Data EEPROM Error Flag bit(1)
1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation or an improper write attempt)
0 = The write operation completed

bit 2 **WREN:** Flash Program/Data EEPROM Write Enable bit
1 = Allows write cycles to Flash program/data EEPROM
0 = Inhibits write cycles to Flash program/data EEPROM

bit 1 **WR:** Write-Control bit
1 = Initiates a data EEPROM erase/write cycle, or a program memory erase cycle or write cycle (The operation is self-timed and the bit is cleared by hardware once the write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. The RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
0 = Does not initiate an EEPROM read

Note 1: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

TABLE 11-16: PORTH FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RH0/SEG47/ AN23	RH0	0	O	DIG	LATH<0> data output.
		1	I	ST	PORTH<0> data input.
	SEG47	1	O	ANA	LCD Segment 47 output; disables all other pin functions.
	AN23	1	I	ANA	A/D Input Channel 23. Default input configuration on POR; does not affect digital input.
RH1/SEG46/ AN22	RH1	0	O	DIG	LATH<1> data output.
		1	I	ST	PORTH<1> data input.
	SEG46	1	O	ANA	LCD Segment 46 output; disables all other pin functions.
	AN22	1	I	ANA	A/D Input Channel 22. Default input configuration on POR; does not affect digital input.
RH2/SEG45/ AN21	RH2	0	O	DIG	LATH<2> data output.
		1	I	ST	PORTH<2> data input.
	SEG45	1	O	ANA	LCD Segment 45 output; disables all other pin functions.
	AN21	1	I	ANA	A/D Input Channel 21. Default input configuration on POR; does not affect digital input.
RH3/SEG44/ AN20	RH3	0	O	DIG	LATH<3> data output.
		1	I	ST	PORTH<3> data input.
	SEG44	1	O	ANA	LCD Segment 44 output; disables all other pin functions.
	AN20	1	I	ANA	A/D Input Channel 20. Default input configuration on POR; does not affect digital input.
RH4/SEG40/ CCP9/P3C/ AN12/C2INC	RH4	0	O	DIG	LATH<4> data output.
		1	I	ST	PORTH<4> data input.
	SEG40	1	O	ANA	LCD Segment 40 output; disables all other pin functions.
	CCP9	0	O	DIG	CCP9 compare/PWM output; takes priority over port data.
		1	I	ST	CCP9 capture input.
	P3C	0	O	—	ECCP3 PWM Output C. May be configured for tri-state during Enhanced PWM.
	AN12	1	I	ANA	A/D Input Channel 12. Default input configuration on POR; does not affect digital input.
	C2INC	x	I	ANA	Comparator 2 Input C.
RH5/SEG41/ CCP8/P3B/ AN13/C2IND	RH5	0	O	DIG	LATH<5> data output.
		1	I	ST	PORTH<5> data input.
	SEG41	1	O	ANA	LCD Segment 41 output; disables all other pin functions.
	CCP8	0	O	DIG	CCP8 compare/PWM output; takes priority over port data.
		1	I	ST	CCP8 capture input.
	P3B	0	O	—	ECCP3 PWM Output B. May be configured for tri-state during Enhanced PWM.
	AN13	1	I	ANA	A/D Input Channel 13. Default input configuration on POR; does not affect digital input.
	C2IND	x	I	ANA	Comparator 2 Input D.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 11-18: PORTJ FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RJ0	RJ0	0	O	DIG	LATJ<0> data output.
		1	I	ST	PORTJ<0> data input.
RJ1/SEG33	RJ1	0	O	DIG	LATJ<1> data output.
		1	I	ST	PORTJ<1> data input.
	SEG33	1	O	ANA	LCD Segment 33 output; disables all other pin functions.
RJ2/SEG34	RJ2	0	O	DIG	LATJ<2> data output.
		1	I	ST	PORTJ<2> data input.
	SEG34	1	O	ANA	LCD Segment 34 output; disables all other pin functions.
RJ3/SEG35	RJ3	0	O	DIG	LATJ<3> data output.
		1	I	ST	PORTJ<3> data input.
	SEG35	1	O	ANA	LCD Segment 35 output; disables all other pin functions.
RJ4/SEG39	RJ4	0	O	DIG	LATJ<4> data output.
		1	I	ST	PORTJ<4> data input.
	SEG39	1	O	ANA	LCD Segment 39 output; disables all other pin functions.
RJ5/SEG38	RJ5	0	O	DIG	LATJ<5> data output.
		1	I	ST	PORTJ<5> data input.
	SEG38	1	O	ANA	LCD Segment 38 output; disables all other pin functions.
RJ6/SEG37	RJ6	0	O	DIG	LATJ<6> data output.
		1	I	ST	PORTJ<6> data input.
	SEG37	1	O	ANA	LCD Segment 37 output; disables all other pin functions.
RJ7/SEG36	RJ7	0	O	DIG	LATJ<7> data output.
		1	I	ST	PORTJ<7> data input.
	SEG36	1	O	ANA	LCD Segment 36 output; disables all other pin functions.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 11-19: SUMMARY OF REGISTERS ASSOCIATED WITH PORTJ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTJ	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	78
LATJ	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0	78
TRISJ	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0	78
LCDSE4	SE39	SE38	SE37	SE36	SE35	SE34	SE33	SE32	83
PADCFG1	RDPU	REPU	RJPU(1)	—	—	RTSECSEL1	RTSECSEL0	—	80

Legend: Shaded cells are not used by PORTJ.

Note 1: Unimplemented in PIC18F6XK90 devices, read as '0'.

12.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable. Its value is set by the PSA and T0PS<2:0> bits (T0CON<3:0>), which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256, in power-of-two increments, are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (for example, `CLRF TMR0`, `MOVWF TMR0`, `BSF TMR0`) clear the prescaler count.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment.

12.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed “on-the-fly” during program execution.

12.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before re-enabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine (ISR).

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

TABLE 12-1: REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
TMR0L	Timer0 Register Low Byte								76
TMR0H	Timer0 Register High Byte								76
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	76

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by Timer0.

17.1 RTCC MODULE REGISTERS

The RTCC module registers are divided into the following categories:

RTCC Control Registers

- RTCCFG
- RTCCAL
- PADCFG1
- ALRMCFG
- ALRMRPT

RTCC Value Registers

- RTCVALH
- RTCVALL

  Both registers access the following registers:
  - YEAR
  - MONTH
  - DAY
  - WEEKDAY
  - HOUR
  - MINUTE
  - SECOND

Alarm Value Registers

- ALRMVALH
- ALRMVALL

  Both registers access the following registers:
  - ALRMMNTH
  - ALRMDAY
  - ALRMWD
  - ALRMHR
  - ALRMMIN
  - ALRMSEC

Note:	The RTCVALH and RTCVALL registers can be accessed through RTCRPT<1:0> (RTCCFG<1:0>). ALRMVALH and ALRMVALL can be accessed through ALRMPTR<1:0> (ALRMCFG<1:0>).

18.0 CAPTURE/COMPARE/PWM (CCP) MODULES

PIC18F87K90 family devices have seven CCP (Capture/Compare/PWM) modules, designated CCP4 through CCP10. All the modules implement standard Capture, Compare and Pulse-Width Modulation (PWM) modes.

Note:	Throughout this section, generic references are used for register and bit names that are the same, except for an 'x' variable that indicates the item's association with the specific CCP module. For example, the control register is named CCPxCON and refers to CCP4CON through CCP10CON.

Each CCP module contains a 16-bit register that can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register. For the sake of clarity, all CCP module operation in the following sections is described with respect to CCP4, but is equally applicable to CCP5 through CCP10.

Note:	The CCP9 and CCP10 modules are disabled on the devices with 32 Kbytes of program memory (PIC18FX5K90).

REGISTER 18-1: CCPxCON: CCPx CONTROL REGISTER (CCP4-CCP10 MODULES)(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle for CCPx Module bits (bit 1, bit 0)

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: CCPx Module Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0001 = Reserved
0010 = Compare mode: toggle output on match (CCPxIF bit is set)
0011 = Reserved
0100 = Capture mode: every falling edge
0101 = Capture mode: every rising edge
0110 = Capture mode: every 4th rising edge
0111 = Capture mode: every 16th rising edge
1000 = Compare mode: initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)
1001 = Compare mode: initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)
1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)
1011 = Compare mode: Special Event Trigger; reset timer on CCPx match (CCPxIF bit is set)(2)
11xx = PWM mode

Note 1: The CCP9 and CCP10 modules are not available on devices with 32 Kbytes of program memory (PIC18FX5K90).

2: CCPxM<3:0> = 1011 will only reset the timer and not start the A/D conversion on a CCPx match.

REGISTER 19-1: CCPxCON: ENHANCED CAPTURE/COMPARE/PWM x CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxM1	PxM0	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PxM<1:0>:** Enhanced PWM Output Configuration bits

If CCPxM<3:2> = 00, 01, 10:

xx = PxA is assigned as a capture/compare input/output; PxB, PxC and PxD are assigned as PORT pins

If CCPxM<3:2> = 11:

00 = Single output: PxA, PxB, PxC and PxD are controlled by steering (see **Section 19.4.7 "Pulse Steering Mode"**)

01 = Full-bridge output forward: PxD is modulated; PxA is active; PxB, PxC are inactive

10 = Half-bridge output: PxA, PxB are modulated with dead-band control; PxC and PxD are assigned as PORT pins

11 = Full-bridge output reverse: PxB is modulated; PxC is active; PxA and PxD are inactive

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle Bit 1 and Bit 0

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: ECCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCPx module)

0001 = Reserved

0010 = Compare mode: toggle output on match

0011 = Capture mode

0100 = Capture mode: every falling edge

0101 = Capture mode: every rising edge

0110 = Capture mode: every fourth rising edge

0111 = Capture mode: every 16th rising edge

1000 = Compare mode: initialize the ECCPx pin low; set the output on a compare match (set CCPxIF)

1001 = Compare mode: initialize the ECCPx pin high; clear the output on a compare match (set CCPxIF)

1010 = Compare mode: generate a software interrupt only; ECCPx pin reverts to an I/O state

1011 = Compare mode: trigger special event (ECCPx resets TMR1 or TMR3, starts A/D conversion, sets CCxIF bit)

1100 = PWM mode: PxA and PxC are active-high; PxB and PxD are active-high

1101 = PWM mode: PxA and PxC are active-high; PxB and PxD are active-low

1110 = PWM mode: PxA and PxC are active-low; PxB and PxD are active-high

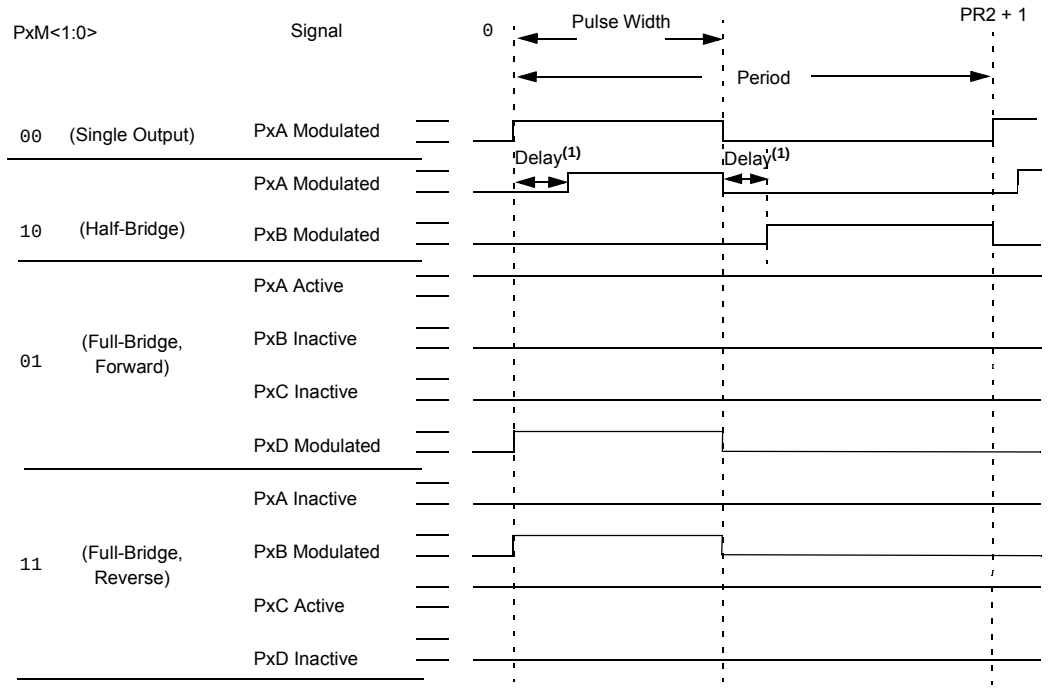
1111 = PWM mode: PxA and PxC are active-low; PxB and PxD are active-low

TABLE 19-3: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	PxM<1:0>	PxA	PxB	PxC	PxD
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: Outputs are enabled by pulse steering in Single mode (see Register 19-5).

FIGURE 19-4: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:

- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (ECCPxDEL<6:0>)

Note 1: Dead-band delay is programmed using the ECCPxDEL register (see **Section 19.4.6 "Programmable Dead-Band Delay Mode"**).

20.3.2.3 Internal Reference

Under firmware control, an internal reference for the LCD bias voltages can be enabled. When enabled, the source of this voltage can be VDD.

When no internal reference is selected, the LCD contrast control circuit is disabled and LCD bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

20.3.2.4 VLCDx Pins

The VLCD3, VLCD2 and VLCD1 pins provide the ability for an external LCD bias network to be used instead of the internal ladder. Use of the VLCDx pins does not prevent use of the internal ladder.

Each VLCD pin has an independent control in the LCDREF register, allowing access to any or all of the LCD bias signals.

This architecture allows for maximum flexibility in different applications. The VLCDx pins could be used to add capacitors to the internal reference ladder for increasing the drive capacity. For applications where the internal contrast control is insufficient, the firmware can choose to enable only the VLCD3 pin, allowing an external contrast control circuit to use the internal reference divider.

20.4 LCD Multiplex Types

The LCD driver module can be configured into four multiplex types:

- Static (only COM0 used)
- 1/2 multiplex (COM0 and COM1 are used)
- 1/3 multiplex (COM0, COM1 and COM2 are used)
- 1/4 multiplex (COM0, COM1, COM2 and COM3 are used)

The LMUX<1:0> setting (LCDCON<1:0>) decides the function of the PORTE<6:4> bits. (For details, see Table 20-4.)

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

Note:	On a Power-on Reset, the LMUX<1:0> bits are '00'.

TABLE 20-4: PORTE<6:4> FUNCTION

LMUX<1:0>	PORTE<6>	PORTE<5>	PORTE<4>
00	Digital I/O	Digital I/O	Digital I/O
01	Digital I/O	Digital I/O	COM1 Driver
10	Digital I/O	COM2 Driver	COM1 Driver
11	COM3 Driver	COM2 Driver	COM1 Driver

20.5 Segment Enables

The LCDSEx registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or a digital only pin. To configure the pin as a segment pin, the corresponding bits in the LCDSEx registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEx registers overrides any bit settings in the corresponding TRIS register.

Note:	On a Power-on Reset, these pins are configured as digital I/O.

20.6 Pixel Control

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel.

Table 20-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

20.10 Operation During Sleep

The LCD module can operate during Sleep. Setting the SLPEN bit (LCDCON<6>) allows the LCD module to go to Sleep. Clearing this bit allows the module to continue operating during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 20-19 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after an LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. For the formulas to calculate the delay, see **Section 20.9 "LCD Interrupts"**.

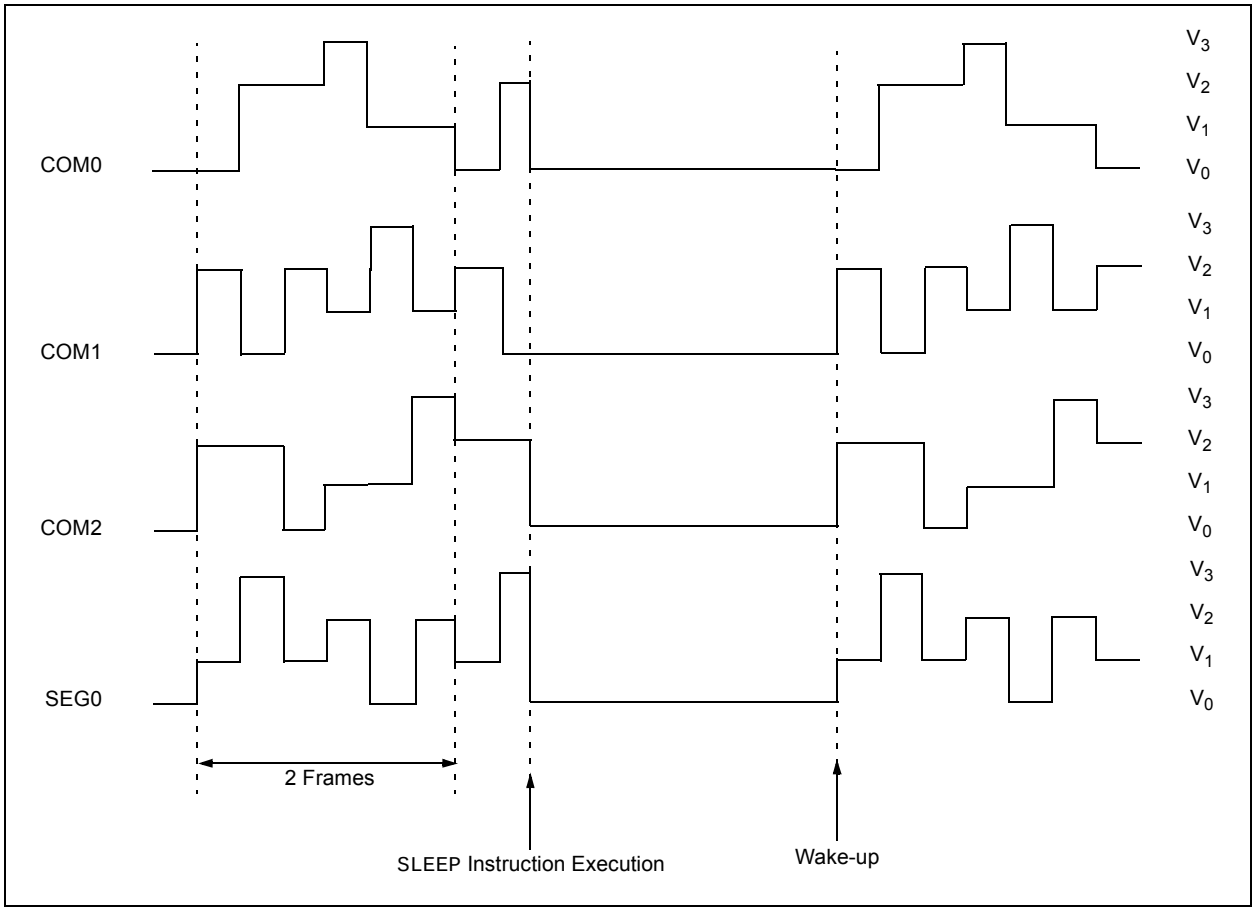
If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. The LCD data cannot be changed.

To allow the module to continue operation while in Sleep, the clock source must be either the internal RC oscillator or Timer1 external oscillator.

If the system clock is selected and the module is programmed to not Sleep, the module will ignore the SLPEN bit and stop operation immediately. The minimum LCD voltage then will be driven onto the segments and commons.

Note:	The internal RC oscillator or external SOSC oscillator must be used to operate the LCD module during Sleep.

FIGURE 20-19: SLEEP ENTRY/EXIT WHEN SLPEN = 1 OR CS<1:0> = 00



REGISTER 21-2: SSPxCON1: MSSPx CONTROL REGISTER 1 (SPI MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV(1)	SSPEN(2)	CKP	SSPM3(3)	SSPM2(3)	SSPM1(3)	SSPM0(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL:** Write Collision Detect bit
- 1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
- 0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)

SPI Slave mode:
- 1 = A new byte is received while the SSPxBUF register is still holding the previous data. In case of overflow, the data in SSPxSR is lost. Overflow can only occur in Slave mode. The user must read the SSPxBUF, even if only transmitting data, to avoid setting overflow (must be cleared in software).
- 0 = No overflow

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(2)
- 1 = Enables serial port and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
- 0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit
- 1 = Idle state for clock is a high level
- 0 = Idle state for clock is a low level

bit 3-0 **SSPM<3:0>:** Master Synchronous Serial Port Mode Select bits(3)
- 1010 = SPI Master mode: Clock = FOSC/8
- 0101 = SPI Slave mode: Clock = SCKx pin; $\overline{SSx}$ pin control is disabled; $\overline{SSx}$ can be used as an I/O pin
- 0100 = SPI Slave mode: Clock = SCKx pin; $\overline{SSx}$ pin control is enabled
- 0011 = SPI Master mode: Clock = TMR2 Output/2
- 0010 = SPI Master mode: Clock = FOSC/64
- 0001 = SPI Master mode: Clock = FOSC/16
- 0000 = SPI Master mode: Clock = FOSC/4

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.

2: When enabled, these pins must be properly configured as inputs or outputs.

3: Bit combinations not specifically listed here are either reserved or implemented in I^2C™ mode only.

21.3.9 OPERATION IN POWER-MANAGED MODES

In SPI Master mode, module clocks may be operating at a different speed than when in full-power mode; in the case of the Sleep mode, all clocks are halted.

In Idle modes, a clock is provided to the peripherals. That clock can be from the primary clock source, the secondary clock (SOSC oscillator) or the INTOSC source. See **Section 3.3 "Clock Sources and Oscillator Switching"** for additional information.

In most cases, the speed that the master clocks SPI data is not important; however, this should be evaluated for each system.

If MSSP interrupts are enabled, they can wake the controller from Sleep mode, or one of the Idle modes, when the master completes sending data. If an exit from Sleep or Idle mode is not desired, MSSP interrupts should be disabled.

If the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in any power-managed mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set, and if enabled, will wake the device.

21.3.10 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

21.3.11 BUS MODE COMPATIBILITY

Table 21-1 shows the compatibility between the standard SPI modes and the states of the CKP and CKE control bits.

TABLE 21-1: SPI BUS MODES

Standard SPI Mode Terminology	Control Bits State	
	CKP	CKE
0, 0	0	1
0, 1	0	0
1, 0	1	1
1, 1	1	0

There is also an SMP bit which controls when the data is sampled.

21.3.12 SPI CLOCK SPEED AND MODULE INTERACTIONS

Because MSSP1 and MSSP2 are independent modules, they can operate simultaneously at different data rates. Setting the SSPM<3:0> bits of the SSPxCON1 register determines the rate for the corresponding module.

An exception is when both modules use Timer2 as a time base in Master mode. In this instance, any changes to the Timer2 module's operation will affect both MSSP modules equally. If different bit rates are required for each module, the user should select one of the other three time base options for one of the modules.

TABLE 23-2: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF	77
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE	77
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP	77
ADRESH	A/D Result Register High Byte								76
ADRESL	A/D Result Register Low Byte								76
ADCON0	—	CHS4	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	76
ADCON1	TRIGSEL1	TRIGSEL0	VCFG1	VCFG0	VNCFG	CHSN2	CHSN1	CHSN0	76
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	76
ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0	81
ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8	81
ANCON2	ANSEL23	ANSEL22	ANSEL21	ANSEL20	ANSEL19	ANSEL18	ANSEL17	ANSEL16	81
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	80
PORTA	RA7(2)	RA6(2)	RA5	RA4	RA3	RA2	RA1	RA0	78
TRISA	TRISA7(2)	TRISA6(2)	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	78
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	78
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	78
PORTG	—	—	RG5(3)	RG4	RG3	RG2	RG1	RG0	78
TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	78
PORTH(1)	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	78
TRISH(1)	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	78

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: This register is not implemented on 64-pin devices.

2: These bits are available only in certain oscillator modes, when the OSC2 Configuration bit = 0. If that Configuration bit is cleared, this signal is not implemented.

3: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.

TABLE 28-1: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	—	XINST	—	SOSCSEL1	SOSCSEL0	INTOSCSEL	—	$\overline{\text{RETEN}}$	-1-1 1--1
300001h	CONFIG1H	IESO	FCMEN	—	PLLCFG	FOSC3	FOSC2	FOSC1	FOSC0	0000 1000
300002h	CONFIG2L	—	BORPWR1	BORWPR0	BORV1	BORV0	BOREN1	BOREN0	$\overline{\text{PWRTEN}}$	-111 1111
300003h	CONFIG2H	—	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN1	WDTEN0	-111 1111
300004h	CONFIG3L	—	—	—	—	—	—	—	RTCOSC	---- ---1
300005h	CONFIG3H	MCLRE	—	—	—	MSSPMSK	—	ECCPMX(2)	CCP2MX	1--- 1-11
300006h	CONFIG4L	$\overline{\text{DEBUG}}$	—	—	BBSIZ0	—	—	—	STVREN	1--1 ---1
300008h	CONFIG5L	CP7(1)	CP6(1)	CP5(1)	CP4(1)	CP3	CP2	CP1	CP0	1111 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	WRT7(1)	WRT6(1)	WRT5(1)	WRT4(1)	WRT3	WRT2	WRT1	WRT0	1111 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	EBTR7(1)	EBTR6(1)	EBTR5(1)	EBTR4(1)	EBTR3	EBTR2	EBTR1	EBTR0	1111 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1(3)	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx
3FFFFFh	DEVID2(3)	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

Note 1: Implemented in the PIC18F67K90 and PIC18F87K90 devices.

2: Implemented in the 80-pin devices (PIC18F8XK90).

3: See Register 28-14 for DEVID1 values. DEVID registers are read-only and cannot be programmed by the user.

RRNCF **Rotate Right f (No Carry)**

Syntax: RRNCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<n>) → dest<n – 1>,
(f<0>) → dest<7>

Status Affected: N, Z

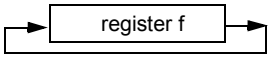
Encoding:

0100	00da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1:
```
RRNCF   REG, 1, 0
Before Instruction
    REG     =   1101 0111
After Instruction
    REG     =   1110 1011
```

Example 2:
```
RRNCF   REG, 0, 0
Before Instruction
    W       =   ?
    REG     =   1101 0111
After Instruction
    W       =   1110 1011
    REG     =   1101 0111
```

SETF **Set f**

Syntax: SETF f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: FFh → f

Status Affected: None

Encoding:

0110	100a	ffff	ffff

Description: The contents of the specified register are set to FFh.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example:
```
SETF    REG,1
Before Instruction
    REG     =   5Ah
After Instruction
    REG     =   FFh
```

D

E

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