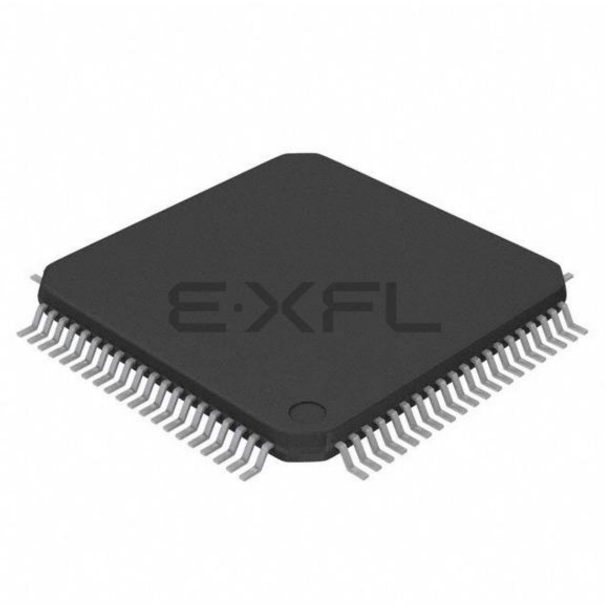

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f85k90-e-pt

TABLE 1-3: PIC18F6XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number QFN/TQFP	Pin Type	Buffer Type	Description
				PORTA is a bidirectional I/O port.
RA0/AN0/ULPWU	24			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog Input 0.
ULPWU		I	Analog	Ultra Low-Power Wake-up (ULPW) input.
RA1/AN1/SEG18	23			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog Input 1.
SEG18		O	Analog	SEG18 output for LCD.
RA2/AN2/VREF-	22			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog Input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
RA3/AN3/VREF+	21			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog Input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/SEG14	28			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
SEG14		O	Analog	SEG14 output for LCD.
RA5/AN4/SEG15/T1CKI/T3G/HLVDIN	27			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog Input 4.
SEG15		O	Analog	SEG15 output for LCD.
T1CKI		I	ST	Timer1 clock input.
T3G		I	ST	Timer3 external clock gate input.
HLVDIN		I	Analog	High/Low-Voltage Detect (HLVD) input.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I²C™ = I²C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.

TABLE 11-7: PORTD FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RD0/SEG0/ CTPLS	RD0	0	O	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	SEG0	1	O	ANA	LCD Segment 0 output; disables all other pin functions.
	CTPLS	x	O	DIG	CTMU pulse generator output.
RD1/SEG1/ T5CKI/T7G	RD1	0	O	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	SEG1	1	O	ANA	LCD Segment 1 output; disables all other pin functions.
	T5CKI	x	I	ST	Timer5 clock input.
	T7G	x	I	ST	Timer7 external clock gate input.
RD2/SEG2	RD2	0	O	DIG	LATD<2> data output.
		1	I	ST	PORTD<2> data input.
	SEG2	1	O	ANA	LCD Segment 2 output; disables all other pin functions.
RD3/SEG3	RD3	0	O	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	SEG3	1	O	ANA	LCD Segment 3 output; disables all other pin functions.
RD4/SEG4/ SDO2	RD4	0	O	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	SEG4	1	O	ANA	LCD Segment 4 output; disables all other pin functions.
	SDO2	0	P	DOG	SPI data output (MSSP module).
RD5/SEG5/ SDI2/SDA2	RD5	0	O	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input.
	SEG5	1	O	ANA	LCD Segment 5 output; disables all other pin functions.
	SDI2	1	I	ST	SPI data input (MSSP module).
	SDA2	0	O	I^2C	I^2C™ data input (MSSP module). Input type depends on module setting.
		1	I	ANA	LCD Segment 5 output; disables all other pin functions.
RD6/SEG6/ SCK2/SCL2	RD6	0	O	DIG	LATD<6> data output.
		1	I	ST	PORTD<6> data input.
	SEG6	1	O	ANA	LCD Segment 6 output; disables all other pin functions.
	SCK2	0	O	DIG	SPI clock output (MSSP module); takes priority over port data.
		1	I	ST	SPI clock input (MSSP module).
	SCL2	0	O	DIG	I^2C clock output (MSSP module); takes priority over port data.
		1	I	I^2C	I^2C clock input (MSSP module). Input type depends on module setting.
RD7/SEG7/ $\overline{SS2}$	RD7	0	O	DIG	LATD<7> data output.
		1	I	ST	PORTD<7> data input.
	SEG7	1	I	ANA	LCD Segment 7 output; disables all other pin functions.
	$\overline{SS2}$	1	I	TTL	Slave select input for MSSP module.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, I^2C = I^2C Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

13.8.3 TIMER1 GATE TOGGLE MODE

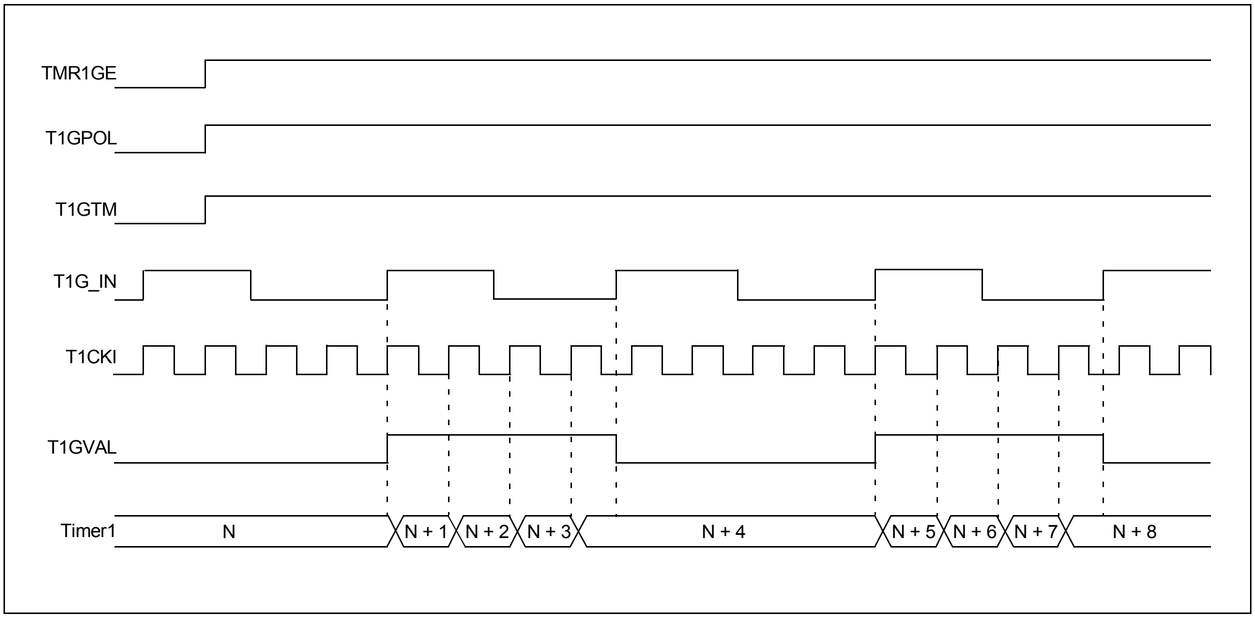
When Timer1 Gate Toggle mode is enabled, it is possible to measure the full cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. (For timing details, see Figure 13-5.)

The T1GVAL bit (T1GCON<2>) indicates when the Toggled mode is active and the timer is counting.

The Timer1 Gate Toggle mode is enabled by setting the T1GTM bit (T1GCON<5>). When T1GTM is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

FIGURE 13-5: TIMER1 GATE TOGGLE MODE



17.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

The key features of the Real-Time Clock and Calendar (RTCC) module are:

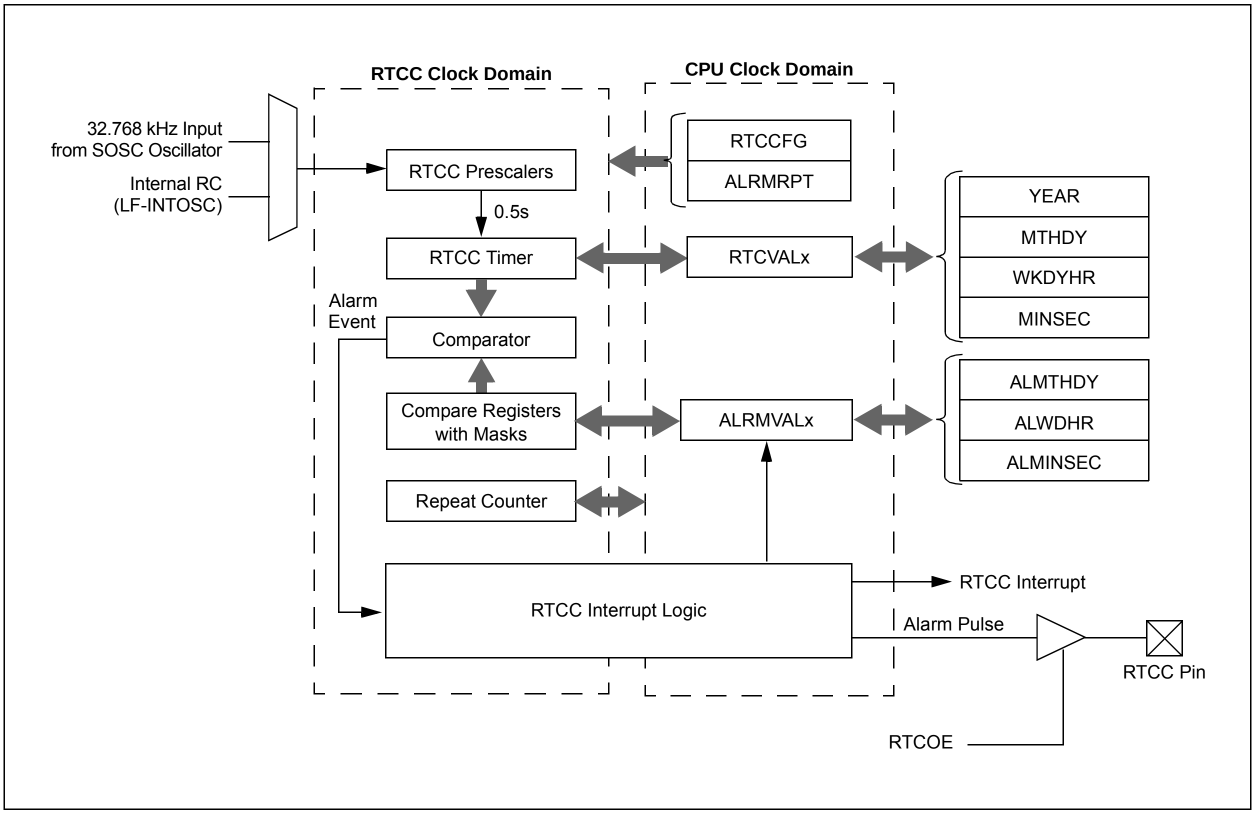
- Time: hours, minutes and seconds
- Twenty-four hour format (military time)
- Calendar: weekday, date, month and year
- Alarm configurable
- Year range: 2000 to 2099
- Leap year correction
- BCD format for compact firmware
- Optimized for low-power operation
- User calibration with auto-adjust
- Calibration range: ±2.64 seconds error per month
- Requirements: external 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

The RTCC module is intended for applications where accurate time must be maintained for an extended period with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery life while keeping track of time.

The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

Hours are measured in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

FIGURE 17-1: RTCC BLOCK DIAGRAM



NOTES:

REGISTER 18-4: CCPRxL: CCPx PERIOD LOW BYTE REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
CCPRxL7	CCPRxL6	CCPRxL5	CCPRxL4	CCPRxL3	CCPRxL2	CCPRxL1	CCPRxL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CCPRxL<7:0>:** CCPx Period Register Low Byte bits

Capture Mode:
Capture register low byte.

Compare Mode:
Compare register low byte.

PWM Mode:
Duty Cycle register low byte.

REGISTER 18-5: CCPRxH: CCPx PERIOD HIGH BYTE REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
CCPRxH7	CCPRxH6	CCPRxH5	CCPRxH4	CCPRxH3	CCPRxH2	CCPRxH1	CCPRxH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CCPRxH<7:0>:** CCPx Period Register High Byte bits

Capture Mode:
Capture register high byte.

Compare Mode:
Compare register high byte.

PWM Mode:
Duty Cycle Buffer register high byte.

REGISTER 19-1: CCPxCON: ENHANCED CAPTURE/COMPARE/PWM x CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxM1	PxM0	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PxM<1:0>:** Enhanced PWM Output Configuration bits

If CCPxM<3:2> = `00`, `01`, `10`:
`xx` = PxA is assigned as a capture/compare input/output; PxB, PxC and PxD are assigned as PORT pins

If CCPxM<3:2> = `11`:
`00` = Single output: PxA, PxB, PxC and PxD are controlled by steering (see **Section 19.4.7 "Pulse Steering Mode"**)
`01` = Full-bridge output forward: PxD is modulated; PxA is active; PxB, PxC are inactive
`10` = Half-bridge output: PxA, PxB are modulated with dead-band control; PxC and PxD are assigned as PORT pins
`11` = Full-bridge output reverse: PxB is modulated; PxC is active; PxA and PxD are inactive

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle Bit 1 and Bit 0

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: ECCPx Mode Select bits

`0000` = Capture/Compare/PWM off (resets ECCPx module)
`0001` = Reserved
`0010` = Compare mode: toggle output on match
`0011` = Capture mode
`0100` = Capture mode: every falling edge
`0101` = Capture mode: every rising edge
`0110` = Capture mode: every fourth rising edge
`0111` = Capture mode: every 16^{th} rising edge
`1000` = Compare mode: initialize the ECCPx pin low; set the output on a compare match (set CCPxIF)
`1001` = Compare mode: initialize the ECCPx pin high; clear the output on a compare match (set CCPxIF)
`1010` = Compare mode: generate a software interrupt only; ECCPx pin reverts to an I/O state
`1011` = Compare mode: trigger special event (ECCPx resets TMR1 or TMR3, starts A/D conversion, sets CCxIF bit)
`1100` = PWM mode: PxA and PxC are active-high; PxB and PxD are active-high
`1101` = PWM mode: PxA and PxC are active-high; PxB and PxD are active-low
`1110` = PWM mode: PxA and PxC are active-low; PxB and PxD are active-high
`1111` = PWM mode: PxA and PxC are active-low; PxB and PxD are active-low

20.1 LCD Registers

The LCD driver module has 32 registers:

- LCD Control Register (LCDCON)
- LCD Phase Register (LCDPS)
- LCD Reference Ladder Register (LCDRL)
- LCD Reference Voltage Control Register (LCDREF)
- Six LCD Segment Enable Registers (LCDSE5:LCDSE0)
- 24 LCD Data Registers (LCDDATA23:LCDDATA0)

The LCDCON register, shown in Register 20-1, controls the overall operation of the module. Once the module is configured, the LCDEN (LCDCON<7>) bit is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN (LCDCON<6>) bit.

The LCDPS register, shown in Register 20-2, configures the LCD clock source prescaler and the type of waveform, Type-A or Type-B. For details on these features, see **Section 20.2 “LCD Clock Source Selection”**, **Section 20.3 “LCD Bias Types”** and **Section 20.8 “LCD Waveform Generation”**.

REGISTER 20-1: LCDCON: LCD CONTROL REGISTER

R/W-0	R/W-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDEN	SLPEN	WERR	—	CS1	CS0	LMUX1	LMUX0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled

bit 6 **SLPEN:** LCD Driver Enable in Sleep mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode

bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register is written while WA (LCDPS<4>) = 0 (must be cleared in software)
0 = No LCD write error

bit 4 **Unimplemented:** Read as ‘0’

bit 3-2 **CS<1:0>:** Clock Source Select bits
00 = (FOSC/4)/8192
01 = SOSC oscillator/32
1x = INTRC (31.25 kHz)/32

bit 1-0 **LMUX<1:0>:** Commons Select bits

LMUX<1:0>	Multiplex	Maximum Number of Pixels (PIC18F6X90)	Maximum Number of Pixels (PIC18F8X90)	Bias
00	Static (COM0)	33	48	Static
01	1/2 (COM<1:0>)	66	96	1/2 or 1/3
10	1/3 (COM<2:0>)	99	144	1/2 or 1/3
11	1/4 (COM<3:0>)	132	192	1/3

REGISTER 21-6: SSPxCON2: MSSPx CONTROL REGISTER 2 (I^2C™ SLAVE MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ADMSK5	ADMSK4	ADMSK3	ADMSK2	ADMSK1	SEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **GCEN:** General Call Enable bit
1 = Enables interrupt when a general call address (0000h) is received in the SSPxSR
0 = General call address is disabled

bit 6 **ACKSTAT:** Acknowledge Status bit
Unused in Slave mode.

bit 5-2 **ADMSK<5:2>:** Slave Address Mask Select bits (5-Bit Address Masking mode)
1 = Masking of corresponding bits of SSPxADD is enabled
0 = Masking of corresponding bits of SSPxADD is disabled

bit 1 **ADMSK1:** Slave Address Least Significant bit(s) Mask Select bit
In 7-Bit Addressing mode:
1 = Masking of SSPxADD<1> only is enabled
0 = Masking of SSPxADD<1> only is disabled
In 10-Bit Addressing mode:
1 = Masking of SSPxADD<1:0> is enabled
0 = Masking of SSPxADD<1:0> is disabled

bit 0 **SEN:** Stretch Enable bit(1)
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: If the I^2C module is active, this bit may not be set (no spooling) and the SSPxBUF may not be written to (or writes to the SSPxBUF are disabled).

REGISTER 21-7: SSPxMSK: I^2C™ SLAVE ADDRESS MASK REGISTER (7-BIT MASKING MODE)(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **MSK<7:0>:** Slave Address Mask Select bit
1 = Masking of the corresponding bit of SSPxADD is enabled
0 = Masking of the corresponding bit of SSPxADD is disabled

Note 1: This register shares the same SFR address as SSPxADD and is only addressable in select MSSPx operating modes. See **Section 21.4.3.4 “7-Bit Address Masking Mode”** for more details.
2: MSK0 is not used as a mask bit in 7-bit addressing.

21.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDAx when SCLx goes from a low level to a high level.
b) SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD<6:0> and counts down to 0. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 21-31). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 21-32).

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 21-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

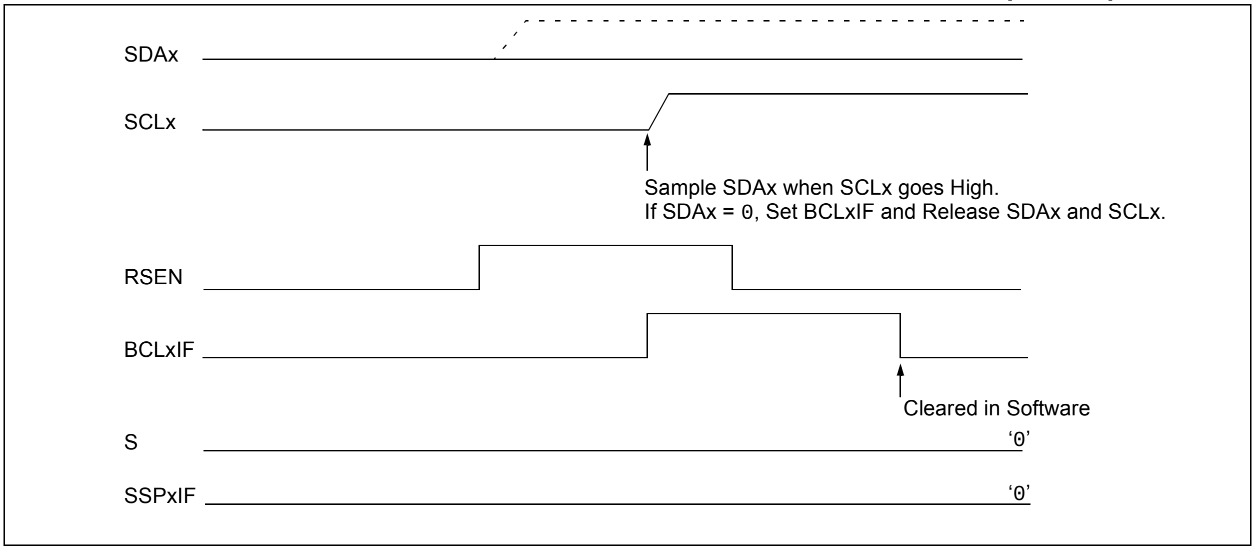
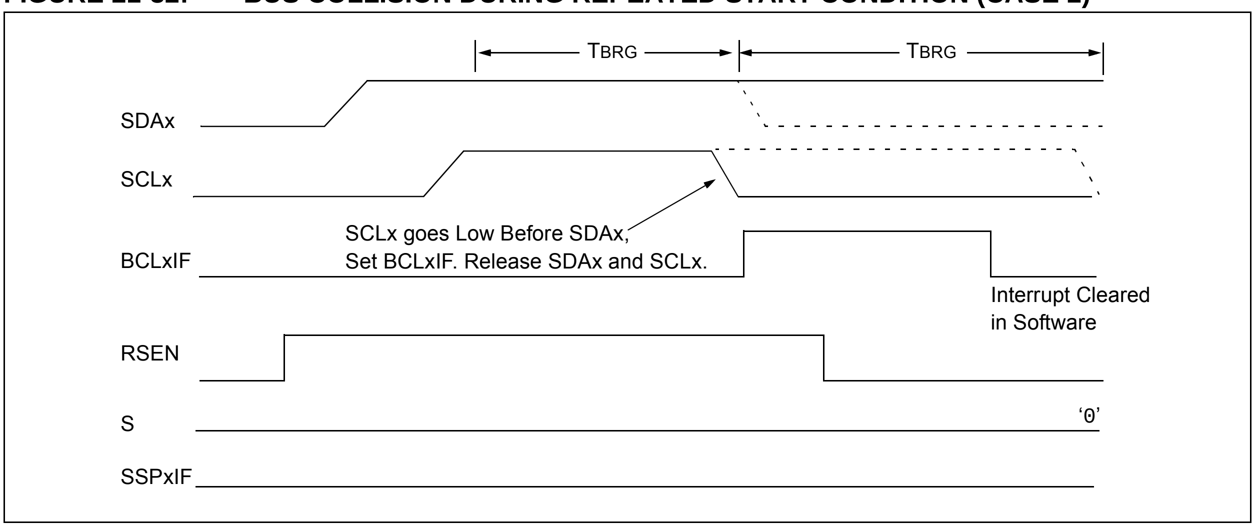


FIGURE 21-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



REGISTER 22-3: BAUDCONx: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF:** Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL:** Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP:** Data/Receive Polarity Select bit
Asynchronous mode:
1 = Receive data (RXx) is inverted (active-low)
0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
1 = Data (DTx) is inverted (active-low)
0 = Data (DTx) is not inverted (active-high)

bit 4 **TXCKP:** Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Idle state for transmit (TXx) is a low level
0 = Idle state for transmit (TXx) is a high level
Synchronous mode:
1 = Idle state for clock (CKx) is a high level
0 = Idle state for clock (CKx) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGHx and SPBRGx
0 = 8-bit Baud Rate Generator – SPBRGx only (Compatible mode), SPBRGHx value is ignored

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RXx pin – interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
0 = RXx pin is not monitored or the rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN:** Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement is disabled or completed
Synchronous mode:
Unused in this mode.

FIGURE 22-4: ASYNCHRONOUS TRANSMISSION

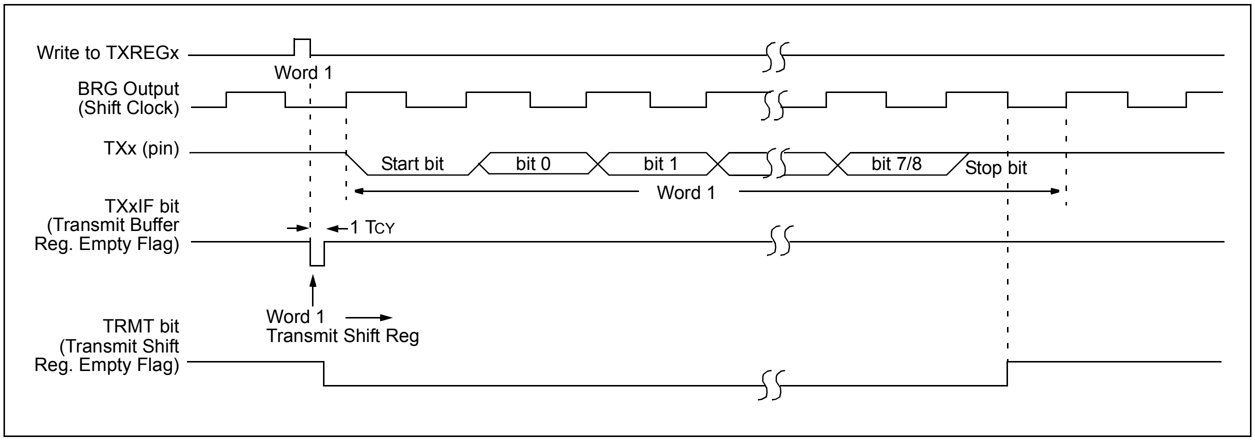
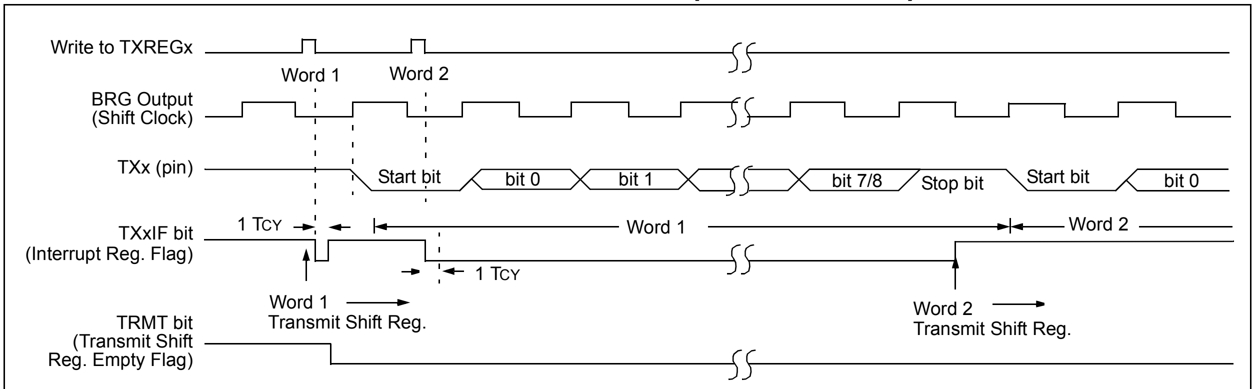


FIGURE 22-5: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

22.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTAx<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTAx<4>). In addition, enable bit, SPEN (RCSTAx<7>), is set in order to configure the TXx and RXx pins to CKx (clock) and DTx (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CKx line. Clock polarity is selected with the TXCKP bit (BAUDCONx<4>). Setting TXCKP sets the Idle state on CKx as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

22.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 22-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The TSR register obtains its data from the Read/Write Transmit Buffer register, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREGx (if available).

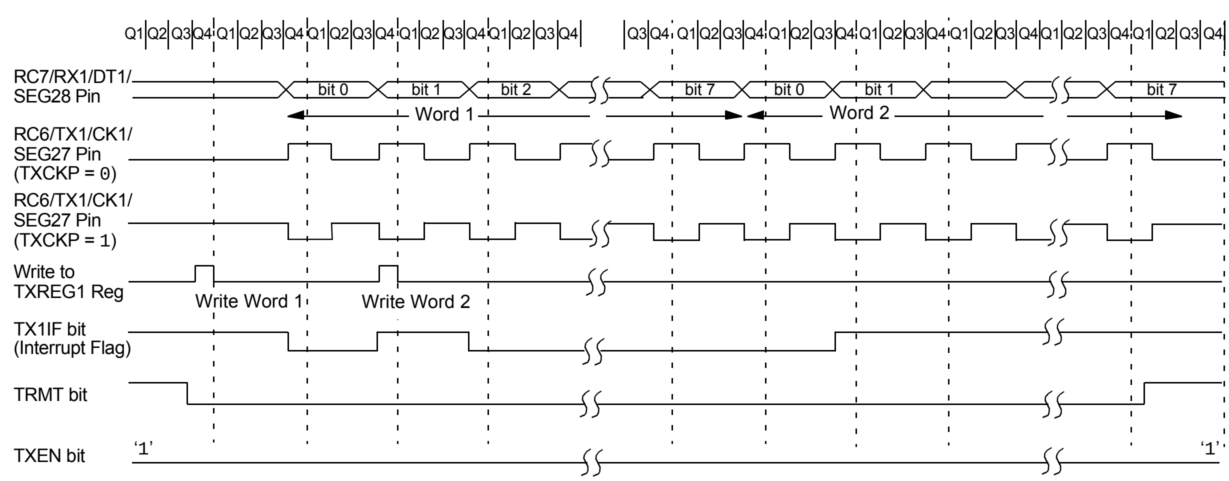
Once the TXREGx register transfers the data to the TSR register (occurs in one T_{CY}), the TXREGx is empty and the TXxIF flag bit is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXxIE. TXxIF is set regardless of the state of enable bit, TXxIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREGx register.

While flag bit, TXxIF, indicates the status of the TXREGx register, another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user must poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. If interrupts are desired, set enable bit, TXxIE.
4. If 9-bit transmission is desired, set bit, TX9.
5. Enable the transmission by setting bit, TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Start transmission by loading data to the TXREGx register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 22-11: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPBRGx = 0, continuous transmission of two 8-bit words. This example is equally applicable to EUSART2 (RG1/TX2/CK2/AN19/C3OUT and RG2/RX2/DT2/AN18/C3INA).

27.2 CTMU Operation

The CTMU works by using a fixed current source to charge a circuit. The type of circuit depends on the type of measurement being made.

In the case of charge measurement, the current is fixed and the amount of time the current is applied to the circuit is fixed. The amount of voltage read by the A/D becomes a measurement of the circuit's capacitance.

In the case of time measurement, the current, as well as the capacitance of the circuit, is fixed. In this case, the voltage read by the A/D is representative of the amount of time elapsed from the time the current source starts and stops charging the circuit.

If the CTMU is being used as a time delay, both capacitance and current source are fixed, as well as the voltage supplied to the comparator circuit. The delay of a signal is determined by the amount of time it takes the voltage to charge to the comparator threshold voltage.

27.2.1 THEORY OF OPERATION

The operation of the CTMU is based on the equation for charge:

$$C = I \bullet \frac{dV}{dT}$$

More simply, the amount of charge measured in coulombs in a circuit is defined as current in amperes (I) multiplied by the amount of time in seconds that the current flows (t). Charge is also defined as the capacitance in farads (C) multiplied by the voltage of the circuit (V). It follows that:

$$I \bullet t = C \bullet V$$

The CTMU module provides a constant, known current source. The A/D Converter is used to measure (V) in the equation, leaving two unknowns: capacitance (C) and time (t). The above equation can be used to calculate capacitance or time, by either the relationship using the known fixed capacitance of the circuit:

$$t = (C \bullet V)/I$$

or by:

$$C = (I \bullet t)/V$$

using a fixed time that the current source is applied to the circuit.

27.2.2 CURRENT SOURCE

At the heart of the CTMU is a precision current source, designed to provide a constant reference for measurements. The level of current is user-selectable across three ranges or a total of two orders of magnitude, with the ability to trim the output in ±2% increments (nominal). The current range is selected by the IRNG<1:0> bits (CTMUICON<1:0>), with a value of '`00`' representing the lowest range.

Current trim is provided by the ITRIM<5:0> bits (CTMUICON<7:2>). These six bits allow trimming of the current source in steps of approximately 2% per step. Half of the range adjusts the current source positively and the other half reduces the current source. A value of '`000000`' is the neutral position (no change). A value of '`100000`' is the maximum negative adjustment (approximately -62%) and '`011111`' is the maximum positive adjustment (approximately +62%).

27.2.3 EDGE SELECTION AND CONTROL

CTMU measurements are controlled by edge events occurring on the module's two input channels. Each channel, referred to as Edge 1 and Edge 2, can be configured to receive input pulses from one of the edge input pins (CTED1 and CTED2) or CCPx Special Event Triggers. The input channels are level-sensitive, responding to the instantaneous level on the channel rather than a transition between levels. The inputs are selected using the EDG1SEL and EDG2SEL bit pairs (CTMUCONL<3:2, 6:5>).

In addition to source, each channel can be configured for event polarity using the EDGE2POL and EDGE1POL bits (CTMUCONL<7,4>). The input channels can also be filtered for an edge event sequence (Edge 1 occurring before Edge 2) by setting the EDGSEQEN bit (CTMUCONH<2>).

27.2.4 EDGE STATUS

The CTMUCON register also contains two status bits, EDG2STAT and EDG1STAT (CTMUCONL<1:0>). Their primary function is to show if an edge response has occurred on the corresponding channel. The CTMU automatically sets a particular bit when an edge response is detected on its channel. The level-sensitive nature of the input channels also means that the status bits become set immediately if the channel's configuration is changed and matches the channel's current state.

The module uses the edge status bits to control the current source output to external analog modules (such as the A/D Converter). Current is only supplied to external modules when only one (not both) of the status bits is set. Current is shut off when both bits are either set or cleared. This allows the CTMU to measure current only during the interval between edges. After both status bits are set, it is necessary to clear them before another measurement is taken. Both bits should be cleared simultaneously, if possible, to avoid re-enabling the CTMU current source.

In addition to being set by the CTMU hardware, the edge status bits can also be set by software. This permits a user application to manually enable or disable the current source. Setting either (but not both) of the bits enables the current source. Setting or clearing both bits at once disables the source.

FIGURE 29-1: GENERAL FORMAT FOR INSTRUCTIONS

Example Instruction

Byte-oriented file register operations

15 10	9	8	7 0
OPCODE	d	a	f (FILE #)

`ADDWF MYREG, W, B`

d = `0` for result destination to be WREG register
d = `1` for result destination to be file register (f)
a = `0` to force Access Bank
a = `1` for BSR to select bank
f = 8-bit file register address

Byte to Byte move operations (2-word)

15 12	11 0
OPCODE	f (Source FILE #)
15 12	**11 0**
`1111`	f (Destination FILE #)

`MOVFF MYREG1, MYREG2`

f = 12-bit file register address

Bit-oriented file register operations

15 12	11 9	8	7 0
OPCODE	b (BIT #)	a	f (FILE #)

`BSF MYREG, bit, B`

b = 3-bit position of bit in file register (f)
a = `0` to force Access Bank
a = `1` for BSR to select bank
f = 8-bit file register address

Literal operations

15 8	7 0
OPCODE	k (literal)

`MOVLW 7Fh`

k = 8-bit immediate value

Control operations

`CALL`, `GOTO` and Branch operations

15 8	7 0
OPCODE	n<7:0> (literal)
15 12	**11 0**
`1111`	n<19:8> (literal)

`GOTO Label`

n = 20-bit immediate value

15 8		7 0
OPCODE	S	n<7:0> (literal)
15 12		**11 0**
`1111`		n<19:8> (literal)

`CALL MYFUNC`

S = Fast bit

15 11	10 0
OPCODE	n<10:0> (literal)

`BRA MYFUNC`

15 8	7 0
OPCODE	n<7:0> (literal)

`BC MYFUNC`

LFSR **Load FSR**

Syntax: LFSR f, k

Operands: $0 \le f \le 2$
$0 \le k \le 4095$

Operation: $k \rightarrow$ FSRf

Status Affected: None

Encoding:

`1110`	`1110`	`00ff`	k_{11}`kkk`
`1111`	`0000`	k_7`kkk`	`kkkk`

Description: The 12-bit literal ‘k’ is loaded into the file select register pointed to by ‘f’.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal ‘k’ MSB	Process Data	Write literal ‘k’ MSB to FSRfH
Decode	Read literal ‘k’ LSB	Process Data	Write literal ‘k’ to FSRfL

Example: `LFSR 2, 3ABh`

After Instruction
FSR2H = 03h
FSR2L = ABh

MOVF **Move f**

Syntax: MOVF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in$ [`0`,`1`]
$a \in$ [`0`,`1`]

Operation: $f \rightarrow$ dest

Status Affected: N, Z

Encoding:

`0101`	`00da`	`ffff`	`ffff`

Description: The contents of register ‘f’ are moved to a destination dependent upon the status of ‘d’. If ‘d’ is ‘`0`’, the result is placed in W. If ‘d’ is ‘`1`’, the result is placed back in register ‘f’. Location ‘f’ can be anywhere in the 256-byte bank.

If ‘a’ is ‘`0`’, the Access Bank is selected. If ‘a’ is ‘`1`’, the BSR is used to select the GPR bank.

If ‘a’ is ‘`0`’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write W

Example: `MOVF REG, 0, 0`

Before Instruction
REG = 22h
W = FFh
After Instruction
REG = 22h
W = 22h

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended) (Continued)

PIC18F87K90 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2,3)						
	All devices	3.7	8.5	μA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_RUN** mode, SOSCSEL = 01)
		5.4	10	μA	+25°C		
		6.6	13	μA	+85°C		
		13	30	μA	+125°C		
	All devices	8.7	18	μA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		10	20	μA	+25°C		
		12	23	μA	+85°C		
		25	60	μA	+125°C		
	All devices	60	160	μA	-40°C	VDD = 5V(5) Regulator Enabled	
		90	190	μA	+25°C		
		100	240	μA	+85°C		
		200	450	μA	+125°C		
	All devices	1.2	4	μA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_IDLE** mode, SOSCSEL = 01)
		1.7	5	μA	+25°C		
		2.6	6	μA	+85°C		
		9	20	μA	+125°C		
	All devices	1.6	7	μA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		2.8	9	μA	+25°C		
		4.1	10	μA	+85°C		
		17	40	μA	+125°C		
	All devices	60	150	μA	-40°C	VDD = 5V(5) Regulator Enabled	
		80	180	μA	+25°C		
		100	240	μA	+85°C		
		180	440	μA	+125°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

6: LCD glass is not connected; resistor current is not included.

7: 48 MHz maximum frequency at 125°C.

31.5.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 31-4: EXTERNAL CLOCK TIMING

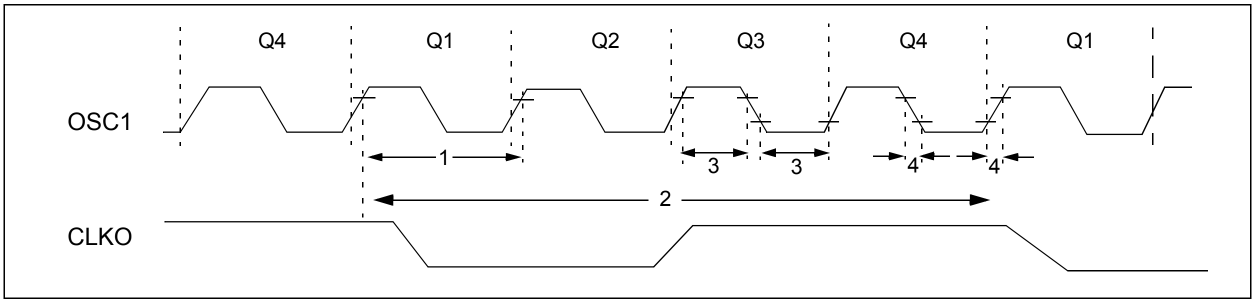


TABLE 31-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency(1)	DC	64	MHz	EC, ECIO Oscillator mode, -40°C ≤ TA ≤ +85°C
			DC	48	MHz	-40°C ≤ TA ≤ +125°C
		Oscillator Frequency(1)	DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	16	MHz	HS Oscillator mode
			4	16	MHz	HS + PLL Oscillator mode
			5	33	kHz	LP Oscillator mode
1	TOSC	External CLKIN Period(1)	15.6	—	ns	EC, ECIO Oscillator mode
		Oscillator Period(1)	250	—	ns	RC Oscillator mode
			250	10,000	ns	XT Oscillator mode
			40	250	ns	HS Oscillator mode
			62.5	250	ns	HS + PLL Oscillator mode
			5	200	μs	LP Oscillator mode
2	TCY	Instruction Cycle Time(1)	62.5	—	ns	TCY = 4/FOSC
3	TOSL, TOSH	External Clock in (OSC1) High or Low Time	30	—	ns	XT Oscillator mode
			2.5	—	μs	LP Oscillator mode
			10	—	ns	HS Oscillator mode
4	TOSR, TOSF	External Clock in (OSC1) Rise or Fall Time	—	20	ns	XT Oscillator mode
			—	50	ns	LP Oscillator mode
			—	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

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