Microchip Technology - PIC18F87K90-E/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f87k90-e-pt

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/SEG30/FLT0	58			
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External Interrupt 0.
SEG30		O	Analog	SEG30 output for LCD.
FLT0		I	ST	Enhanced PWM Fault input for ECCP1/2/3.
RB1/INT1/SEG8	57			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External Interrupt 1.
SEG8		O	Analog	SEG8 output for LCD.
RB2/INT2/SEG9/CTED1	56			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External Interrupt 2.
SEG9		O	Analog	SEG9 output for LCD.
CTED1		I	ST	CTMU Edge 1 input.
RB3/INT3/SEG10/ CTED2/ECCP2/P2A	55			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External Interrupt 3.
SEG10		O	Analog	SEG10 output for LCD.
CTED2		I	ST	CTMU Edge 2 input.
ECCP2		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A		O	ST	Enhanced PWM2 Output A.
RB4/KBI0/SEG11	54			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
SEG11		O	Analog	SEG11 output for LCD.
RB5/KBI1/SEG29/T3CKI/ T1G	53			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
SEG29		O	Analog	SEG29 output for LCD.
T3CKI		I	ST	Timer3 clock input.
T1G		I	ST	Timer1 external clock gate input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin, ENVREG, must always be connected directly to either a supply voltage or to ground. Tying ENVREG to VDD enables the regulator, while tying it to ground disables the regulator. Refer to **Section 28.3 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

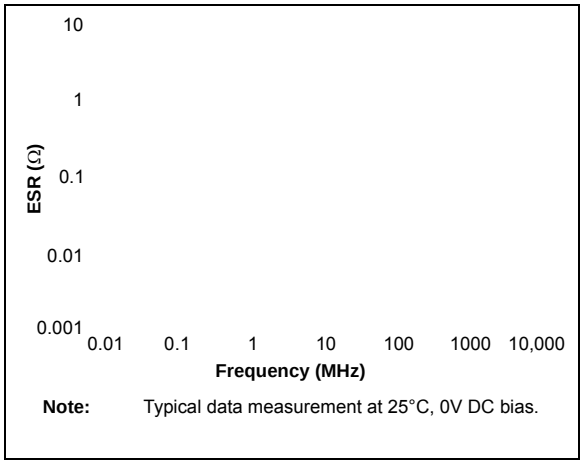
It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 31.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 31.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Some PIC18FXXKXX families, or some devices within a family, do not provide the option of enabling or disabling the on-chip voltage regulator:

- Some devices (with the name, PIC18**LF**XXKXX) permanently disable the voltage regulator.
  These devices do not have the ENVREG pin and require a 0.1 µF capacitor on the VCAP/VDDCORE pin. The VDD level of these devices must comply with the "voltage regulator disabled" specification for Parameter D001, in **Section 31.0 "Electrical Characteristics"**.
- Some devices permanently enable the voltage regulator.
  These devices also do not have the ENVREG pin. The 10 µF capacitor is still required on the VCAP/VDDCORE pin.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
EECON1	PIC18F6XK90	PIC18F8XK90	xx-0 x000	uu-0 u000	uu-u uuuu
EECON2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	0000 0000
LCDDATA23	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA22	PIC18F6XK90	PIC18F8XK90	---- ---x	---- ---u	---- ---u
LCDDATA22	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA21	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA20	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA19	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA18	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA17	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA16	PIC18F6XK90	PIC18F8XJ90	---- ---x	---- ---u	---- ---u
LCDDATA16	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA15	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA14	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA13	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA12	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA11	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA10	PIC18F6XK90	PIC18F8XK90	---- ---x	---- ---u	---- ---u
LCDDATA10	PIC18F6XK90	PIC18F8XJ90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA9	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA8	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA7	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA6	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA5	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA4	PIC18F6XK90	PIC18F8XJ90	---- ---x	---- ---u	---- ---u
LCDDATA4	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA3	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA2	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA1	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
LCDDATA0	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
BAUDCON1	PIC18F6XK90	PIC18F8XK90	0100 0-00	0100 0-00	uuuu u-uu
OSCCON2	PIC18F6XK90	PIC18F8XK90	-0-- 0-x0	-0-- 0-u0	-u-- u-uu
EEADRH	PIC18F6XK90	PIC18F8XK90	---- --00	---- --00	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
SPBRGH2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SPBRG2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
RCREG2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TXREG2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PSTR2CON	PIC18F6XK90	PIC18F8XK90	00-0 0001	00-0 0001	uu-u uuuu
PSTR3CON	PIC18F6XK90	PIC18F8XK90	00-0 0001	00-0 0001	uu-u uuuu
PMD0	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PMD1	PIC18F6XK90	PIC18F8XK90	-000 000-	-000 000-	-uuu uuu-
PMD2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PMD3	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TMR5H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR5L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
T5CON	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu uuuu
T5GCON	PIC18F6XK90	PIC18F8XK90	0000 0x00	0000 0x00	uuuu uuuu
CCPR4H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR4L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP4CON	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
CCPR5H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR5L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP5CON	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
CCPR6H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR6L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP6CON	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
CCPR7H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR7L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP7CON	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
TMR4	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR4	PIC18F6XK90	PIC18F8XK90	1111 1111	uuuu uuuu	uuuu uuuu
T4CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
SSP2BUF	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP2ADD	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SSP2STAT	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SSP2CON1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

REGISTER 17-9: DAY: DAY VALUE REGISTER(1)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 17-10: WEEKDAY: WEEKDAY VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

Note 1: A write to this register is only allowed when RTCWREN = 1.

19.0 ENHANCED CAPTURE/COMPARE/PWM (ECCP) MODULE

PIC18F87K90 family devices have three Enhanced Capture/Compare/PWM (ECCP) modules: ECCP1, ECCP2 and ECCP3. These modules contain a 16-bit register, which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register. These ECCP modules are upward compatible with CCP

Note:	Throughout this section, generic references are used for register and bit names that are the same, except for an 'x' variable that indicates the item's association with the ECCP1, ECCP2 or ECCP3 module. For example, the control register is named CCPxCON and refers to CCP1CON, CCP2CON and CCP3CON.

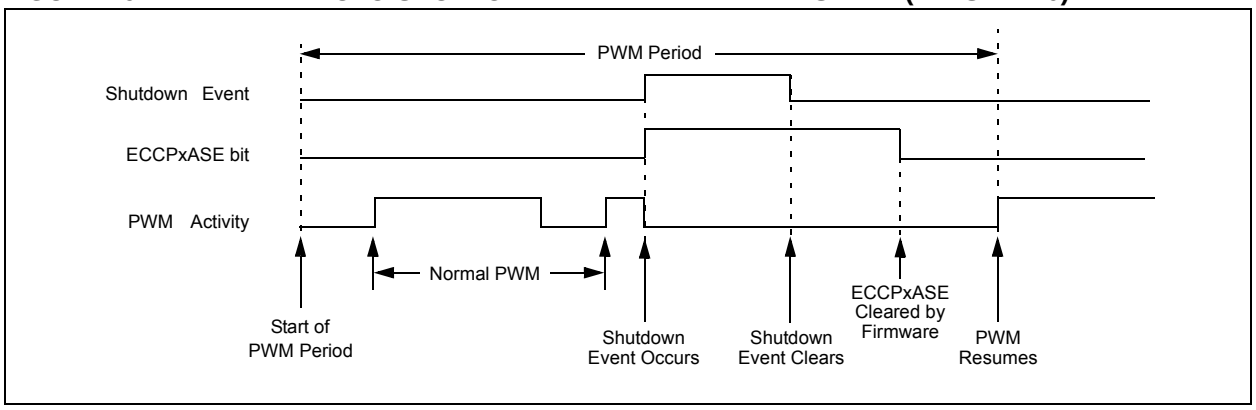
ECCP1, ECCP2 and ECCP3 are implemented as standard CCP modules with Enhanced PWM capabilities. These include:

- Provision for two or four output channels
- Output Steering modes
- Programmable polarity
- Programmable dead-band control
- Automatic shutdown and restart

The enhanced features are discussed in detail in **Section 19.4 "PWM (Enhanced Mode)"**.

The ECCP1, ECCP2 and ECCP3 modules use the control registers, CCP1CON, CCP2CON and CCP3CON. The control registers, CCP4CON through CCP10CON, are for the CCP4 through CCP10 modules.

FIGURE 19-12: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PxRSEN = 0)



19.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PxRSEN bit (ECCPxDEL<7>).

If auto-restart is enabled, the ECCPxASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPxASE bit will be cleared via hardware and normal operation will resume.

The module will wait until the next PWM period begins, however, before re-enabling the output pin. This behavior allows the auto-shutdown with auto-restart features to be used in applications based on current mode of PWM control.

FIGURE 19-13: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PxRSEN = 1)

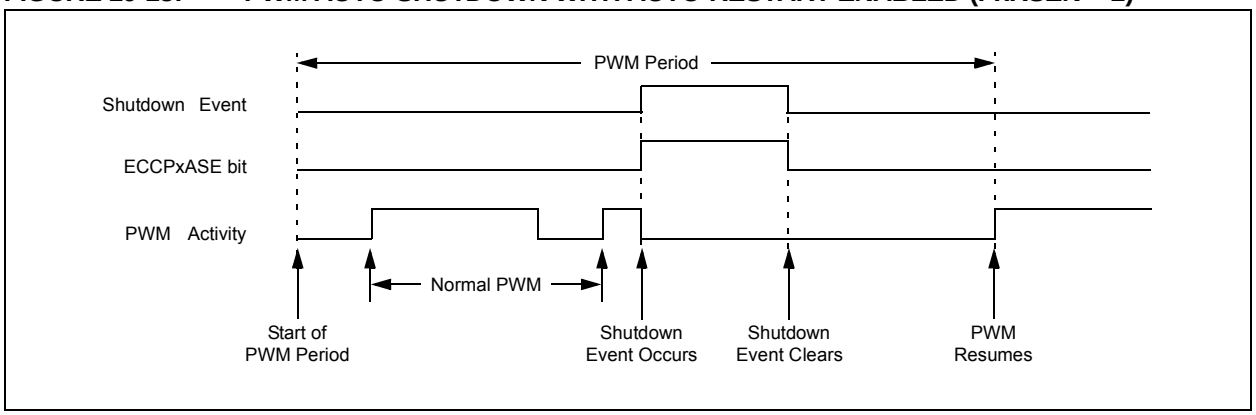


TABLE 20-2: LCDDATA REGISTERS AND BITS FOR SEGMENT AND COM COMBINATIONS

Segments	COM Lines			
	0	1	2	3
0 through 7	LCDDATA0	LCDDATA6	LCDDATA12	LCDDATA18
	S00C0:S07C0	S00C1:S07C1	S00C2:S07C2	S00C3:S07C3
8 through 15	LCDDATA1	LCDDATA7	LCDDATA13	LCDDATA19
	S08C0:S15C0	S08C1:S15C1	S08C2:S15C2	S08C0:S15C3
16 through 23	LCDDATA2	LCDDATA8	LCDDATA14	LCDDATA20
	S16C0:S23C0	S16C1:S23C1	S16C2:S23C2	S16C3:S23C3
24 through 31	LCDDATA3	LCDDATA9	LCDDATA15	LCDDATA21
	S24C0:S31C0	S24C1:S31C1	S24C2:S31C2	S24C3:S31C3
32 through 39	LCDDATA4(1)	LCDDATA10(1)	LCDDATA16(1)	LCDDATA22(1)
	S32C0:S39C0	S32C1:S39C1	S32C2:S39C2	S32C3:S39C3
40 through 47	LCDDATA5(2)	LCDDATA11(2)	LCDDATA17(2)	LCDDATA23(2)
	S40C0:S47C0	S40C1:S47C1	S40C2:S47C2	S40C3:S47C3

Note 1: Bits<7:1> of these registers are not implemented in PIC18F6XK90 devices. Bit 0 of these registers (SEG32Cy) is always implemented.

2: These registers are not implemented in PIC18F6XK90 devices.

REGISTER 20-6: LCDDATAx: LCD DATAx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n + 7)Cy	S(n + 6)Cy	S(n + 5)Cy	S(n + 4)Cy	S(n + 3)Cy	S(n + 2)Cy	S(n + 1)Cy	S(n)Cy
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **S(n + 7)Cy:S(n)Cy:** Pixel On bits

For registers, LCDDATA0 through LCDDATA5: n = (8x), y = 0

For registers, LCDDATA6 through LCDDATA11: n = (8(x – 6)), y = 1

For registers, LCDDATA12 through LCDDATA17: n = (8(x – 12)), y = 2

For registers, LCDDATA18 through LCDDATA23: n = (8(x – 18)), y = 3

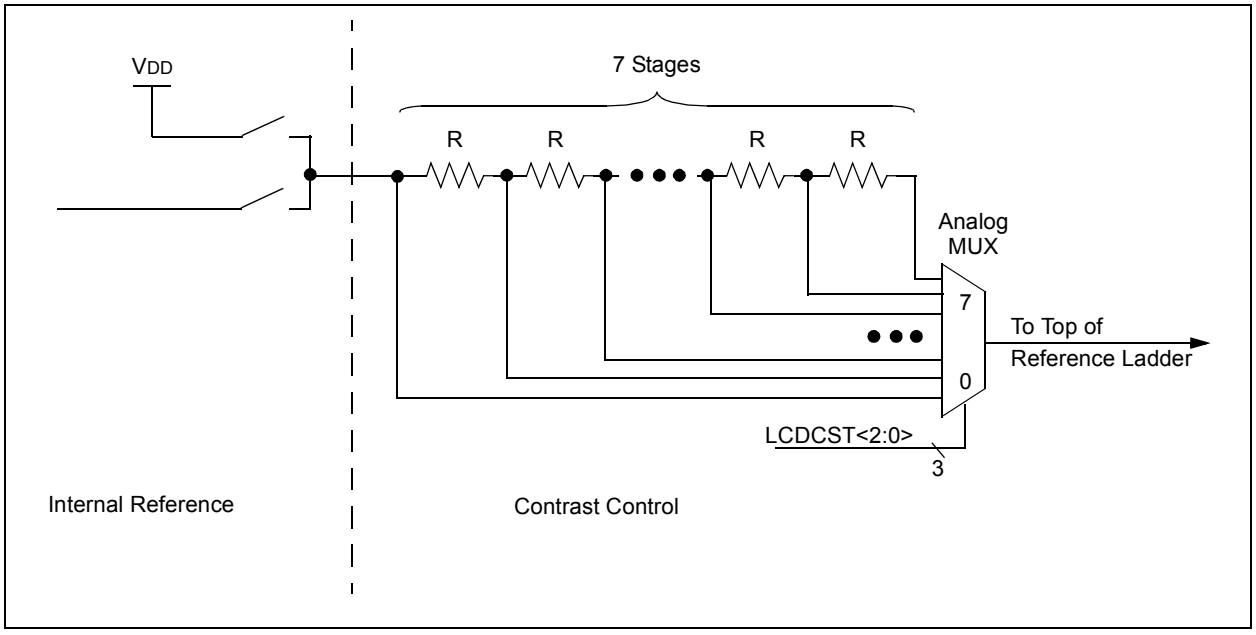
1 = Pixel on (dark)

0 = Pixel off (clear)

20.3.2.2 Contrast Control

The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCST bits (see Figure 20-6.).

FIGURE 20-6: INTERNAL REFERENCE AND CONTRAST CONTROL BLOCK DIAGRAM



20.10 Operation During Sleep

The LCD module can operate during Sleep. Setting the SLPEN bit (LCDCON<6>) allows the LCD module to go to Sleep. Clearing this bit allows the module to continue operating during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 20-19 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after an LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. For the formulas to calculate the delay, see **Section 20.9 "LCD Interrupts"**.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. The LCD data cannot be changed.

To allow the module to continue operation while in Sleep, the clock source must be either the internal RC oscillator or Timer1 external oscillator.

If the system clock is selected and the module is programmed to not Sleep, the module will ignore the SLPEN bit and stop operation immediately. The minimum LCD voltage then will be driven onto the segments and commons.

Note:	The internal RC oscillator or external SOSC oscillator must be used to operate the LCD module during Sleep.

FIGURE 20-19: SLEEP ENTRY/EXIT WHEN SLPEN = 1 OR CS<1:0> = 00

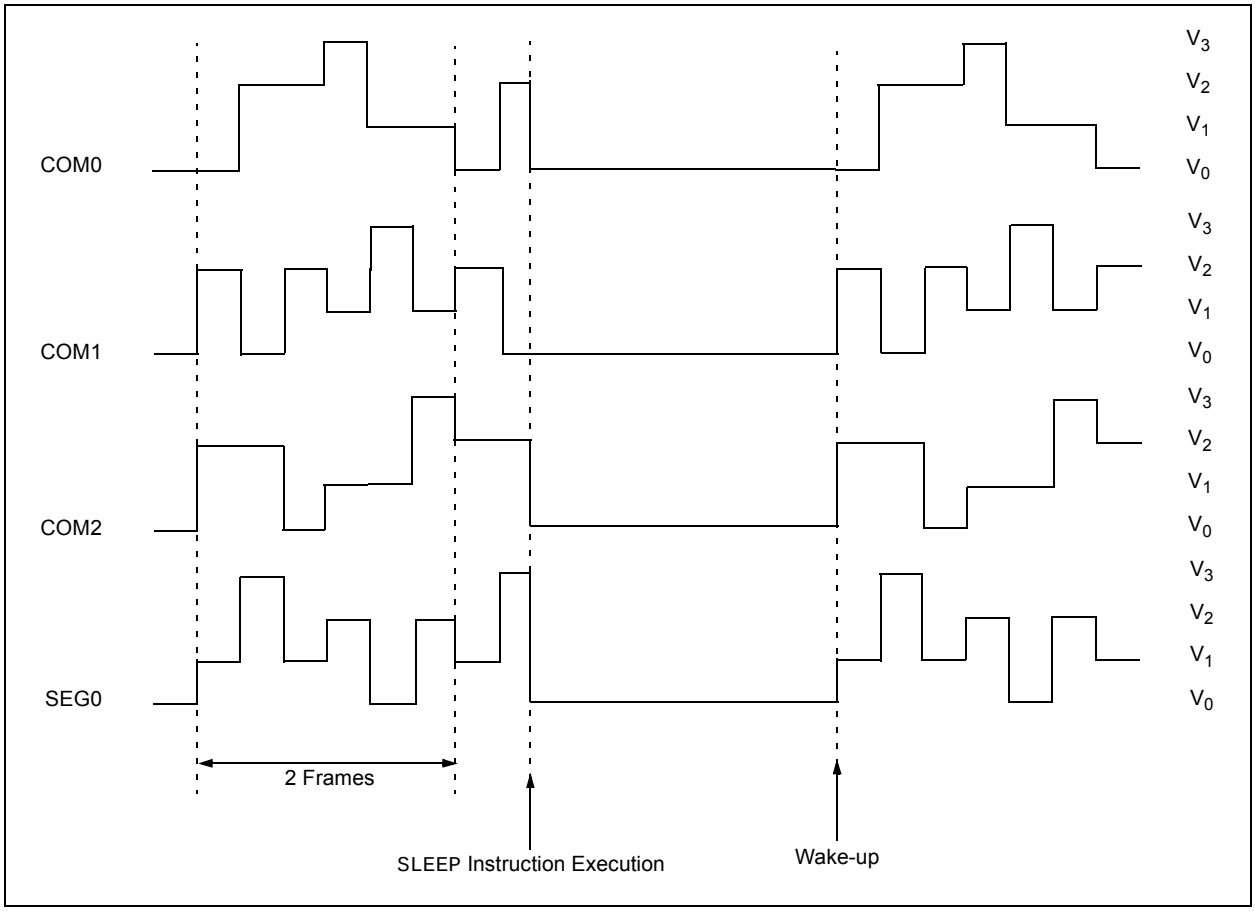


FIGURE 21-29: BUS COLLISION DURING START CONDITION (SCLx = 0)

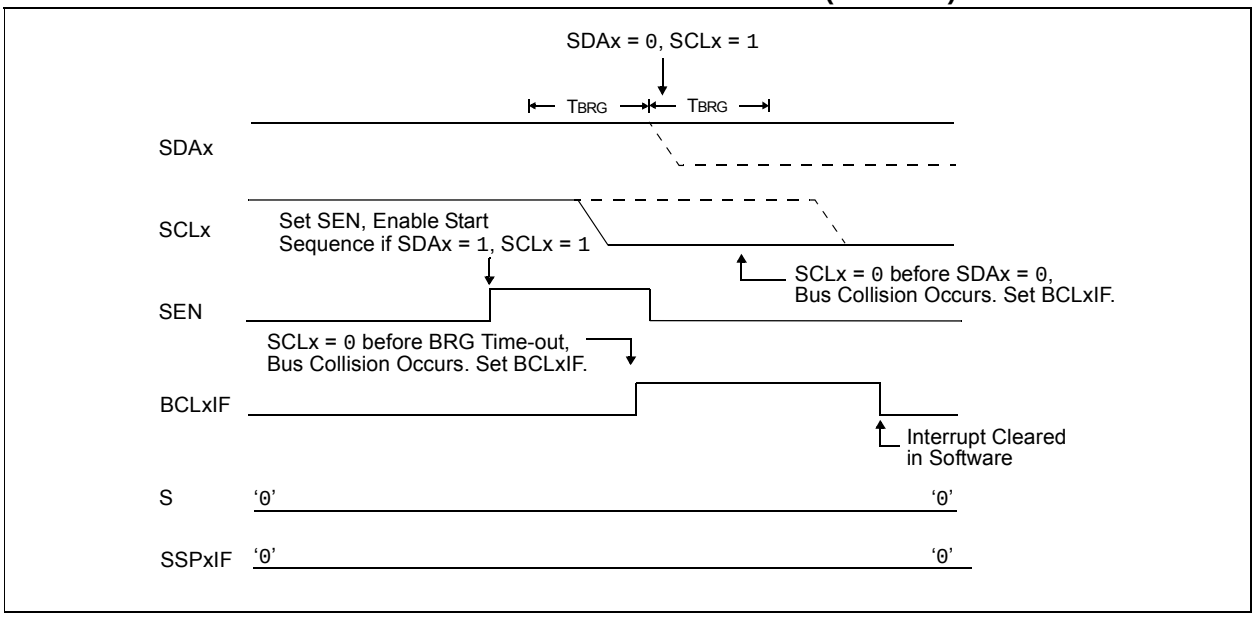
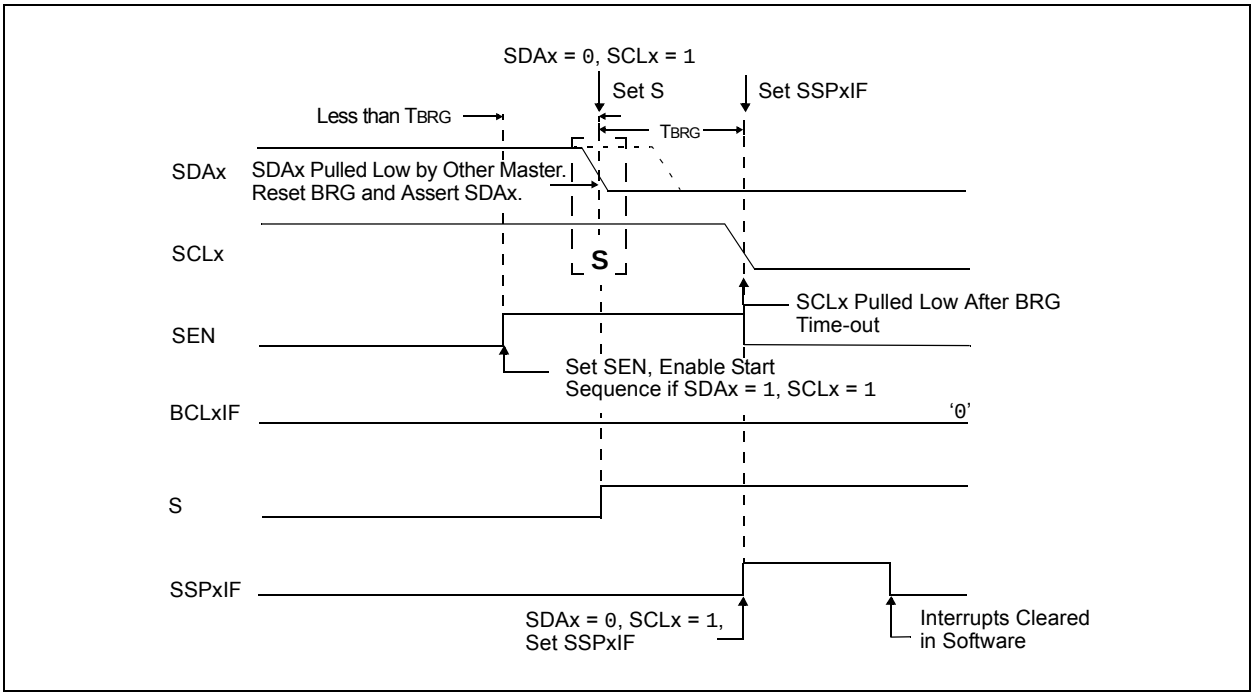


FIGURE 21-30: BRG RESET DUE TO SDAx ARBITRATION DURING START CONDITION



The ANCONx registers are used to configure the operation of the I/O pin associated with each analog channel. Clearing a ANSELx bit configures the corresponding pin (ANx) to operate as a digital only I/O. Setting a bit configures the pin to operate as an analog input for either the A/D Converter or the comparator module, with all digital peripherals disabled and digital inputs read as '0'.

As a rule, I/O pins that are multiplexed with analog inputs default to analog operation on any device Reset.

REGISTER 23-8: ANCON0: A/D PORT CONFIGURATION REGISTER 0

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ANSEL<7:0>:** Analog Port Configuration bits (AN7 and AN0)
0 = Pin is configured as a digital port
1 = Pin is configured as an analog channel – digital input disabled and any inputs read as '0'

REGISTER 23-9: ANCON1: A/D PORT CONFIGURATION REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSEL15(1)	ANSEL14(1)	ANSEL13(1)	ANSEL12(1)	ANSEL11	ANSEL10	ANSEL9	ANSEL8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ANSEL<15:8>:** Analog Port Configuration bits (AN15 through AN8)
0 = Pin is configured as a digital port
1 = Pin is configured as an analog channel – digital input is disabled and any inputs read as '0'

Note 1: AN12 through AN15, and AN20 to AN23, are implemented only on 80-pin devices. For 64-pin devices, the corresponding ANSELx bits are still implemented for these channels, but have no effect.

26.6 Operation During Sleep

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake-up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

26.7 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

TABLE 26-1: REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	77
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR2	OSCFIF	—	SSP2IF	BLC2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF	77
PIE2	OSCFIE	—	SSP2IE	BLC2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE	77
IPR2	OSCFIP	—	SSP2IP	BLC2IP	BCL1IP	HLVDIP	TMR3IP	TMR3GIP	77
TRISA	TRISA7(1)	TRISA6(1)	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	78

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the HLVD module.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

REGISTER 28-5: CONFIG3L: CONFIGURATION REGISTER 3 LOW (BYTE ADDRESS 300004h)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1
—	—	—	—	—	—	—	RTCOSC
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **RTCOSC:** RTCC Reference Clock Select bit
1 = RTCC uses SOSC as a reference clock
0 = RTCC uses LF-INTOSC as a reference clock

REGISTER 28-6: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	R/P-1	U-0	R/P-1	R/P-1
MCLRE	—	—	—	MSSPMSK	—	ECCPMX(1)	CCP2MX
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit
1 = $\overline{\text{MCLR}}$ pin is enabled; RG5 input pin is disabled
0 = RG5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **MSSPMSK:** MSSP V3 7-Bit Address Masking Mode Enable bit
1 = 7-Bit Address Masking mode is enabled
0 = 5-Bit Address Masking mode is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **ECCPMX:** ECCP MUX bit(1)
1 = Enhanced ECCP1 (P1B/P1C) is multiplexed onto RE6 and RE5, CCP6 onto RE6 and CCP7 onto RE5
Enhanced ECCP3 (P3B/P3C) is multiplexed onto RE4 and RE3, CCP8 onto RE4 and CCP9 onto RE3
0 = Enhanced ECCP1 (P1B/P1C) is multiplexed onto RH7 and RH6, CCP6 onto RH7 and CCP7 onto RH6
Enhanced ECCP3 (P3B/P3C) is multiplexed onto RH5 and RH4, CCP8 onto RH5 and CCP9 onto RH4

bit 0 **CCP2MX:** ECCP2 MUX bit
1 = ECCP2 is multiplexed with RC1
0 = ECCP2 input/output is multiplexed with RE7(1)

Note 1: This feature is only available on 80-pin devices.

28.3 On-Chip Voltage Regulator

All of the PIC18F87K90 family devices power their core digital logic at a nominal 3.3V. For designs that are required to operate at a higher typical voltage, such as 5V, all family devices incorporate two on-chip regulators that allow the device to run its core logic from VDD. Those regulators are:

- Normal On-Chip Regulator
- Ultra Low-Power, On-Chip Regulator

The hardware configuration of these regulators is the same and is explained in **Section 28.3.1 "Regulator Enable/disable by Hardware"**. The regulators' only differences relate to when the device enters Sleep, as explained in **Section 28.3.2**.

28.3.1 REGULATOR ENABLE/DISABLE BY HARDWARE

The regulator can be enabled or disabled only by hardware. The regulator is controlled by the ENVREG pin and the VDDCORE/VCAP pin.

28.3.1.1 Regulator Enable Mode

Tying VDD to the pin enables the regulator, which in turn, provides power to the core from the other VDD pins.

When the regulator is enabled, a low-ESR filter capacitor must be connected to the VDDCORE/VCAP pin (see Figure 28-2). This helps maintain the regulator's stability. The recommended value for the filter capacitor is given in **Section 31.2 DC Characteristics**.

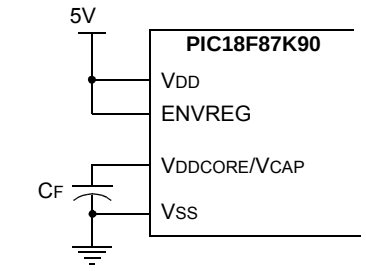
28.3.1.2 Regulator Disable Mode

If ENVREG is tied to VSS, the regulator is disabled. In this case, a 0.1 μF capacitor should be connected to the VDDCORE/VCAP pin (see Figure 28-2).

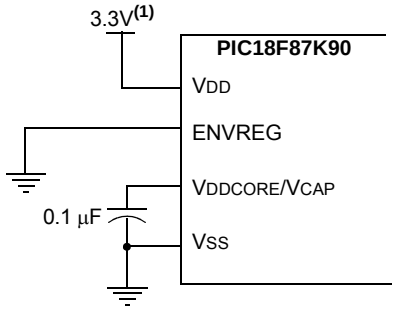
When the regulator is being used, the overall voltage budget is very tight. The regulator should operate the device down to 1.8V. When VDD drops below 3.3V, the regulator no longer regulates, but the output voltage follows the input until VDD reaches 1.8V. Below this voltage, the output of the regulator output may drop to 0V.

FIGURE 28-2: CONNECTIONS FOR THE ON-CHIP REGULATOR

Regulator Enabled (ENVREG tied to VDD):



Regulator Disabled (ENVREG tied to VSS):



Note 1: These are typical operating voltages. For the full operating ranges of VDD and VDDCORE, see **Section 31.2 "DC Characteristics"**.

BNC **Branch if Not Carry**

Syntax: BNC n

Operands: -128 ≤ n ≤ 127

Operation: if Carry bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0011	nnnn	nnnn

Description: If the Carry bit is '0', then the program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNC Jump

Before Instruction
PC = address (HERE)
After Instruction
If Carry = 0;
PC = address (Jump)
If Carry = 1;
PC = address (HERE + 2)

BNN **Branch if Not Negative**

Syntax: BNN n

Operands: -128 ≤ n ≤ 127

Operation: if Negative bit is '0',
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0111	nnnn	nnnn

Description: If the Negative bit is '0', then the program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNN Jump

Before Instruction
PC = address (HERE)
After Instruction
If Negative = 0;
PC = address (Jump)
If Negative = 1;
PC = address (HERE + 2)

30.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

30.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

30.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

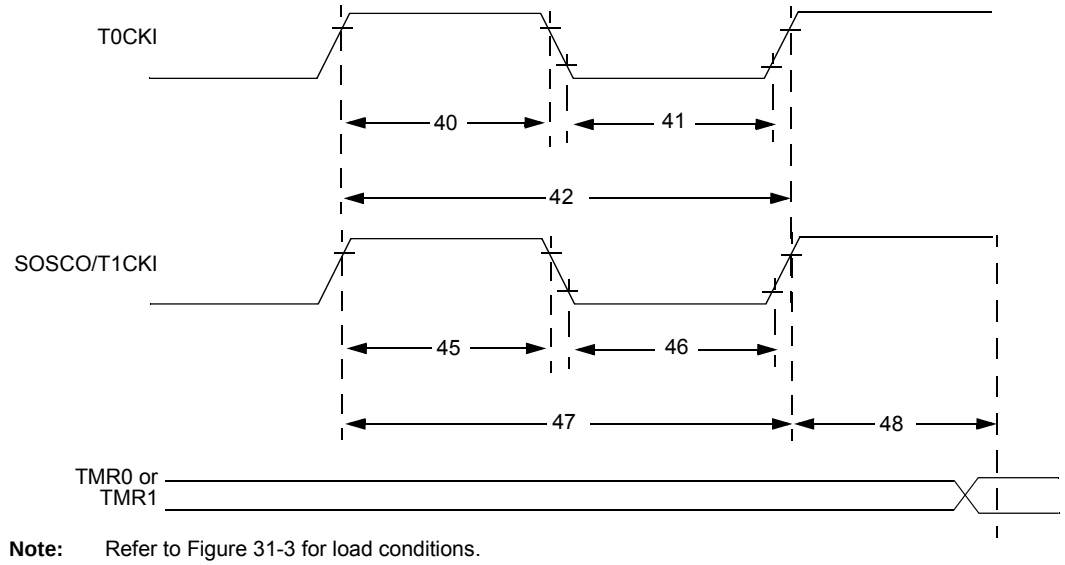
The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

FIGURE 31-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

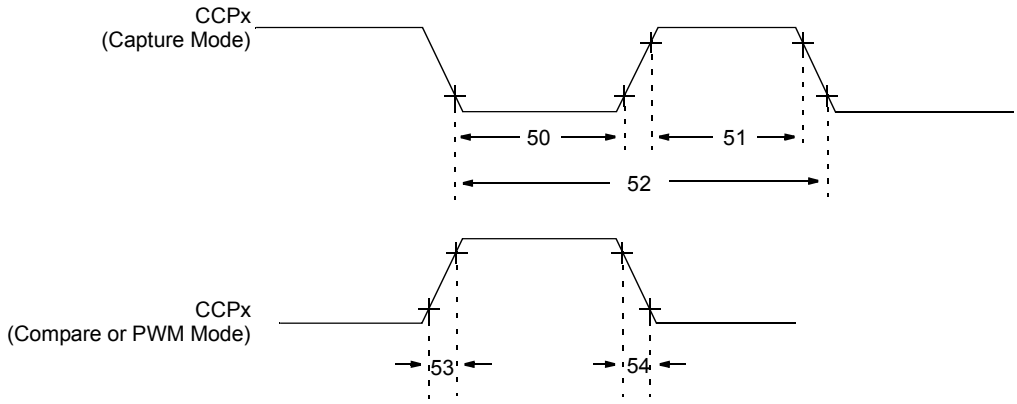


Note: Refer to Figure 31-3 for load conditions.

TABLE 31-12: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
40	TT0H	T0CKI High Pulse Width	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
41	TT0L	T0CKI Low Pulse Width	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
42	TT0P	T0CKI Period	No prescaler	TCY + 10	—	ns	
			With prescaler	Greater of: 20 ns or (TCY + 40)/N	—	ns	N = prescale value (1, 2, 4,..., 256)
45	TT1H	T1CKI High Time	Synchronous, no prescaler	0.5 TCY + 20	—	ns	
			Synchronous, with prescaler	10	—	ns	
			Asynchronous	30	—	ns	
46	TT1L	T1CKI Low Time	Synchronous, no prescaler	0.5 TCY + 5	—	ns	
			Synchronous, with prescaler	10	—	ns	
			Asynchronous	30	—	ns	
47	TT1P	T1CKI Input Period	Synchronous	Greater of: 20 ns or (TCY + 40)/N	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	ns	
	FT1	T1CKI Oscillator Input Frequency Range		DC	50	kHz	
48	TCKE2TMRI	Delay from External T1CKI Clock Edge to Timer Increment		2 TOSC	7 TOSC	—	

FIGURE 31-10: CAPTURE/COMPARE/PWM TIMINGS (ECCP1, ECCP2 MODULES)



Note: Refer to Figure 31-3 for load conditions.

TABLE 31-13: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP1, ECCP2 MODULES)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
51	TccH	CCPx Input High Time	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
52	TccP	CCPx Input Period		$\frac{3\ T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		—	25	ns	
54	TccF	CCPx Output Fall Time		—	25	ns	