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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f87k90t-i-ptrsl

Special Microcontroller Features:

- Operating Voltage Range: 1.8V to 5.5V
- On-Chip 3.3V Regulator
- Operating Speed up to 64 MHz
- Up to 128 Kbytes On-Chip Flash Program Memory
- Data EEPROM of 1,024 Bytes
- 4K x 8 General Purpose Registers (SRAM)
- 10,000 Erase/Write Cycle Flash Program Memory, Minimum
- 1,000,000 Erase/write Cycle Data EEPROM Memory, Typical
- Flash Retention 40 Years, Minimum
- Three Internal Oscillators: LF-INTRC (31 kHz), MF-INTOSC (500 kHz) and HF-INTOSC (16 MHz)
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 4,194s (about 70 minutes)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Programmable:
  - BOR
  - LVD
- Two Enhanced Addressable USART modules:
  - LIN/J2602 support
  - Auto-Baud Detect (ABD)
- 12-Bit A/D Converter with up to 24 Channels:
  - Auto-acquisition and Sleep operation
  - Differential Input mode of operation

3.8 Effects of Power-Managed Modes on the Various Clock Sources

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the SOSC oscillator is operating and providing the device clock. The SOSC oscillator may also run in all power-managed modes if required to clock SOSC.

In RC_RUN and RC_IDLE modes, the internal oscillator provides the device clock source. The 31 kHz LF-INTOSC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see **Section 28.2 "Watchdog Timer (WDT)"** through **Section 28.5 "Fail-Safe Clock Monitor"** for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up).

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTOSC is required to support WDT operation. The SOSC oscillator may be operating to support a Real-Time Clock (RTC). Other features may be operating that do not require a device clock source (i.e., MSSP slave, INTx pins and others). Peripherals that may add significant current consumption are listed in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/ Extended)"**.

3.9 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 5.6 "Power-up Timer (PWRT)"**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on a power-up time of about 64 ms (Parameter 33, Table 31-10); it is always enabled.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (HS, XT or LP modes). The OST does this by counting 1,024 oscillator cycles before allowing the oscillator to clock the device.

There is a delay of interval, TCSD (Parameter 38, Table 31-10), following POR, while the controller becomes ready to execute instructions.

TABLE 3-4: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

Oscillator Mode	OSC1 Pin	OSC2 Pin
EC, ECPLL	Floating, pulled by external clock	At logic low (clock/4 output)
HS, HSPLL	Feedback inverter is disabled at quiescent voltage level	Feedback inverter is disabled at quiescent voltage level
INTOSC, INTPLL1/2	I/O pin, RA6, direction is controlled by TRISA<6>	I/O pin, RA6, direction is controlled by TRISA<7>

Note: See **Section 5.0 "Reset"** for time-outs due to Sleep and $\overline{\text{MCLR}}$ Reset.

4.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode provides controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute SLEEP. To maintain software compatibility with future devices, it is recommended that SCS0 also be cleared, though its value is ignored. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the SLEEP instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value, or the INTSRC/MFIOSEL bit is set, the INTOSC output is enabled. The HFIOFS/MFIOFS bits become set, after the INTOSC output becomes stable after an interval of TIOBST (Parameter 38, Table 31-10). (For information on the HFIOFS/MFIOFS bits, see Table 4-3.)

Clocks to the peripherals continue while the INTOSC source stabilizes. The HFIOFS/MFIOFS bits will remain set if the IRCF bits were previously at a non-zero value or if INTSRC was set before the SLEEP instruction was executed and the INTOSC source was already stable. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the HFIOFS/MFIOFS bits will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TCSD (Parameter 38, Table 31-10), following the wake event, the CPU begins executing code clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

4.5 Selective Peripheral Module Control

Idle mode allows users to substantially reduce power consumption by stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume power. There may be cases where the application needs what this mode does not provide: the allocation of power resources to the CPU, processing with minimal power consumption from the peripherals.

PIC18F87K90 family devices address this requirement by allowing peripheral modules to be selectively disabled, reducing or eliminating their power consumption. This can be done with two control bits:

- Peripheral Enable bit, generically named XXXEN – Located in the respective module's main control register
- Peripheral Module Disable (PMD) bit, generically named XXXMD – Located in one of the PMDx Control registers (PMD0, PMD1, PMD2 or PMD3)

Disabling a module by clearing its XXXEN bit disables the module's functionality, but leaves its registers available to be read and written to. This reduces power consumption, but not by as much as the second approach.

Most peripheral modules have an enable bit.

In contrast, setting the PMD bit for a module disables all clock sources to that module, reducing its power consumption to an absolute minimum. In this state, the control and status registers associated with the peripheral are also disabled, so writes to those registers have no effect and read values are invalid. Many peripheral modules have a corresponding PMD bit.

There are four PMD registers in the PIC18F87K90 family devices: PMD0, PMD1, PMD2 and PMD3. These registers have bits associated with each module for disabling or enabling a particular peripheral.

5.2 Master Clear ($\overline{MCLR}$)

The $\overline{MCLR}$ pin provides a method for triggering a hard external Reset of the device. A Reset is generated by holding the pin low. PIC18 extended microcontroller devices have a noise filter in the $\overline{MCLR}$ Reset path which detects and ignores small pulses.

The $\overline{MCLR}$ pin is not driven low by any internal Resets, including the WDT.

5.3 Power-on Reset (POR)

A Power-on Reset condition is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{MCLR}$ pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (Parameter D004). For a slow rise time, see Figure 5-2.

When the device starts normal operation (exiting the Reset condition), device operating parameters (such as voltage, frequency and temperature) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

Power-on Reset events are captured by the $\overline{POR}$ bit (RCON<1>). The state of the bit is set to '0' whenever a Power-on Reset occurs and does not change for any other Reset event. $\overline{POR}$ is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any Power-on Reset.

5.4 Brown-out Reset (BOR)

The PIC18F87K90 family has four BOR modes:

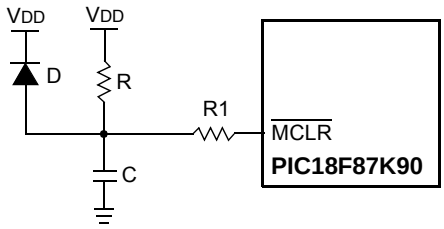
- High-Power BOR
- Medium Power BOR
- Low-Power BOR
- Zero-Power BOR

Each power mode is selected by the BORPWR<1:0> bits setting (CONFIG2L<6:5>). For low, medium and high-power BOR, the module monitors the VDD depending on the BORV<1:0> setting (CONFIG1L<3:2>). A BOR event re-arms the Power-on Reset. It also causes a Reset depending on which of the trip levels has been set: 1.8V, 2V, 2.7V or 3V. The typical (ΔIBOR) trip level for the Low and Medium Power BOR will be 0.75 μA and 3 μA.

In Zero-Power BOR (ZPBORMV), the module monitors the VDD voltage and re-arms the POR at about 2V. ZPBORMV does not cause a Reset, but re-arms the POR.

The BOR accuracy varies with its power level. The lower the power setting, the less accurate the BOR trip levels are. So, the high-power BOR has the highest accuracy and the low-power BOR has the lowest accuracy. The trip levels (BVDD, Parameter D005), current consumption (**Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended)"**) and time required below BVDD (TBOR, Parameter 35) can all be found in **Section 31.0 "Electrical Characteristics"**

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode, D, helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

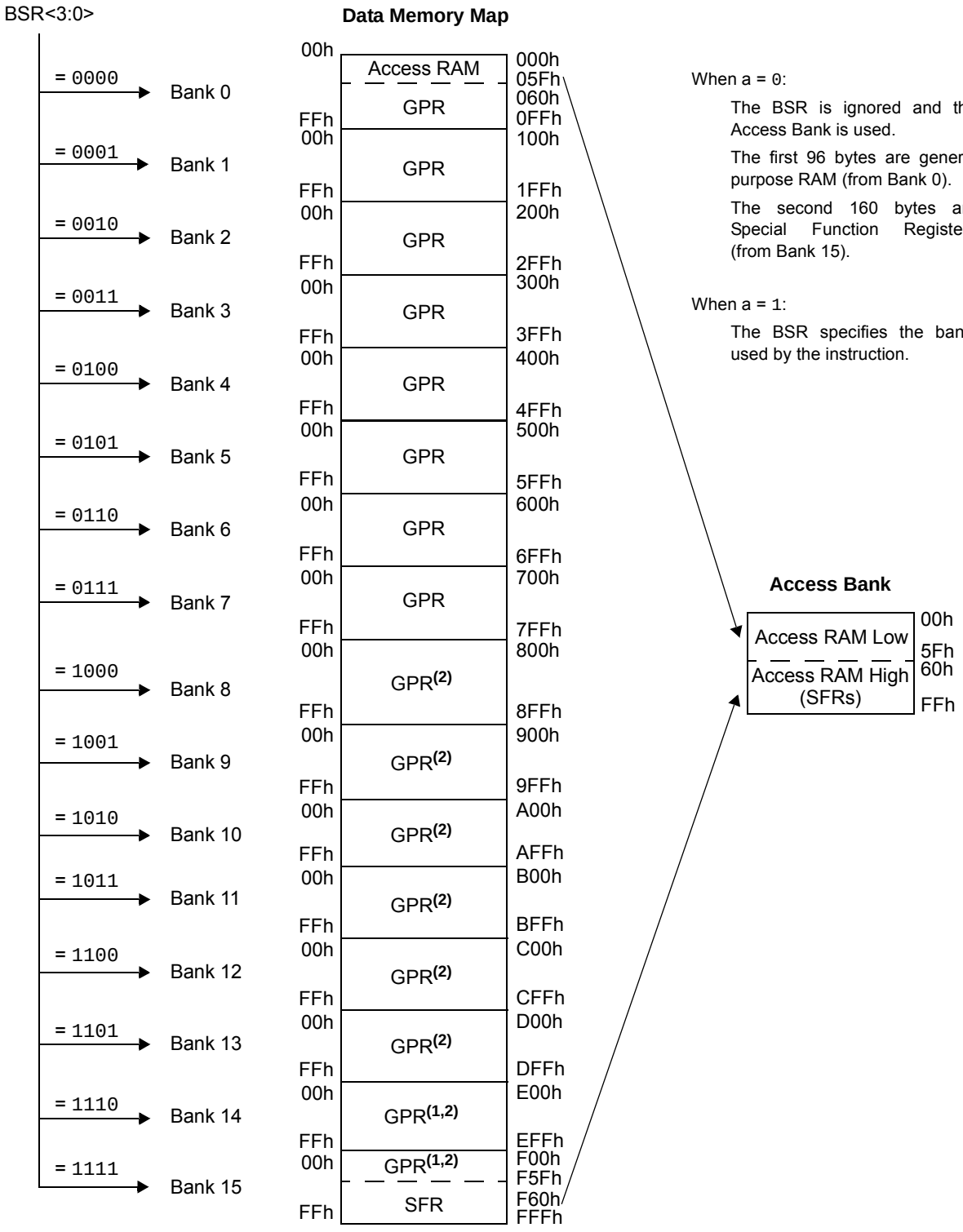
3: R1 ≥ 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor, C, in the event of $\overline{MCLR}$/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5.4.1 DETECTING BOR

The $\overline{BOR}$ bit always resets to '0' on any Brown-out Reset or Power-on Reset event. This makes it difficult to determine if a Brown-out Reset event has occurred just by reading the state of $\overline{BOR}$ alone. A more reliable method is to simultaneously check the state of both $\overline{POR}$ and $\overline{BOR}$. This assumes that the $\overline{POR}$ bit is reset to '1' in software immediately after any Power-on Reset event. If $\overline{BOR}$ is '0' while $\overline{POR}$ is '1', it can be reliably assumed that a Brown-out Reset event has occurred.

LP-BOR cannot be detected with the $\overline{BOR}$ bit in the RCON register. LP-BOR can rearm the $\overline{POR}$ and can cause a Power-on Reset.

FIGURE 6-6: DATA MEMORY MAP FOR PIC18FX5K90 AND PIC18FX7K90 DEVICES



Note 1: Addresses, EF4h through F5Fh, are also used by SFRs, but are not part of the Access RAM. Users must always use the complete address, or load the proper BSR value, to access these registers.

2: These addresses are unused for devices with 32 Kbytes of program memory (PIC18FX5K90). For those devices, read these addresses at 00h.

REGISTER 10-21: IPR6: PERIPHERAL INTERRUPT PRIORITY REGISTER 6

U-0	U-0	U-0	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	—	EEIP	—	CMP3IP	CMP2IP	CMP1IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **EEIP:** EE Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 **SBOREN:** Read as ‘0’

bit 2 **CMP3IP:** CMP3 Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **CMP2IP:** CMP2 Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **CMP1IP:** CMP1 Interrupt Priority bit
1 = High priority
0 = Low priority

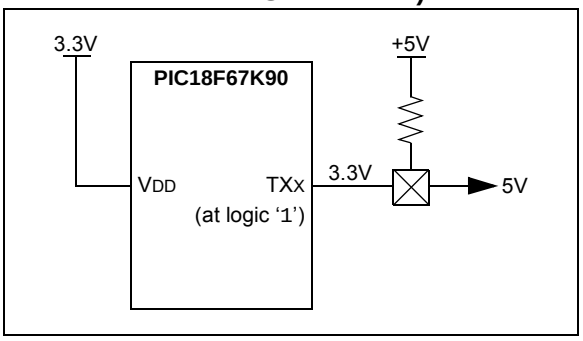
11.1.3 OPEN-DRAIN OUTPUTS

The output pins for several peripherals are also equipped with a configurable, open-drain output option. This allows the peripherals to communicate with external digital logic, operating at a higher voltage level, without the use of level translators.

The open-drain option is implemented on port pins specifically associated with the data and clock outputs of the USARTs, the MSSP module (in SPI mode) and the CCP modules. This option is selectively enabled by setting the open-drain control bits in the registers: ODCON1, ODCON2 and ODCON3.

When the open-drain option is required, the output pin must also be tied through an external pull-up resistor provided by the user to a higher voltage level, up to 5V (Figure 11-2). When a digital logic high signal is output, it is pulled up to the higher voltage level.

FIGURE 11-2: USING THE OPEN-DRAIN OUTPUT (USART SHOWN AS EXAMPLE)



REGISTER 11-1: ODCON1: PERIPHERAL OPEN-DRAIN CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
SSP1OD	CCP2OD	CCP1OD	—	—	—	—	SSP2OD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SSP1OD:** SPI1 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 6 **CCP2OD:** ECCP2 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 5 **CCP1OD:** ECCP1 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **SSP2OD:** SPI2 Open-Drain Output Enable bit
1 = Open-drain capability is enabled
0 = Open-drain capability is disabled

11.7 PORTF, LATF and TRISF Registers

PORTF is a 7-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISF and LATF. All pins on PORTF are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTF is multiplexed with analog peripheral functions, as well as LCD segments. Pins, RF1 through RF6, may be used as comparator inputs or outputs by setting the appropriate bits in the CMCON register. To use RF<7:1> as digital inputs, it is also necessary to turn off the comparators.

Note 1: On device Resets, pins, RF<7:1>, are configured as analog inputs and are read as '0'.

2: To configure PORTF as a digital I/O, turn off the comparators and clear ANCON1 and ANCON2 to digital.

PORTF is also multiplexed with LCD segment drives controlled by bits in the LCDSE2 and LCDSE3 registers. I/O port functions are only available when the segments are disabled.

EXAMPLE 11-6: INITIALIZING PORTF

```
CLRF     PORTF    ; Initialize PORTF by
                  ; clearing output
                  ; data latches
CLRF     LATF     ; Alternate method
                  ; to clear output
                  ; data latches
BANKSEL  ANCON1
MOVLW    01Fh     ; Make AN6, AN7 and AN5 digital
MOVWF    ANCON1   ;
MOVLW    0F0h     ; Make AN8, AN9, AN10 and AN11
                    digital
MOVWF    ANCON2   ; Set PORTF as digital I/O
MOVLW    0CEh     ; Value used to
                  ; initialize data
                  ; direction
MOVWF    TRISF    ; Set RF3:RF1 as inputs
                  ; RF5:RF4 as outputs
                  ; RF7:RF6 as inputs
```

20.1 LCD Registers

The LCD driver module has 32 registers:

- LCD Control Register (LCDCON)
- LCD Phase Register (LCDPS)
- LCD Reference Ladder Register (LCDRL)
- LCD Reference Voltage Control Register (LCDREF)
- Six LCD Segment Enable Registers (LCDSE5:LCDSE0)
- 24 LCD Data Registers (LCDDATA23:LCDDATA0)

The LCDCON register, shown in Register 20-1, controls the overall operation of the module. Once the module is configured, the LCDEN (LCDCON<7>) bit is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN (LCDCON<6>) bit.

The LCDPS register, shown in Register 20-2, configures the LCD clock source prescaler and the type of waveform, Type-A or Type-B. For details on these features, see **Section 20.2 "LCD Clock Source Selection"**, **Section 20.3 "LCD Bias Types"** and **Section 20.8 "LCD Waveform Generation"**.

REGISTER 20-1: LCDCON: LCD CONTROL REGISTER

R/W-0	R/W-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDEN	SLPEN	WERR	—	CS1	CS0	LMUX1	LMUX0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled

bit 6 **SLPEN:** LCD Driver Enable in Sleep mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode

bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register is written while WA (LCDPS<4>) = 0 (must be cleared in software)
0 = No LCD write error

bit 4 **Unimplemented:** Read as '0'

bit 3-2 **CS<1:0>:** Clock Source Select bits
00 = (FOSC/4)/8192
01 = SOSC oscillator/32
1x = INTRC (31.25 kHz)/32

bit 1-0 **LMUX<1:0>:** Commons Select bits

LMUX<1:0>	Multiplex	Maximum Number of Pixels (PIC18F6X90)	Maximum Number of Pixels (PIC18F8X90)	Bias
00	Static (COM0)	33	48	Static
01	1/2 (COM<1:0>)	66	96	1/2 or 1/3
10	1/3 (COM<2:0>)	99	144	1/2 or 1/3
11	1/4 (COM<3:0>)	132	192	1/3

NOTES:

21.4.17.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDAx pin has been deasserted and allowed to float high, SDAx is sampled low after the BRG has timed out.

b) After the SCLx pin is deasserted, SCLx is sampled low before SDAx goes high.

The Stop condition begins with SDAx asserted low. When SDAx is sampled low, the SCLx pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD<6:0> and counts down to 0. After the BRG times out, SDAx is sampled. If SDAx is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 21-33). If the SCLx pin is sampled low before SDAx is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 21-34).

FIGURE 21-33: BUS COLLISION DURING A STOP CONDITION (CASE 1)

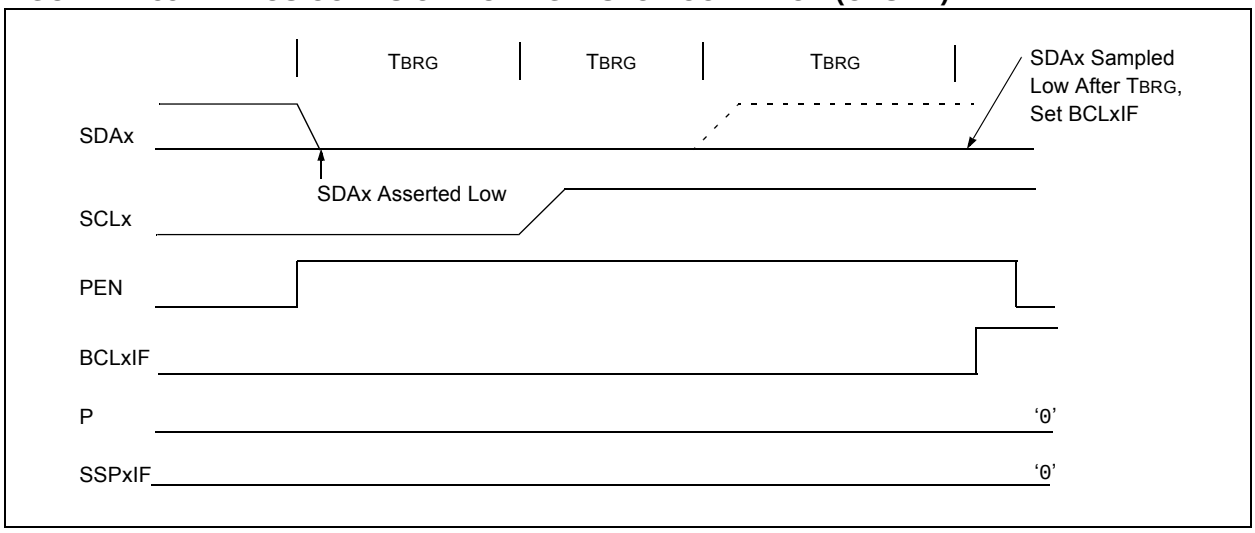


FIGURE 21-34: BUS COLLISION DURING A STOP CONDITION (CASE 2)

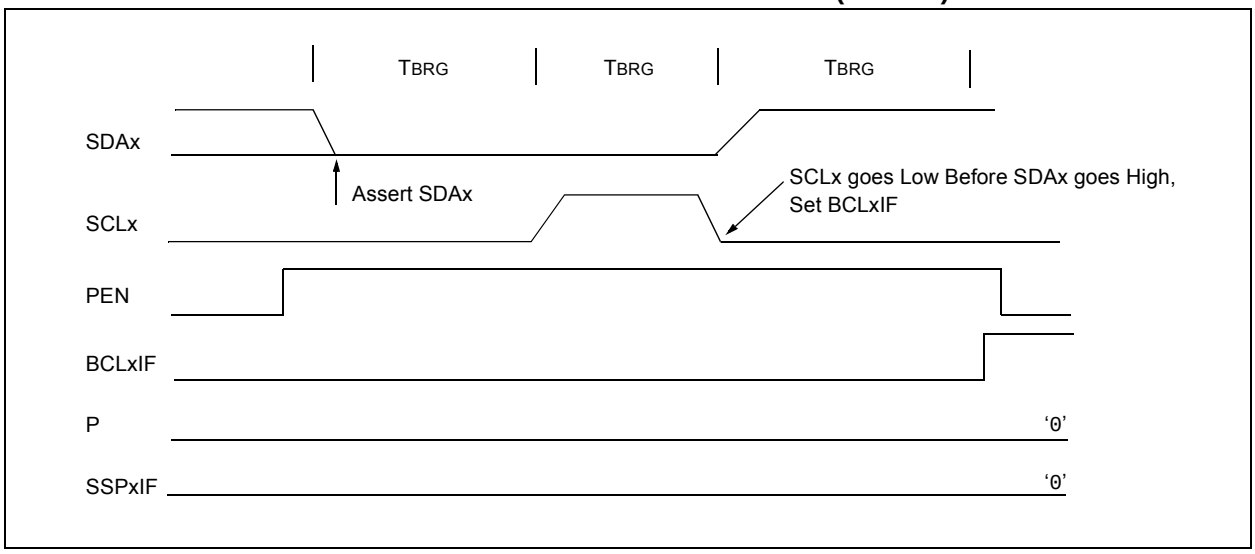
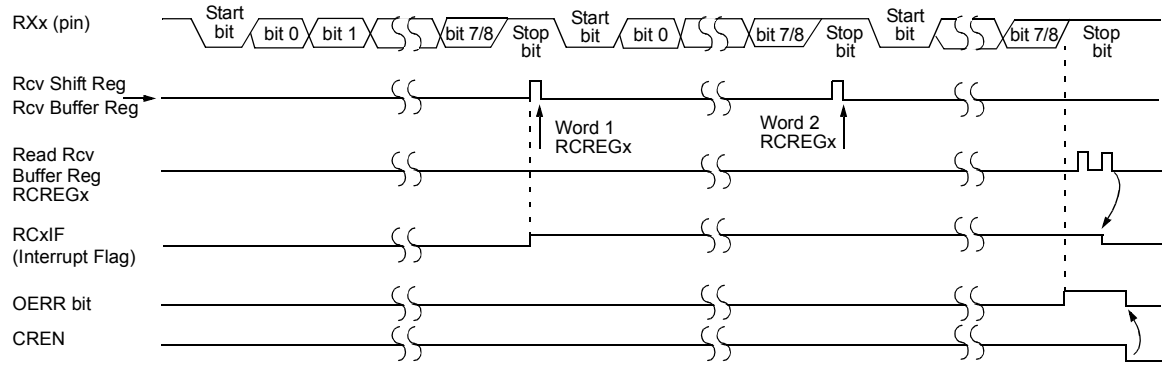


FIGURE 22-7: ASYNCHRONOUS RECEPTION



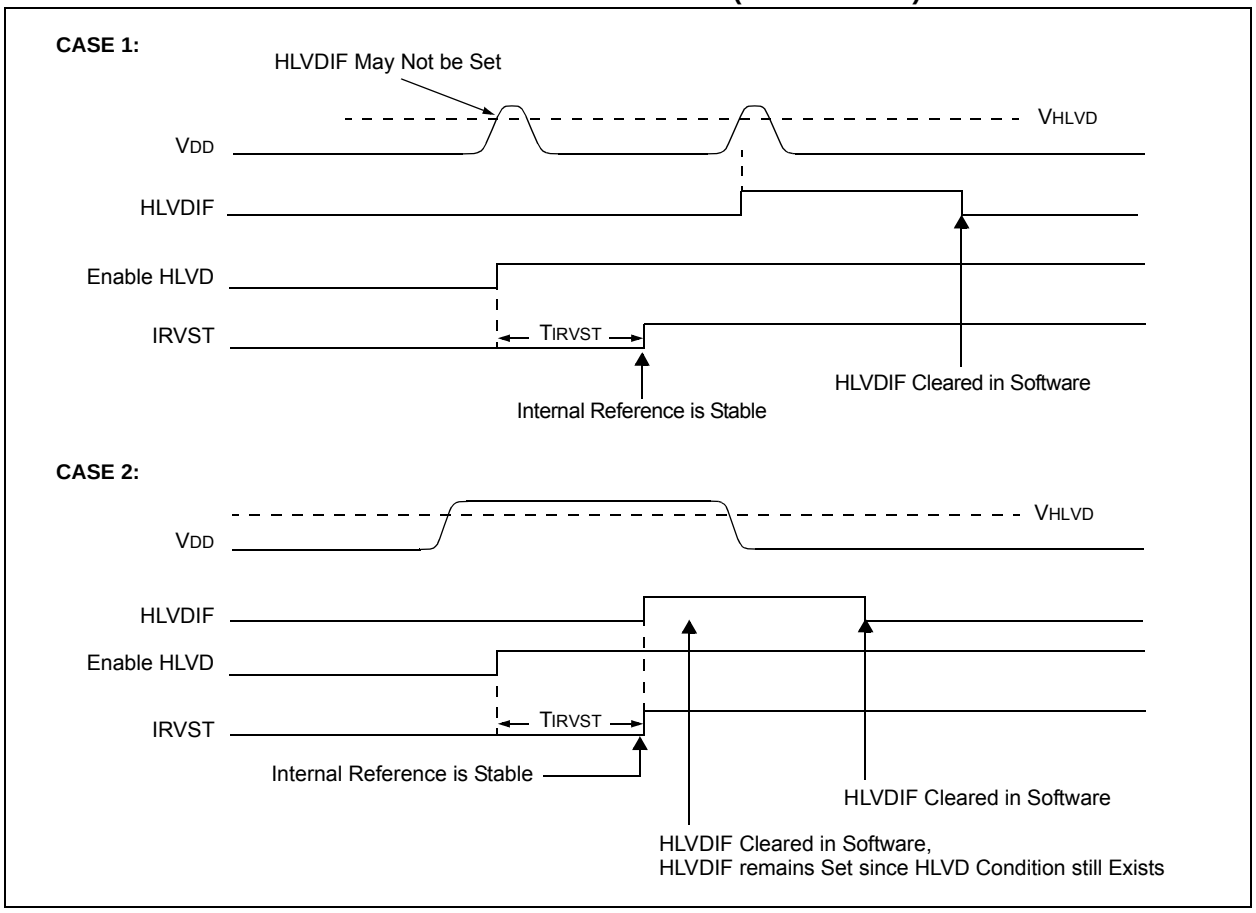
Note: This timing diagram shows three words appearing on the RXx input. The RCREGx (Receive Buffer) is read after the third word causing the OERR (Overrun) bit to be set.

TABLE 22-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF	77
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE	77
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP	77
PIR3	TMR5GIF	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	77
PIE3	TMR5GIE	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	77
IPR3	TMR5GIP	LCDIP	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP	77
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	77
RCREG1	EUSART1 Receive Register								77
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	77
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	79
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte								76
SPBRG1	EUSART1 Baud Rate Generator Register Low Byte								77
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	81
RCREG2	EUSART2 Receive Register								82
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	81
BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	81
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte								82
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte								82

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

FIGURE 26-3: HIGH-VOLTAGE DETECT OPERATION (VDIRMAG = 1)

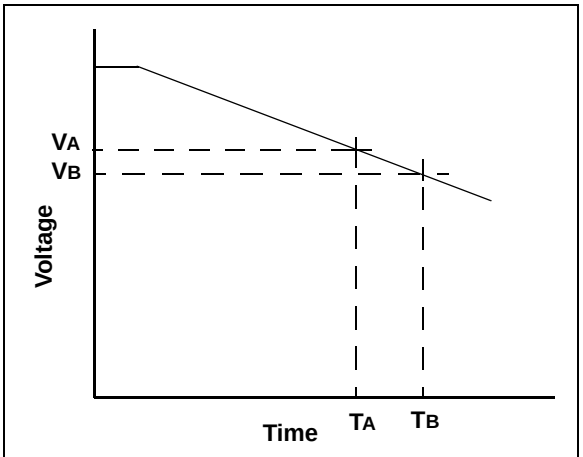


26.5 Applications

In many applications, it is desirable to detect a drop below, or rise above, a particular voltage threshold. For example, the HLVD module could be periodically enabled to detect Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a High-Voltage Detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 26-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, VA, the HLVD logic generates an interrupt at time, TA. The interrupt could cause the execution of an ISR (Interrupt Service Routine), which would allow the application to perform “housekeeping tasks” and a controlled shutdown before the device voltage exits the valid operating range at TB. This would give the application a time window, represented by the difference between TA and TB, to safely exit.

FIGURE 26-4: TYPICAL LOW-VOLTAGE DETECT APPLICATION



Legend: VA = HLVD trip point
VB = Minimum valid device operating voltage

REGISTER 28-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	U-0	R/P-1
—	XINST	—	SOSCSEL1	SOSCSEL0	INTOSCSEL0	—	$\overline{\text{RETEN}}$
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **XINST:** Extended Instruction Set Enable bit

1 = Instruction set extension and Indexed Addressing mode are enabled
0 = Instruction set extension and Indexed Addressing mode are disabled (Legacy mode)

bit 5 **Unimplemented:** Read as ‘0’

bit 4-3 **SOSCSEL<1:0>:** SOSC Power Selection and Mode Configuration bits

11 = High-power SOSC circuit is selected
10 = Digital (SCLKI) mode: I/O port functionality of RC0 and RC1 is enabled
01 = Low-power SOSC circuit is selected
00 = Reserved

bit 2 **INTOSCSEL:** LF-INTOSC Low-Power Enable bit

1 = LF-INTOSC is in High-Power mode during Sleep
0 = LF-INTOSC is in Low-Power mode during Sleep

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **$\overline{\text{RETEN}}$:** VREG Sleep Enable bit

1 = Ultra low-power regulator is disabled. Regulator power in Sleep mode is controlled by VREGSLP (WDTCON<7>)
0 = Ultra low-power regulator is enabled. Regulator power in Sleep mode is controlled by SRETEN (WDTCON<4>).

REGISTER 28-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

R/P-0	R/P-0	U-0	U-0	R/P-1	R/P-0	R/P-0	R/P-0
IESO	FCMEN	—	PLLCFG(1)	FOSC3(2)	FOSC2(2)	FOSC1(2)	FOSC0(2)
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IESO:** Internal/External Oscillator Switchover bit
1 = Two-Speed Start-up is enabled
0 = Two-Speed Start-up is disabled

bit 6 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **PLLCFG:** 4x PLL Enable bit(1)
1 = Oscillator is multiplied by 4
0 = Oscillator is used directly

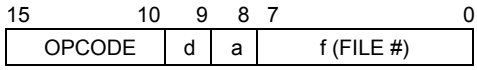
bit 3-0 **FOSC<3:0>:** Oscillator Selection bits(2)
1101 = EC1, EC oscillator (low power, DC-160 kHz)
1100 = EC1IO, EC oscillator with CLKOUT function on RA6 (low power, DC-160 kHz)
1011 = EC2, EC oscillator (medium power, 160 kHz-16 MHz)
1010 = EC2IO, EC oscillator with CLKOUT function on RA6 (medium power,160 kHz-16MHz)
0101 = EC3, EC oscillator (high power, 4 MHz-64 MHz)
0100 = EC3IO, EC oscillator with CLKOUT function on RA6 (high power, 4 MHz-64 MHz)
0011 = HS1, HS oscillator (medium power, 4 MHz-16 MHz)
0010 = HS2, HS oscillator (high power, 16 MHz-25 MHz)
0001 = XT oscillator
0000 = LP oscillator
0111 = RC, External RC oscillator
0110 = RCIO, External RC oscillator with CKLOUT function on RA6
1000 = INTIO2, Internal RC oscillator
1001 = INTIO1, Internal RC oscillator with CLKOUT function on RA6

Note 1: Not valid for the INTIOx PLL mode.
2: INTIO+PLL can only be enabled by the PLLEN bit (OSCTUNE<6>). Other PLL modes can be enabled by either the PLLEN bit or the PLLCFG (CONFIG1H<4>) bit.

FIGURE 29-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

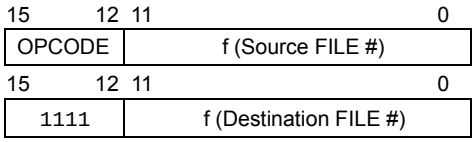
Example Instruction




```
ADDWF MYREG, W, B
```

d = 0 for result destination to be WREG register
d = 1 for result destination to be file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

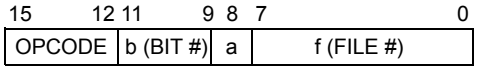
Byte to Byte move operations (2-word)




```
MOVFF MYREG1, MYREG2
```

f = 12-bit file register address

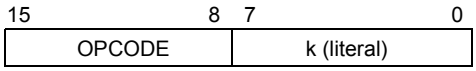
Bit-oriented file register operations




```
BSF MYREG, bit, B
```

b = 3-bit position of bit in file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

Literal operations

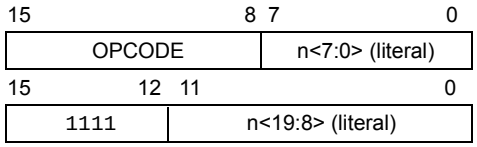



```
MOVLW 7Fh
```

k = 8-bit immediate value

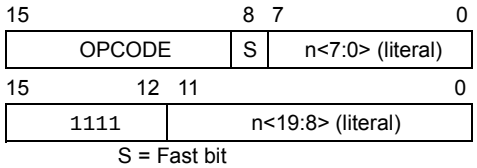
Control operations

CALL, GOTO and Branch operations



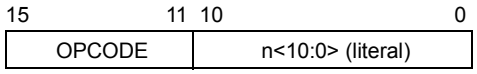

```
GOTO Label
```

n = 20-bit immediate value

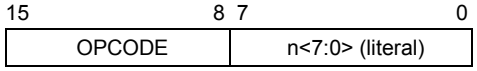



```
CALL MYFUNC
```

S = Fast bit




```
BRA MYFUNC
```




```
BC MYFUNC
```

RETURN **Return from Subroutine**

Syntax: RETURN {s}

Operands: s ∈ [0,1]

Operation: (TOS) → PC;
if s = 1,
(WS) → W,
(STATUSS) → STATUS,
(BSRS) → BSR,
PCLATU, PCLATH are unchanged

Status Affected: None

Encoding:

0000	0000	0001	001s

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the Program Counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If 's' = 0, no update of these registers occurs.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

Example: RETURN

After Instruction:
PC = TOS

RLCF **Rotate Left f through Carry**

Syntax: RLCF f {,d {,a}}

Operands: 0 ≤ f ≤ 255
d ∈ [0,1]
a ∈ [0,1]

Operation: (f<n>) → dest<n + 1>,
(f<7>) → C,
(C) → dest<0>

Status Affected: C, N, Z

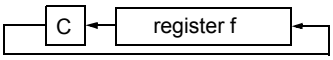
Encoding:

0011	01da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

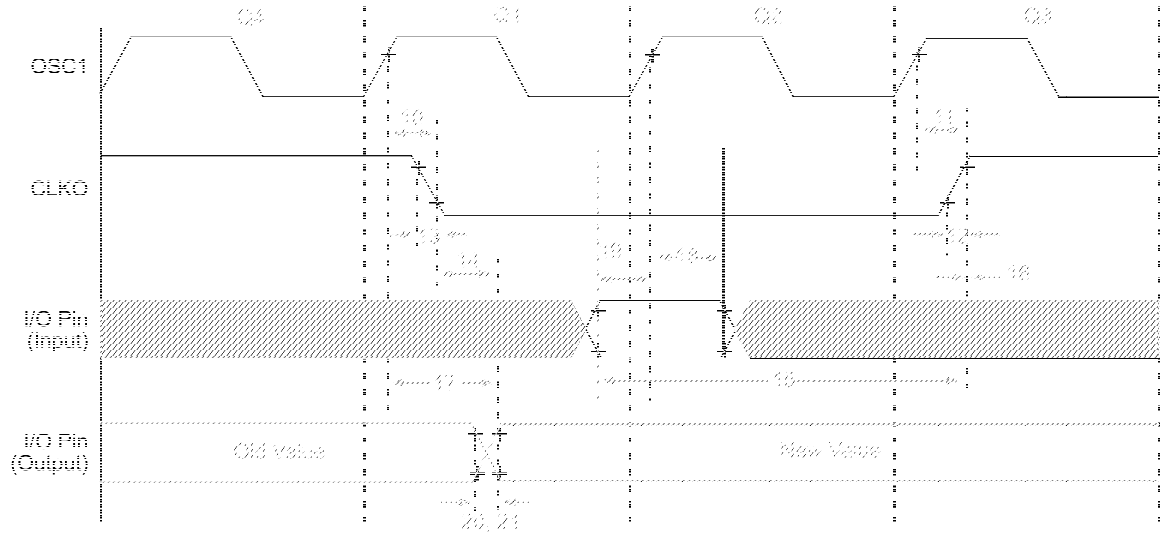
Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RLCF REG, 0, 0

Before Instruction
REG = 1110 0110
C = 0
After Instruction
REG = 1110 0110
W = 1100 1100
C = 1

FIGURE 31-5: CLKO AND I/O TIMING



Note: Refer to Figure 31-3 for load conditions.

TABLE 31-9: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
10	TOSH2CKL	OSC1 ↑ to CLKO ↓	—	75	200	ns	**(Note 1)**
11	TOSH2CKH	OSC1 ↑ to CLKO ↑	—	75	200	ns	**(Note 1)**
12	TCKR	CLKO Rise Time	—	15	30	ns	**(Note 1)**
13	TCKF	CLKO Fall Time	—	15	30	ns	**(Note 1)**
14	TCKL2IOV	CLKO ↓ to Port Out Valid	—	—	0.5 TCY + 20	ns	
15	TIOV2CKH	Port In Valid before CLKO ↑	0.25 TCY + 25	—	—	ns	
16	TCKH2IOI	Port In Hold after CLKO ↑	0	—	—	ns	
17	TOSH2IOV	OSC1 ↑ (Q1 cycle) to Port Out Valid	—	50	150	ns	
18	TOSH2IOI	OSC1 ↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	100	—	—	ns	
19	TIOV2OSH	Port Input Valid to OSC1 ↑ (I/O in setup time)	0	—	—	ns	
20	TIOR	Port Output Rise Time	—	10	25	ns	
21	TIOF	Port Output Fall Time	—	10	25	ns	
22†	TINP	INTx pin High or Low Time	20	—	—	ns	
23†	TRBP	RB<7:4> Change INTx High or Low Time	TCY	—	—	ns	

† These parameters are asynchronous events not related to any internal clock edges.

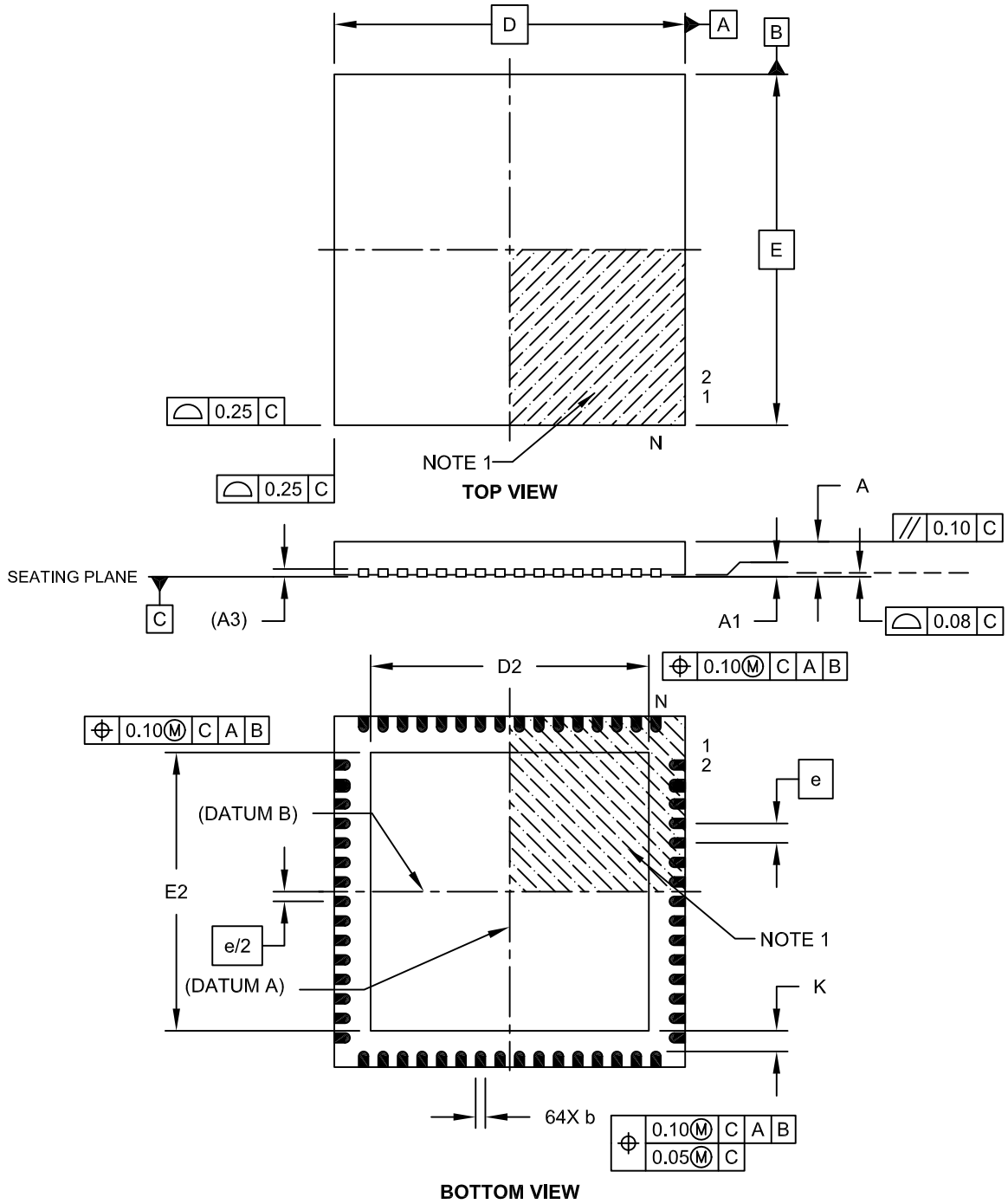
Note 1: Measurements are taken in EC mode, where CLKO output is 4 x TOSC.

32.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149B Sheet 1 of 2

D

E