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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf516spmc-gk7e1

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activation compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from power saving mode.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 32 external interrupt input pin
- Include one non-maskable interrupt(NMI)

Watch dog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- High-speed internal CR Clock : 4 MHz
- Low-speed internal CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

2. Packages

Package \ Product name	MB9BF516S MB9BF517S MB9BF518S	MB9BF516T MB9BF517T MB9BF518T
LQFP: FPT-144P-M08 (0.5 mm pitch)	○	-
LQFP: FPT-176P-M07 (0.5 mm pitch)	-	○
BGA: BGA-192P-M06 (0.8 mm pitch)	-	○

○: Supported

Note: See "14. Package Dimensions" for detailed information on each package.

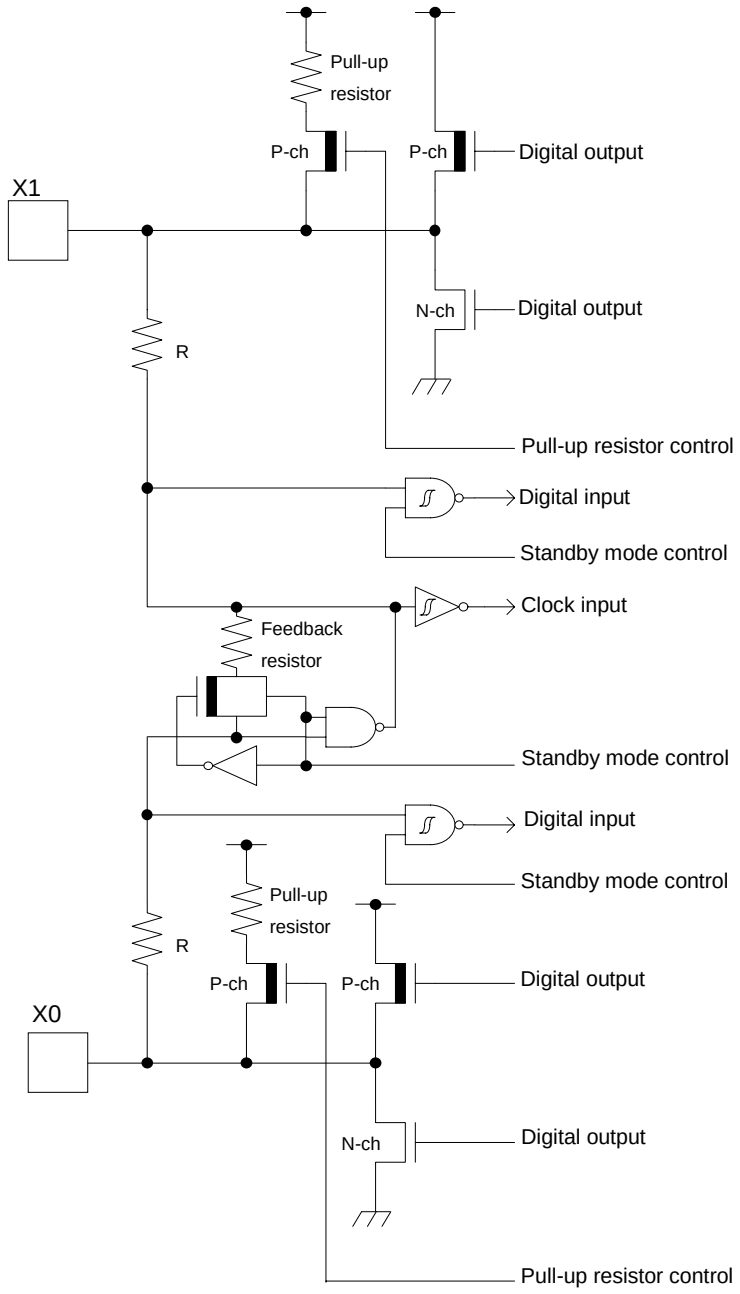
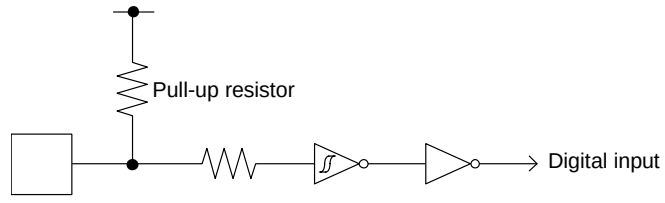
Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
20	20	G2	P57 SOT1_0 TIOB09_2 INT16_1 MNCLE_0	E	H
21	21	G3	P58 SCK1_0 TIOA11_2 INT17_1 MNWEX_0	E	H
22	22	G4	P59 SIN7_0 RX1_1 TIOB11_2 INT09_2 MNREX_0	E	H
23	23	G5	P5A SOT7_0 TX1_1 TIOA13_1 INT18_1 MCSX0_0	E	H
24	24	G6	P5B SCK7_0 TIOB13_1 INT19_1 MCSX1_0	E	H
25	-	H1	P5C TIOA06_2 INT28_0 IC20_1	E	H
26	-	H2	P5D TIOB06_2 INT29_0 DTTI2X_1	E	H
27	25	J1	VSS	-	
28	-	H3	P30 AIN0_0 TIOB00_1 INT03_2	E	H
29	-	H4	P31 BIN0_0 TIOB01_1 SCK6_1 INT04_2	E	H
30	-	H5	P32 ZIN0_0 TIOB02_1 SOT6_1 INT05_2	E	H

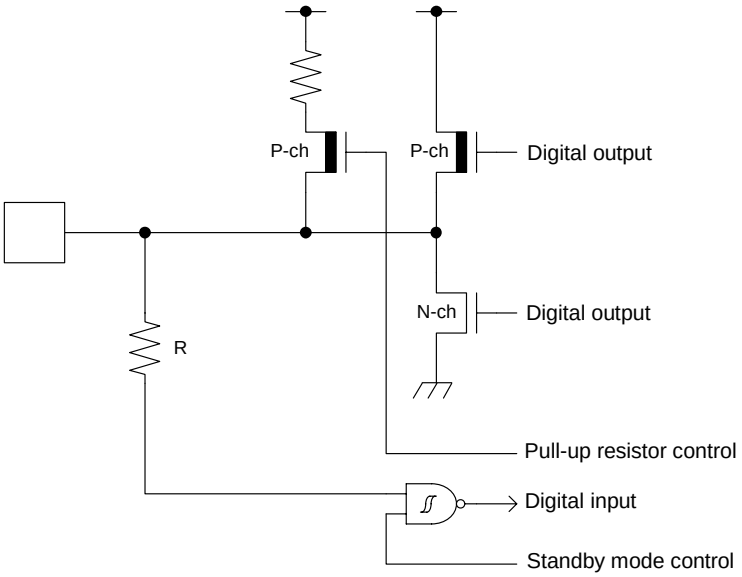
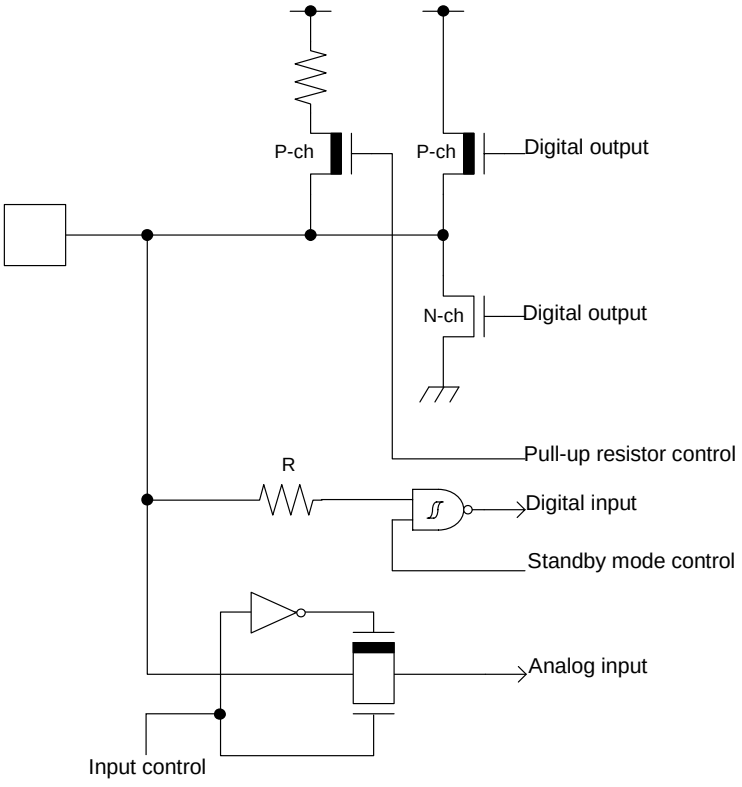
Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
31	-	H6	P33 INT04_0 TIOB03_1 SIN6_1 ADTG_6	E	H
32	-	J4	P34 FRCK0_0 TX0_1 TIOB04_1	E	I
33	-	J4	P35 IC03_0 RX0_1 TIOB05_1 INT08_1	E	H
34	26	J3	P36 IC02_0 SIN5_2 INT09_1 TIOA12_2 MCSX2_0	E	H
35	27	J2	P37 IC01_0 SOT5_2 INT10_1 TIOB12_2 MCSX3_0	E	H
36	28	K1	P38 IC00_0 SCK5_2 INT11_1 MCLKOUT_0	E	H
37	29	K2	P39 DTTI0X_0 ADTG_2	E	I
38	30	K3	P3A RTO00_0 TIOA00_1	G	I
39	31	K4	P3B RTO01_0 TIOA01_1	G	I
40	32	L1	P3C RTO02_0 TIOA02_1	G	I
41	33	L2	P3D RTO03_0 TIOA03_1	G	I
42	34	L3	P3E RTO04_0 TIOA04_1	G	I

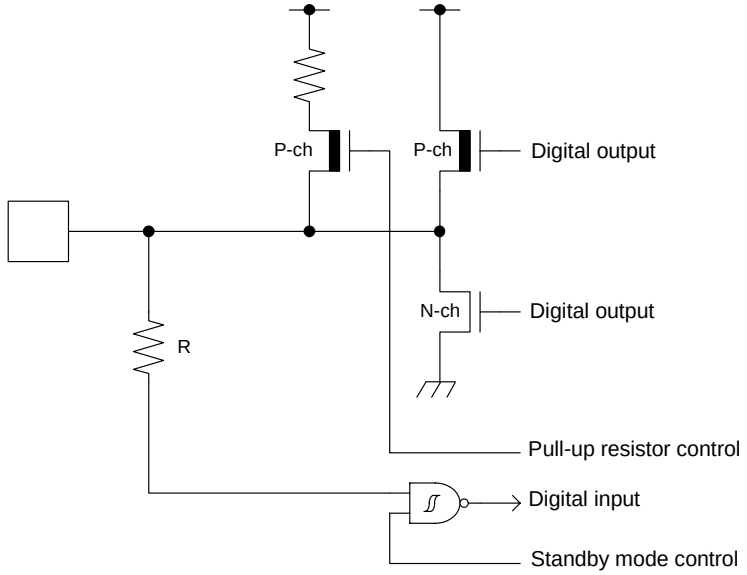
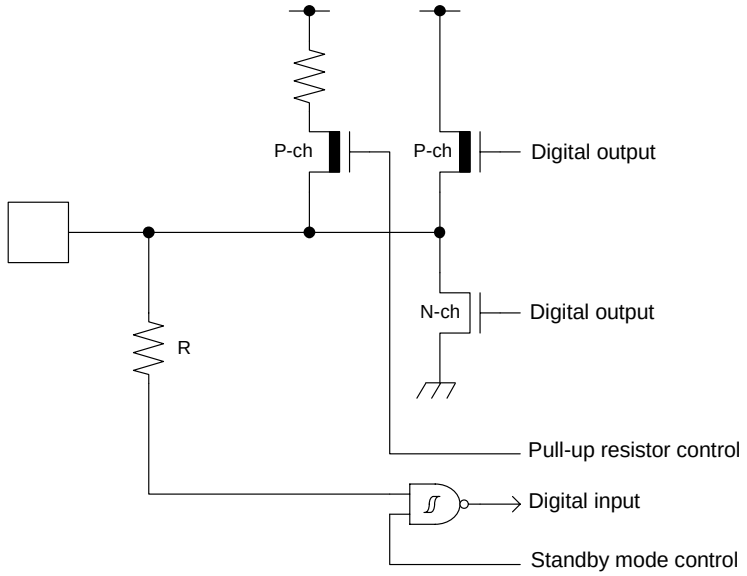
Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
61	53	N6	P4B TIOB02_0 IC12_1 ZIN0_1 MADATA01_0	E	I
62	54	M6	P4C TIOB03_0 IC13_1 SCK7_1 AIN1_2 MADATA02_0	E	I
63	55	L6	P4D TIOB04_0 FRCK1_1 SOT7_1 BIN1_2 MADATA03_0	E	I
64	56	K6	P4E TIOB05_0 INT06_2 SIN7_1 ZIN1_2 MADATA04_0	E	H
65	57	J6	P70 TIOA04_2 TX0_0 MADATA05_0	E	I
66	58	N8	P71 INT13_2 TIOB04_2 RX0_0 MADATA06_0	E	H
67	59	M8	P72 SIN2_0 INT14_2 AIN2_0 MADATA07_0	E	H
68	60	L8	P73 SOT2_0 INT15_2 BIN2_0 MADATA08_0	E	H
69	61	K8	P74 SCK2_0 ZIN2_0 MADATA09_0	E	I
70	62	P8	P75 SIN3_0 ADTG_8 INT07_1 MADATA10_0	E	H

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	46	38	N2
	TIOA0_1		38	30	K3
	TIOA0_2		11	11	E3
	TIOB0_0	Base timer ch.0 TIOB pin	59	51	L5
	TIOB0_1		28	-	H3
	TIOB0_2		12	12	E4
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	47	39	N3
	TIOA1_1		39	31	K4
	TIOA1_2		16	16	F3
	TIOB1_0	Base timer ch.1 TIOB pin	60	52	K5
	TIOB1_1		29	-	H4
	TIOB1_2		17	17	F4
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	48	40	M3
	TIOA2_1		40	32	L1
	TIOA2_2		169	139	C5
	TIOB2_0	Base timer ch.2 TIOB pin	61	53	N6
	TIOB2_1		30	-	H5
	TIOB2_2		168	138	B5
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	49	41	L4
	TIOA3_1		41	33	L2
	TIOA3_2		165	135	C6
	TIOB3_0	Base timer ch.3 TIOB pin	62	54	M6
	TIOB3_1		31	-	H6
	TIOB3_2		166	136	D6
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	50	42	M4
	TIOA4_1		42	34	L3
	TIOA4_2		65	57	J6
	TIOB4_0	Base timer ch.4 TIOB pin	63	55	L6
	TIOB4_1		32	-	J5
	TIOB4_2		66	58	N8
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	51	43	N4
	TIOA5_1		43	35	M2
	TIOA5_2		8	8	D3
	TIOB5_0	Base timer ch.5 TIOB pin	64	56	K6
	TIOB5_1		33	-	J4
	TIOB5_2		9	9	D4
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	170	-	B4
	TIOA6_1		148	118	E9
	TIOA6_2		25	-	H1
	TIOB6_0	Base timer ch.6 TIOB pin	171	-	C4
	TIOB6_1		161	131	D7
	TIOB6_2		26	-	H2

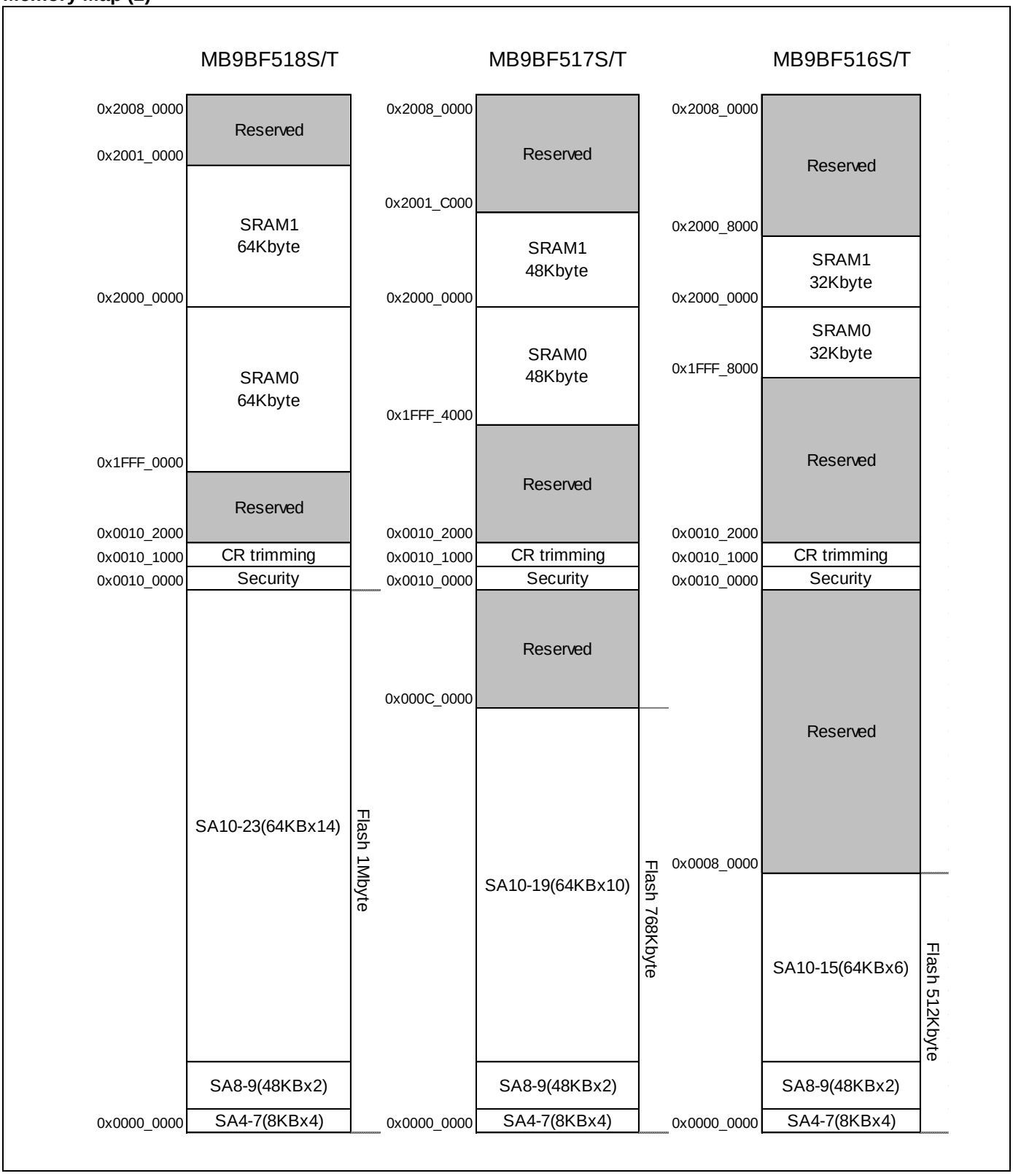
5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
K		• CMOS level output • TTL level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
L		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Memory Map (2)


MB9BF518S/T
MB9BF517S/T
MB9BF516S/T
0x2008_0000
Reserved
0x2001_0000
SRAM1
64Kbyte
0x2000_0000
SRAM0
64Kbyte
0x1FFF_0000
Reserved
0x0010_2000
CR trimming
0x0010_1000
Security
0x0010_0000
SA10-23(64KBx14)
SA8-9(48KBx2)
SA4-7(8KBx4)
0x0000_0000
Flash 1Mbyte
0x2001_C000
SRAM1
48Kbyte
SRAM0
48Kbyte
0x1FFF_4000
0x000C_0000
SA10-19(64KBx10)
Flash 768Kbyte
0x2000_8000
SRAM1
32Kbyte
SRAM0
32Kbyte
0x1FFF_8000
0x0008_0000
SA10-15(64KBx6)
Flash 512Kbyte

List of Pin Status

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"/ or Input enable	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop*1 Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop*1 Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

12.4 AC Characteristics

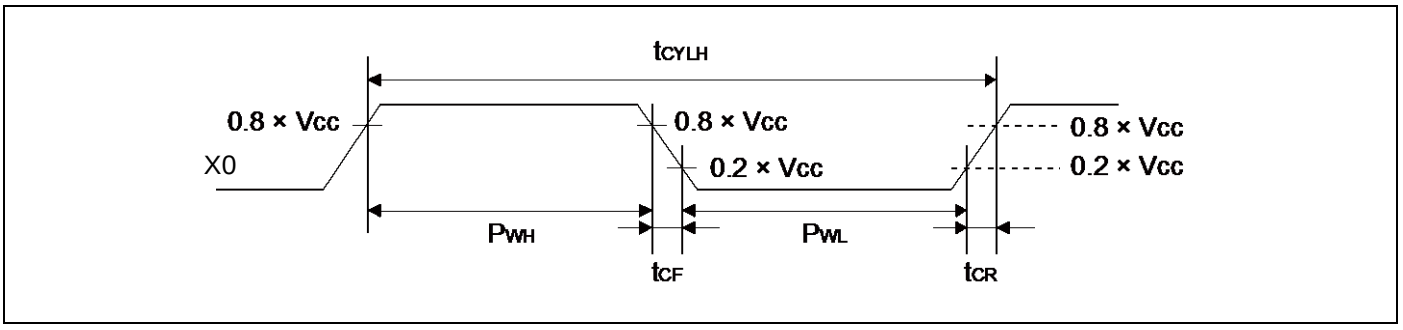
12.4.1 Main Clock Input Characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	Vcc ≥ 4.5 V	4	50	MHz	When crystal oscillator is connected
			Vcc < 4.5 V	4	20		
			Vcc ≥ 4.5 V	4	50	MHz	When using external clock
			Vcc < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		Vcc ≥ 4.5 V	20	250	ns	When using external clock
			Vcc < 4.5 V	50	250		
Input clock pulse width	-		PWH/tCYLH, PWL/tCYLH	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	144	MHz	Master clock
	F_{CC}	-	-	-	144	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	72	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	72	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	72	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	6.94	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	13.8	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	13.8	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	13.8	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter 2-1:Clock" in "FM3 Family Peripheral Manual".

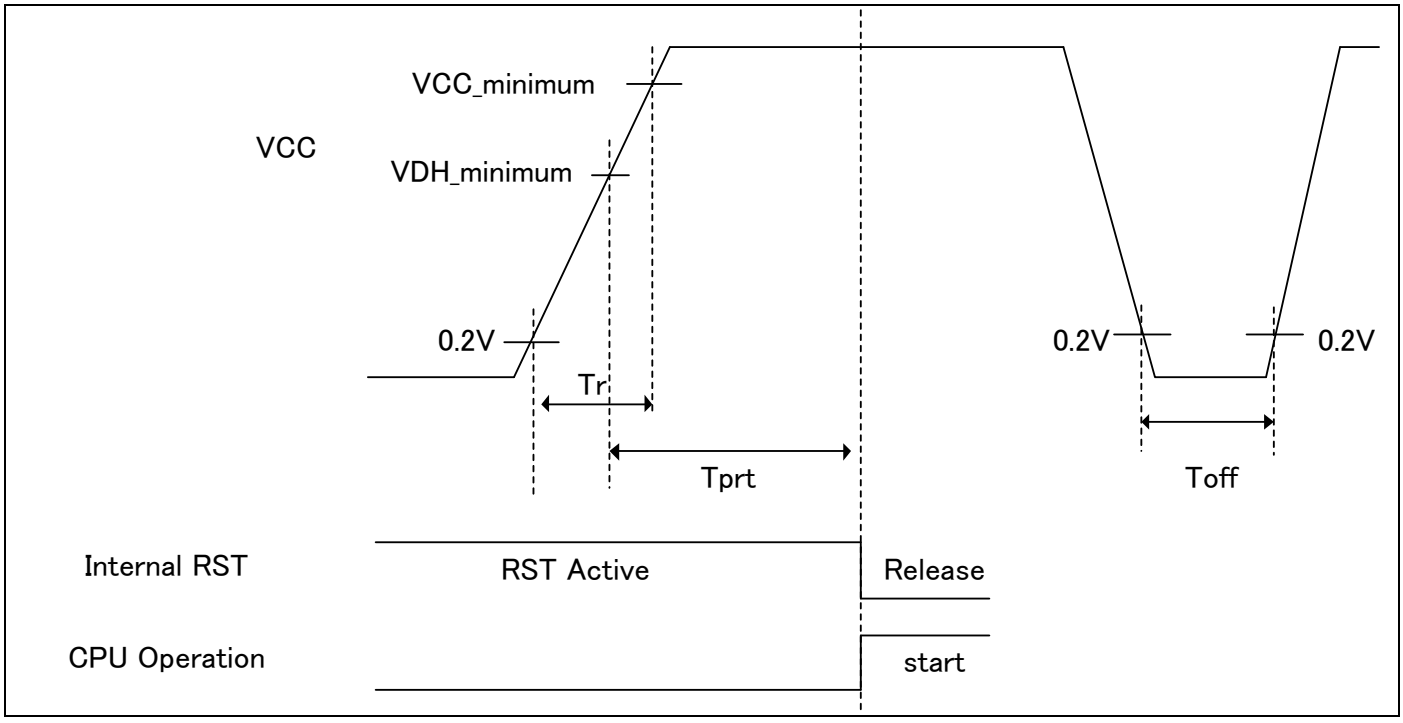
*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this datasheet.



12.4.7 Power-on Reset Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	VCC	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.46	0.76	ms	



Glossary

VCC_minimum : Minimum V_{CC} of recommended operating conditions

VDH_minimum : Minimum release voltage of Low-Voltage detection reset.
See "12.7. Low-Voltage Detection Characteristics"

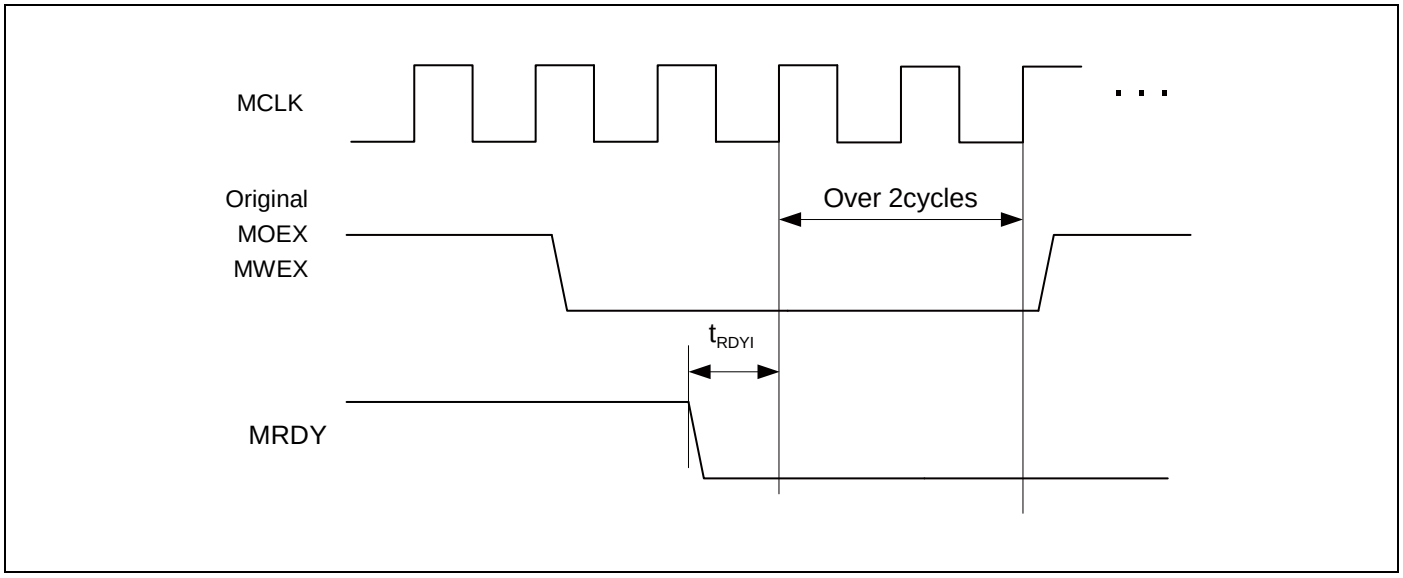
Separate Bus Access Asynchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

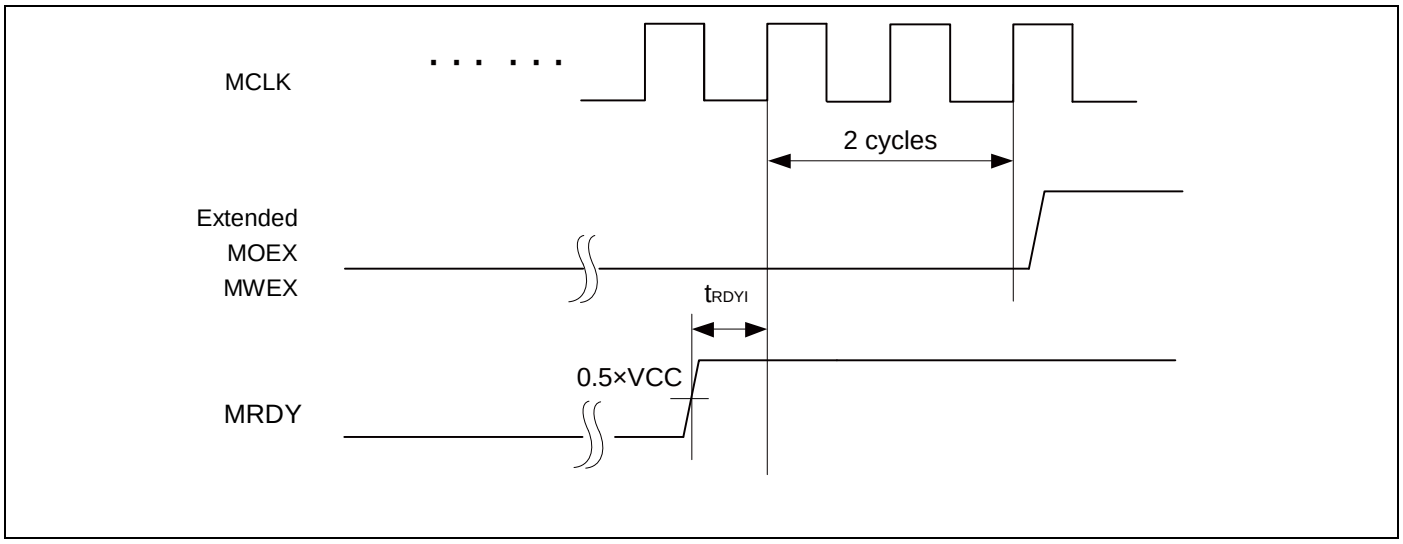
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MCSX ↓ → Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	Vcc ≥ 4.5 V	-9	+9	ns
			Vcc < 4.5 V	-12	+12	
MOEX ↑ → Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	20	-	ns
			Vcc < 4.5 V	38	-	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX Min pulse width	t_{WEW}	MWEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MWEX ↑ → Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MCSX ↓ → Data output time	t_{CSL-DV}	MCSX, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK-9	MCLK+9	ns
			Vcc < 4.5 V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	

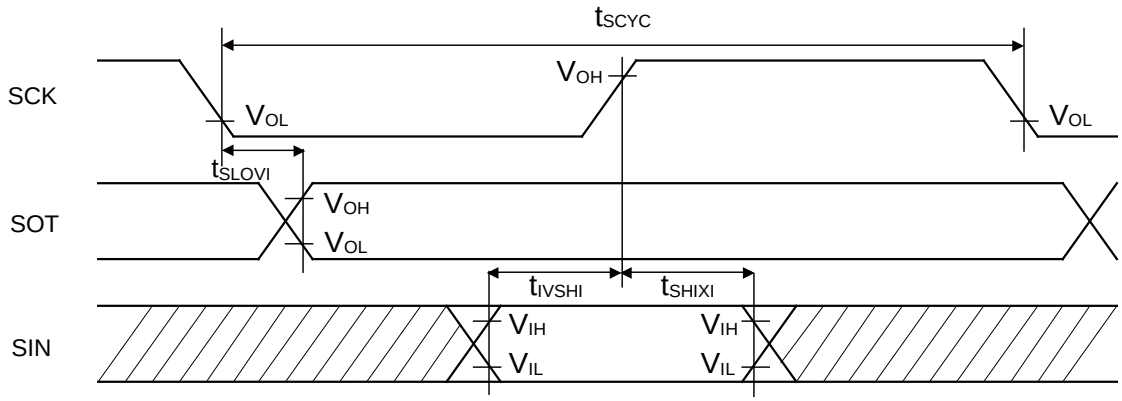
Note: When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)

When RDY is input

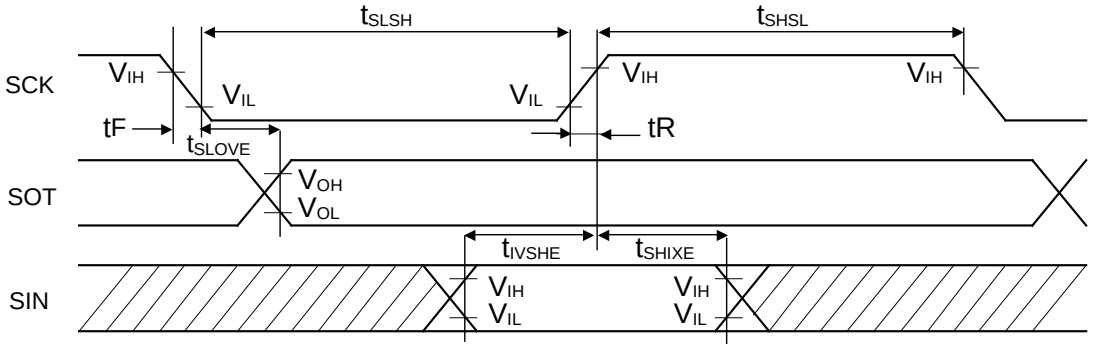


When RDY is released





Master mode



Slave mode

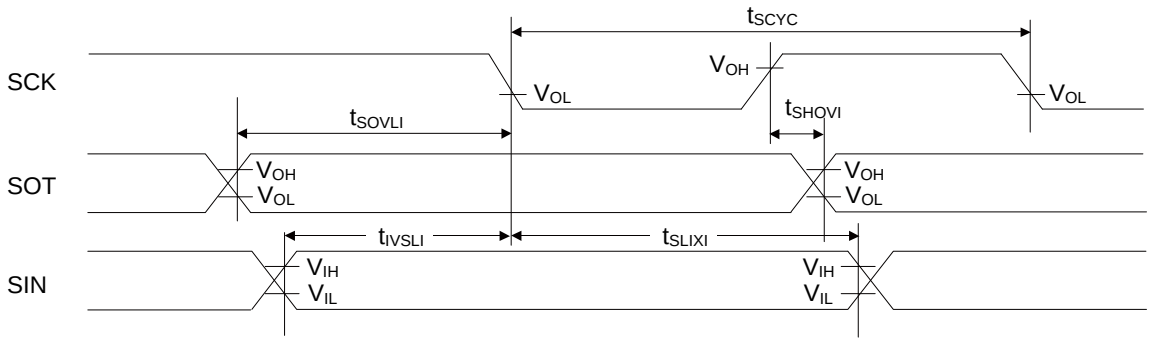
CSIO (SPI = 1, SCINV = 0)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

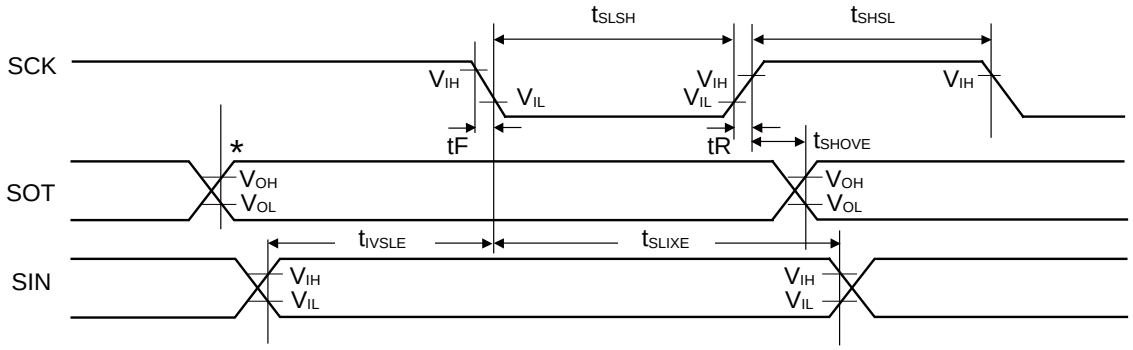
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance = 30 pF.



Master mode



Slave mode

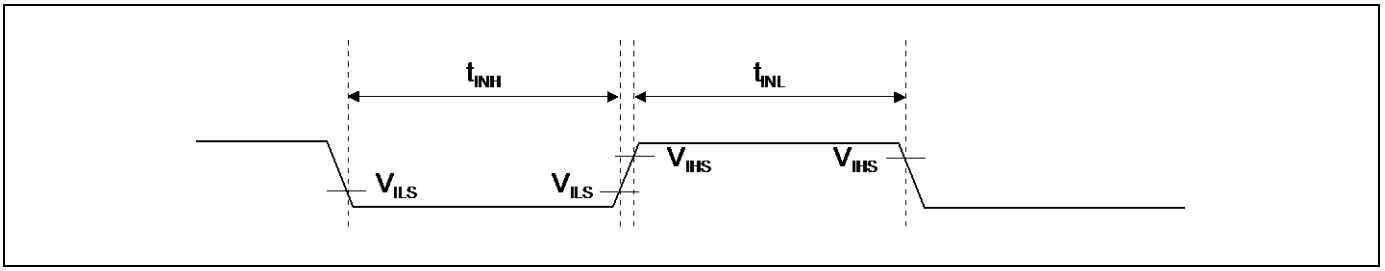
*: Changes when writing to TDR register

12.4.11 External Input Timing

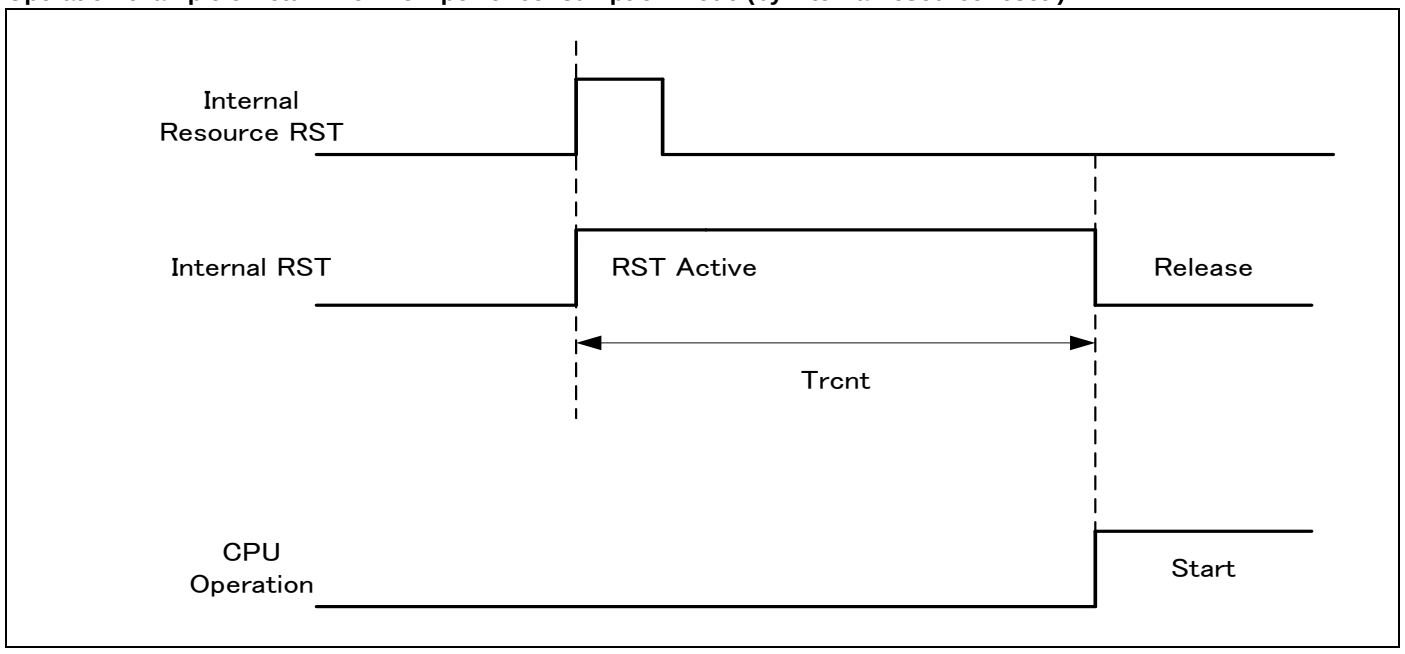
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*	-	ns	Wave form generator
		INTxx, NMIX	Except Timer mode, Stop mode	$2t_{CYCP}$ + 100*	-	ns	External interrupt NMI
			Timer mode, Stop mode	500	-	ns	

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "8. Block Diagram" in this datasheet.



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
  See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".
- The time during the power-on reset/low-voltage detection reset is excluded. See “12.4.3. Internal CR Oscillation Characteristics in 12.4. AC Characteristics in 12. Electrical Characteristics” for the detail on the time during the power-on reset/low -voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.