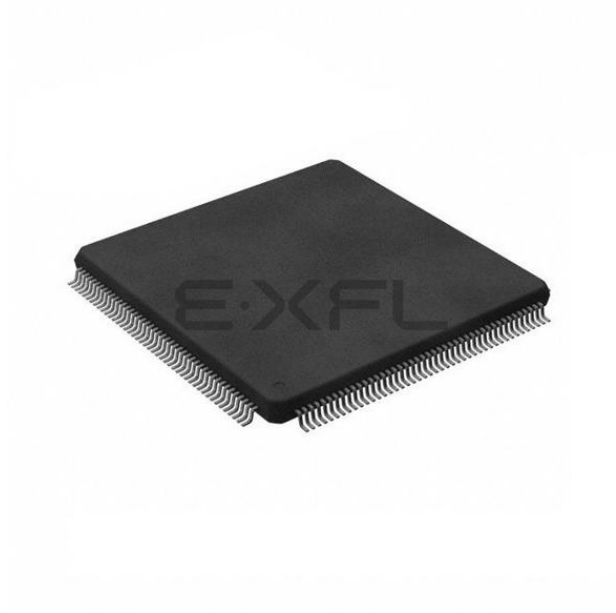


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	154
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf517tpmc-gk7e1

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activation compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from power saving mode.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 32 external interrupt input pin
- Include one non-maskable interrupt(NMI)

Watch dog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- High-speed internal CR Clock : 4 MHz
- Low-speed internal CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

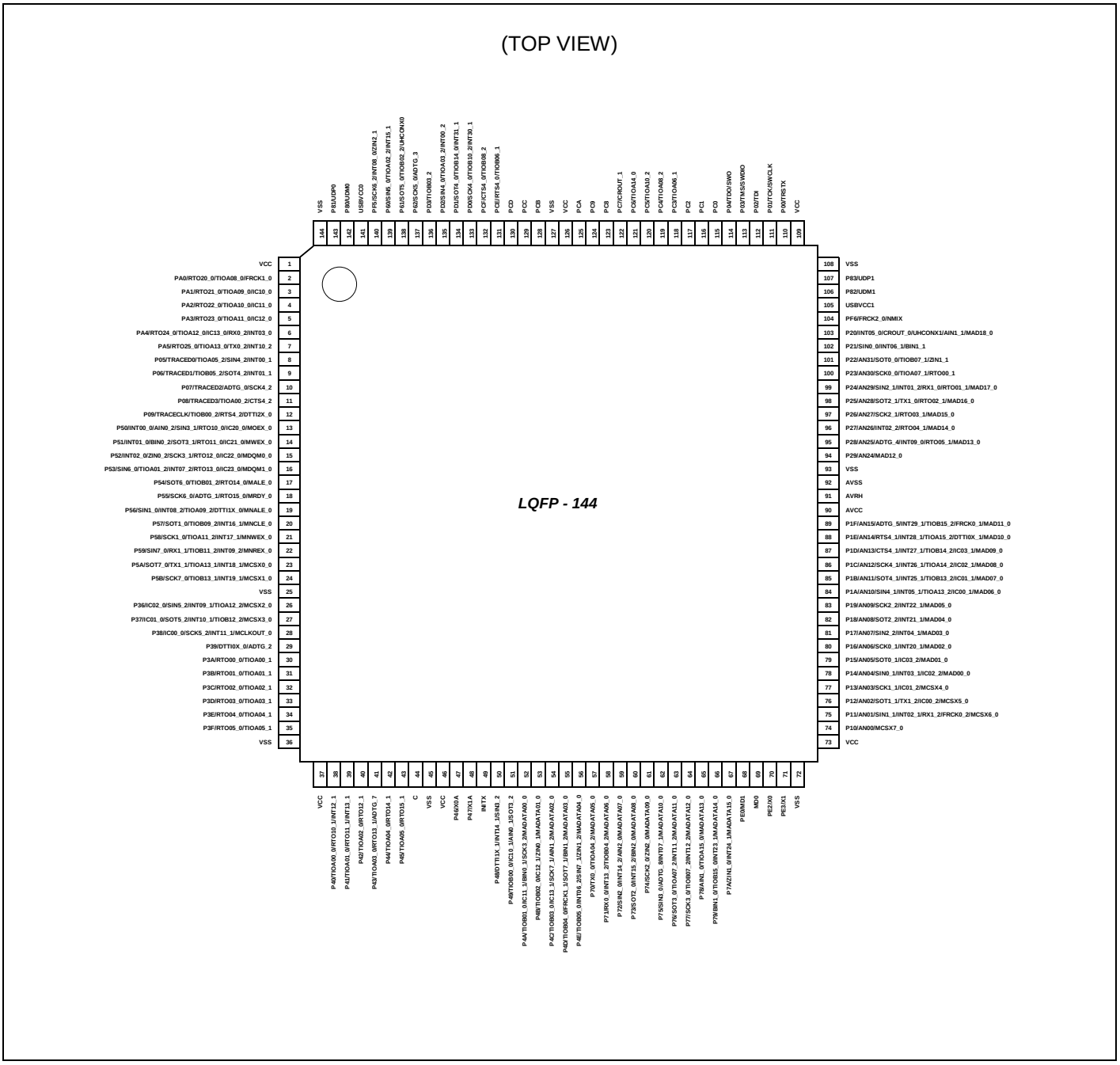
2. Packages

Package \ Product name	MB9BF516S MB9BF517S MB9BF518S	MB9BF516T MB9BF517T MB9BF518T
LQFP: FPT-144P-M08 (0.5 mm pitch)	○	-
LQFP: FPT-176P-M07 (0.5 mm pitch)	-	○
BGA: BGA-192P-M06 (0.8 mm pitch)	-	○

○: Supported

Note: See "14. Package Dimensions" for detailed information on each package.

FPT-144P-M08



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

TIOA09_0 and TIOA09_2 cannot be used as the external startup trigger input (TGIN signal) at I/O mode 1 (timer full mode) of the Base Timer. See "Base Timer" in "7. Handling Devices" for details.

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
117	-	G9	PB7 AN23 TIOB12_1 INT23_0 ZIN2_2	F	L
118	94	F10	P29 AN24 MAD12_0	F	K
119	95	F11	P28 AN25 ADTG_4 INT09_0 RTO05_1 MAD13_0	F	L
120	96	F12	P27 AN26 INT02_2 RTO04_1 MAD14_0	F	L
121	97	F13	P26 AN27 SCK2_1 RTO03_1 MAD15_0	F	K
122	98	E10	P25 AN28 SOT2_1 TX1_0 RTO02_1 MAD16_0	F	K
123	99	E11	P24 AN29 SIN2_1 RX1_0 INT01_2 RTO01_1 MAD17_0	F	L
124	100	E12	P23 AN30 SCK0_0 TIOA07_1 RTO00_1	F	K
125	101	E13	P22 AN31 SOT0_0 TIOB07_1 ZIN1_1	F	K
126	102	D12	P21 SIN0_0 INT06_1 BIN1_1	E	H

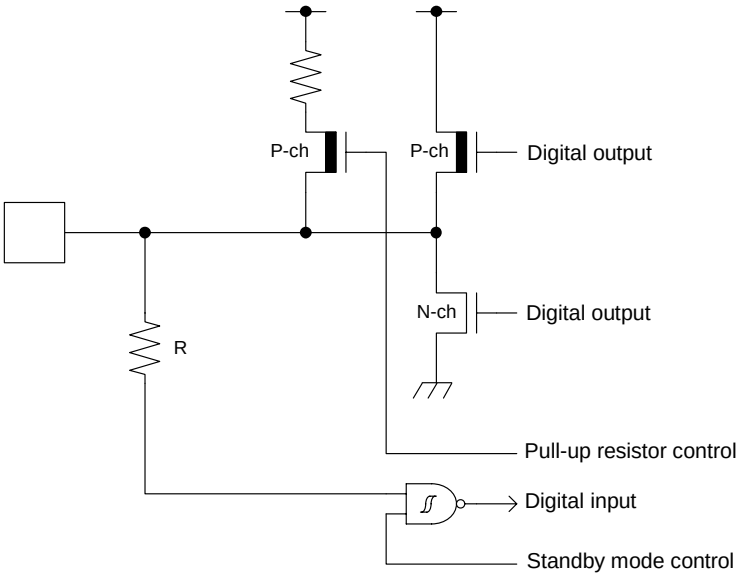
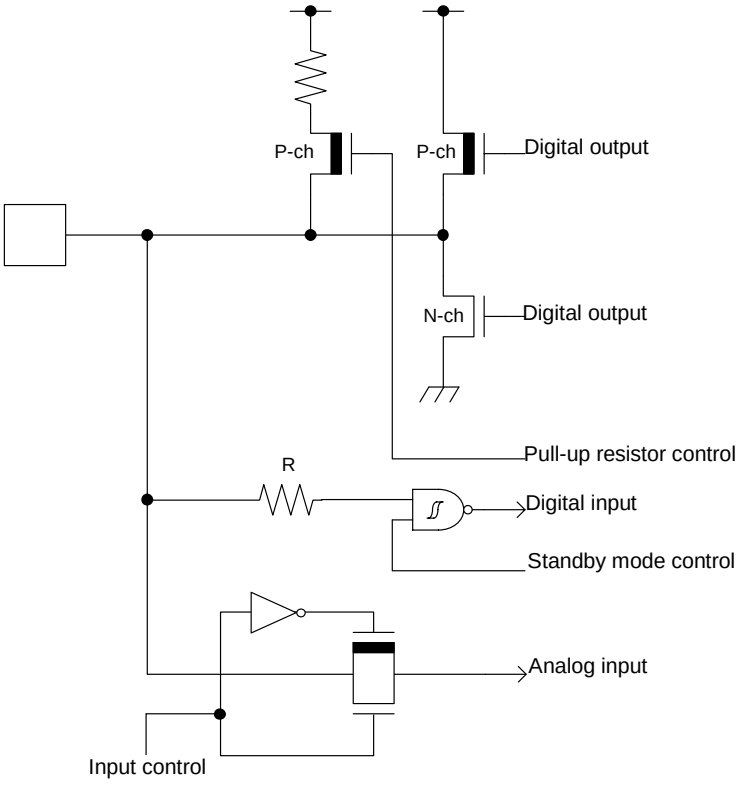
Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
143	-	D10	P94 TIOB12_0 RTO24_1 SCK5_1 INT26_0 MAD23_0	E	H
144	-	B9	P95 TIOB13_0 RTO25_1 INT27_0 MAD24_0	E	H
145	115	C9	PC0	K	Q
146	116	B8	PC1	K	Q
147	117	D9	PC2	K	Q
148	118	E9	PC3 TIOA06_1	K	Q
149	119	F9	PC4 TIOA08_2	K	Q
150	120	C8	PC5 TIOA10_2	K	Q
-	-	A5	VSS	-	
151	121	D8	PC6 TIOA14_0	K	Q
152	122	E8	PC7 CROUT_1	L	Q
153	123	A10	PC8	K	Q
154	124	F8	PC9	K	Q
155	125	B7	PCA	K	Q
156	126	A9	VCC	-	
157	127	A11	VSS	-	
158	128	A7	PCB	L	Q
159	129	C7	PCC	K	Q
160	130	A6	PCD	K	Q
161	131	D7	PCE RTS4_0 TIOB06_1	L	Q
162	132	E7	PCF CTS4_0 TIOB08_2	L	Q
163	133	F7	PD0 SCK4_0 TIOB10_2 INT30_1	L	R
164	134	B6	PD1 SOT4_0 TIOB14_0 INT31_1	L	R
-	-	N7	VSS	-	
-	-	G8	VSS	-	
-	-	H7	VSS	-	
-	-	H8	VSS	-	

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 14	TIOA14_0	Base timer ch.14 TIOA pin	151	121	D8
	TIOA14_1		78	-	N10
	TIOA14_2		102	86	J10
	TIOB14_0	Base timer ch.14 TIOB pin	164	134	B6
	TIOB14_1		79	-	L10
	TIOB14_2		103	87	J9
Base Timer 15	TIOA15_0	Base timer ch.15 TIOA pin	73	65	N9
	TIOA15_1		80	-	K10
	TIOA15_2		104	88	H10
	TIOB15_0	Base timer ch.15 TIOB pin	74	66	M9
	TIOB15_1		81	-	M10
	TIOB15_2		105	89	H9
CAN 0	TX0_0	CAN interface ch.0 TX output	65	57	J6
	TX0_1		32	-	J5
	TX0_2		7	7	D1
	RX0_0	CAN interface ch.0 RX output	66	58	N8
	RX0_1		33	-	J4
	RX0_2		6	6	D2
CAN 1	TX1_0	CAN interface ch.1 TX output	122	98	E10
	TX1_1		23	23	G5
	TX1_2		92	76	L13
	RX1_0	CAN interface ch.1 RX output	123	99	E11
	RX1_1		22	22	G4
	RX1_2		91	75	M12
Debugger	SWCLK	Serial wire debug interface clock input	135	111	A12
	SWDIO	Serial wire debug interface data input / output	137	113	B12
	SWO	Serial wire viewer output	138	114	B11
	TCK	J-TAG test clock input	135	111	A12
	TDI	J-TAG test data input	136	112	C12
	TDO	J-TAG debug data output	138	114	B11
	TMS	J-TAG test mode state input/output	137	113	B12
	TRACECLK	Trace CLK output of ETM	12	12	E4
	TRACED0	Trace data output of ETM	8	8	D3
	TRACED1		9	9	D4
	TRACED2		10	10	E2
	TRACED3		11	11	E3
	TRSTX	J-TAG test reset Input	134	110	B13

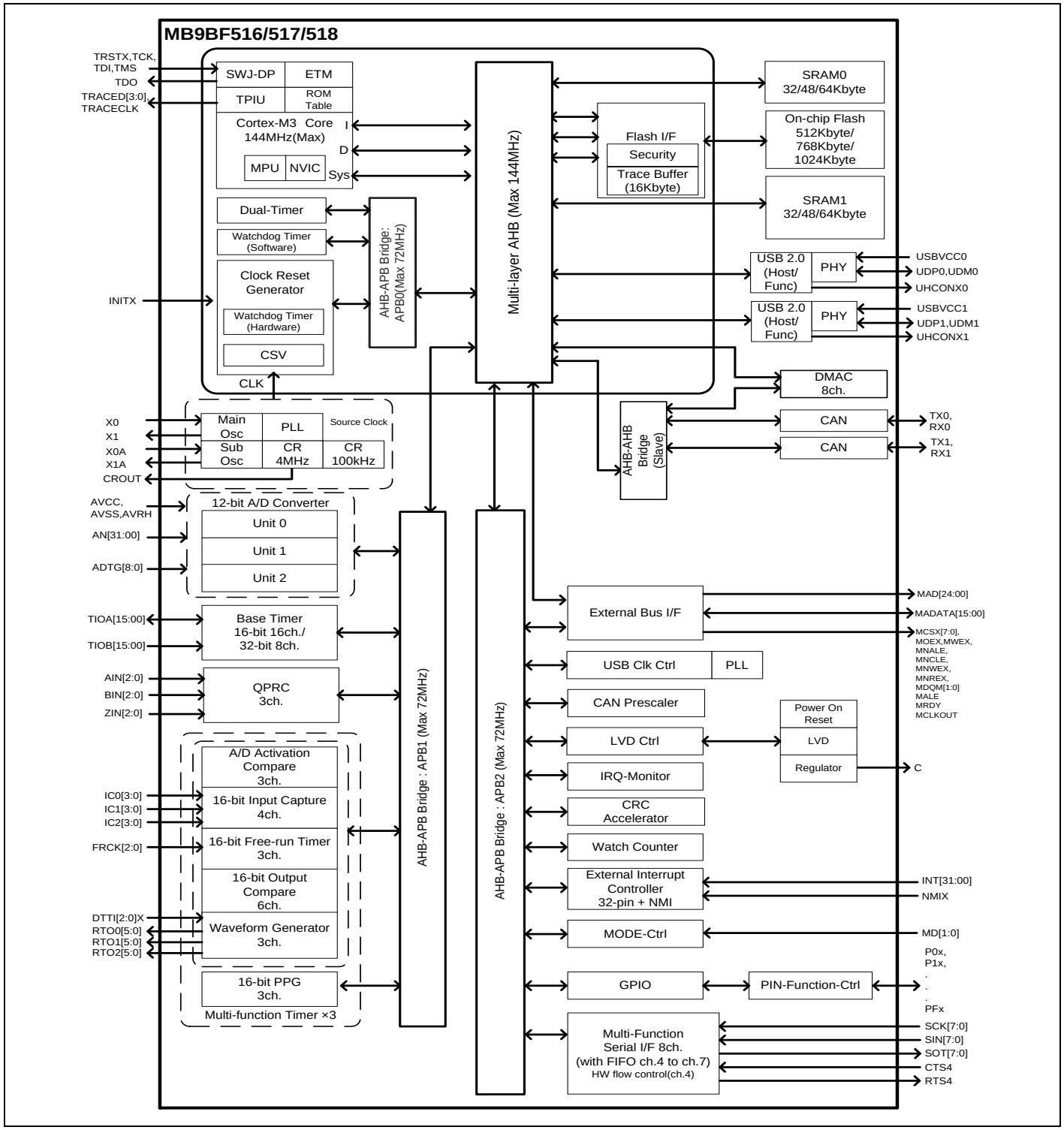
Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin	16	16	F3
	SIN6_1		31	-	H6
	SIN6_2		170	-	B4
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	17	17	F4
	SOT6_1 (SDA6_1)		30	-	H5
	SOT6_2 (SDA6_2)		171	-	C4
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	18	18	F5
	SCK6_1 (SCL6_1)		29	-	H4
	SCK6_2 (SCL6_2)		172	140	B3
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin	22	22	G4
	SIN7_1		64	56	K6
	SIN7_2		110	-	H13
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	23	23	G5
	SOT7_1 (SDA7_1)		63	55	L6
	SOT7_2 (SDA7_2)		111	-	H12
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	24	24	G6
	SCK7_1 (SCL7_1)		62	54	M6
	SCK7_2 (SCL7_2)		112	-	H11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Timer 2	DTTI2X_0	Input signal controlling wave form generator outputs RTO20 to RTO25 of multi-function timer 2.	12	12	E4
	DTTI2X_1		26	-	H2
	FRCK2_0	16-bit free-run timer ch.2 external clock input pin	128	104	C13
	FRCK2_1		78	-	N10
	IC20_0	16-bit input capture ch.2 input pin of multi-function timer 2. ICxx describes channel number.	13	13	E5
	IC20_1		25	-	H1
	IC21_0		14	14	F1
	IC21_1		79	-	L10
	IC22_0		15	15	F2
	IC22_1		80	-	K10
	IC23_0		16	16	F3
	IC23_1		81	-	M10
	RTO20_0 (PPG20_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	B2
	RTO20_1 (PPG20_1)		139	-	C11
	RTO21_0 (PPG20_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	C2
	RTO21_1 (PPG20_1)		140	-	D11
	RTO22_0 (PPG22_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	C3
	RTO22_1 (PPG22_1)		141	-	B10
	RTO23_0 (PPG22_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	D5
	RTO23_1 (PPG22_1)		142	-	C10
	RTO24_0 (PPG24_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	D2
	RTO24_1 (PPG24_1)		143	-	D10
	RTO25_0 (PPG24_0)	Wave form generator output of multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	D1
	RTO25_1 (PPG24_1)		144	-	B9

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
RESET	INITX	External Reset Input. A reset is valid when INITX="L".	57	49	N5
Mode	MD0	Mode 0 Pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	85	69	N12
	MD1	Mode 1 Pin. During serial programming to Flash memory, MD1="L" must be input.	84	68	N13
POWER	VCC	Power supply Pin	1	1	C1
	VCC	Power supply Pin	45	37	N1
	VCC	Power supply Pin	54	46	P4
	VCC	Power supply Pin	89	73	M14
	VCC	Power supply Pin	133	109	A13
	USBVCC0	3.3V Power supply port for USB I/O	173	141	A4
	USBVCC1		129	105	E14
	VCC	Power supply Pin	156	126	A9
GND	VSS	GND Pin	27	25	J1
	VSS	GND Pin	44	36	M1
	VSS	GND Pin	53	45	P3
	VSS	GND Pin	88	72	N14
	VSS	GND Pin	109	93	F14
	VSS	GND Pin	132	108	B14
	VSS	GND Pin	157	127	A11
	VSS	GND Pin	176	144	B1
	VSS	GND Pin	-	-	E1
	VSS	GND Pin	-	-	G1
	VSS	GND Pin	-	-	P7
	VSS	GND Pin	-	-	P11
	VSS	GND Pin	-	-	L14
	VSS	GND Pin	-	-	A8
	VSS	GND Pin	-	-	A5
	VSS	GND Pin	-	-	N7
	VSS	GND Pin	-	-	M7
	VSS	GND Pin	-	-	L7
	VSS	GND Pin	-	-	K7
	VSS	GND Pin	-	-	J7
	VSS	GND Pin	-	-	G7
	VSS	GND Pin	-	-	H7
	VSS	GND Pin	-	-	H8
	VSS	GND Pin	-	-	G8

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

8. Block Diagram



Note: The following items vary depending on the package.

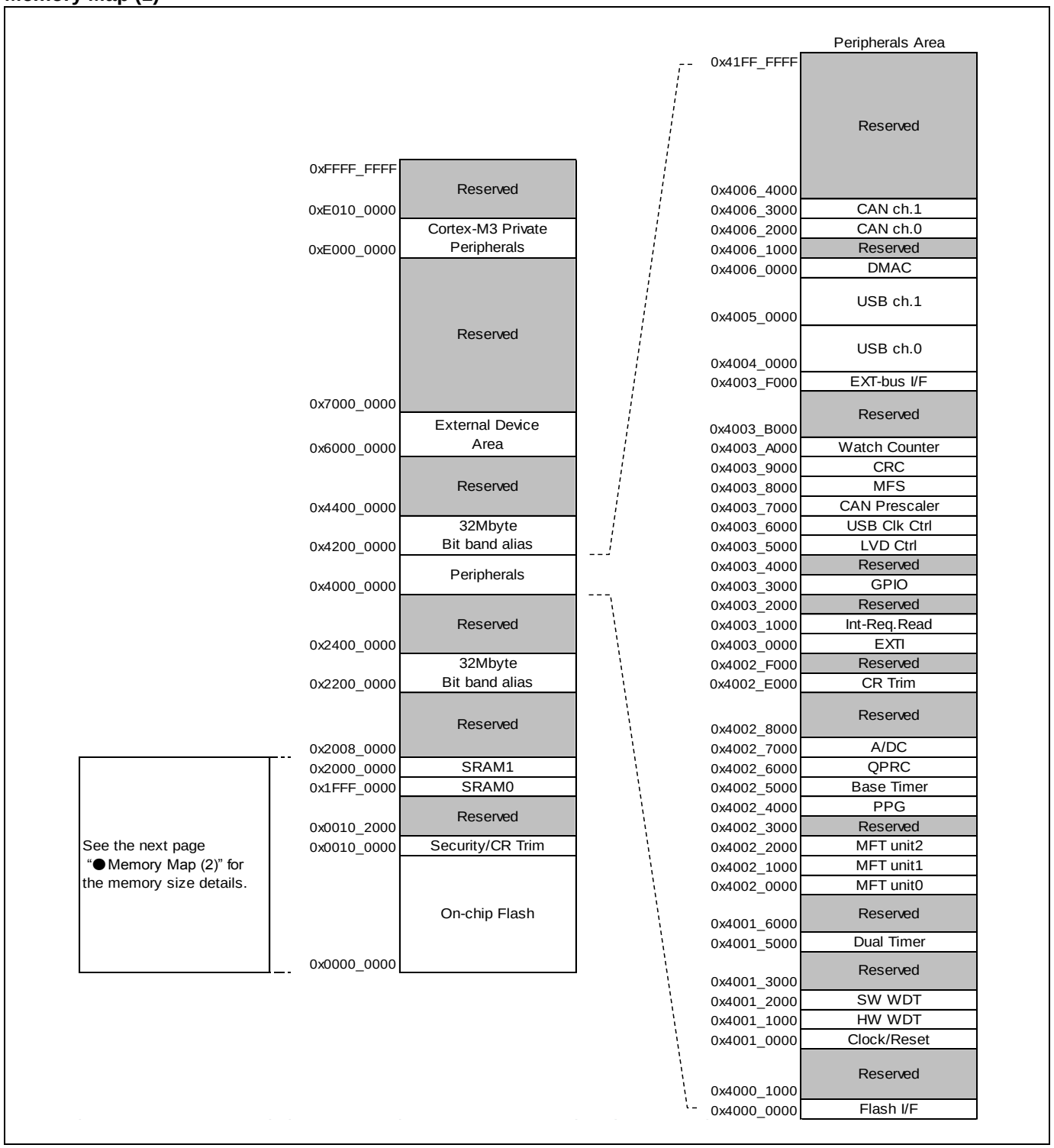
- Number of external bus interface pin
- Number of 12-bit A/D converter channel

9. Memory Size

See "Memory Size" in "1. Product Lineup" to confirm the memory size.

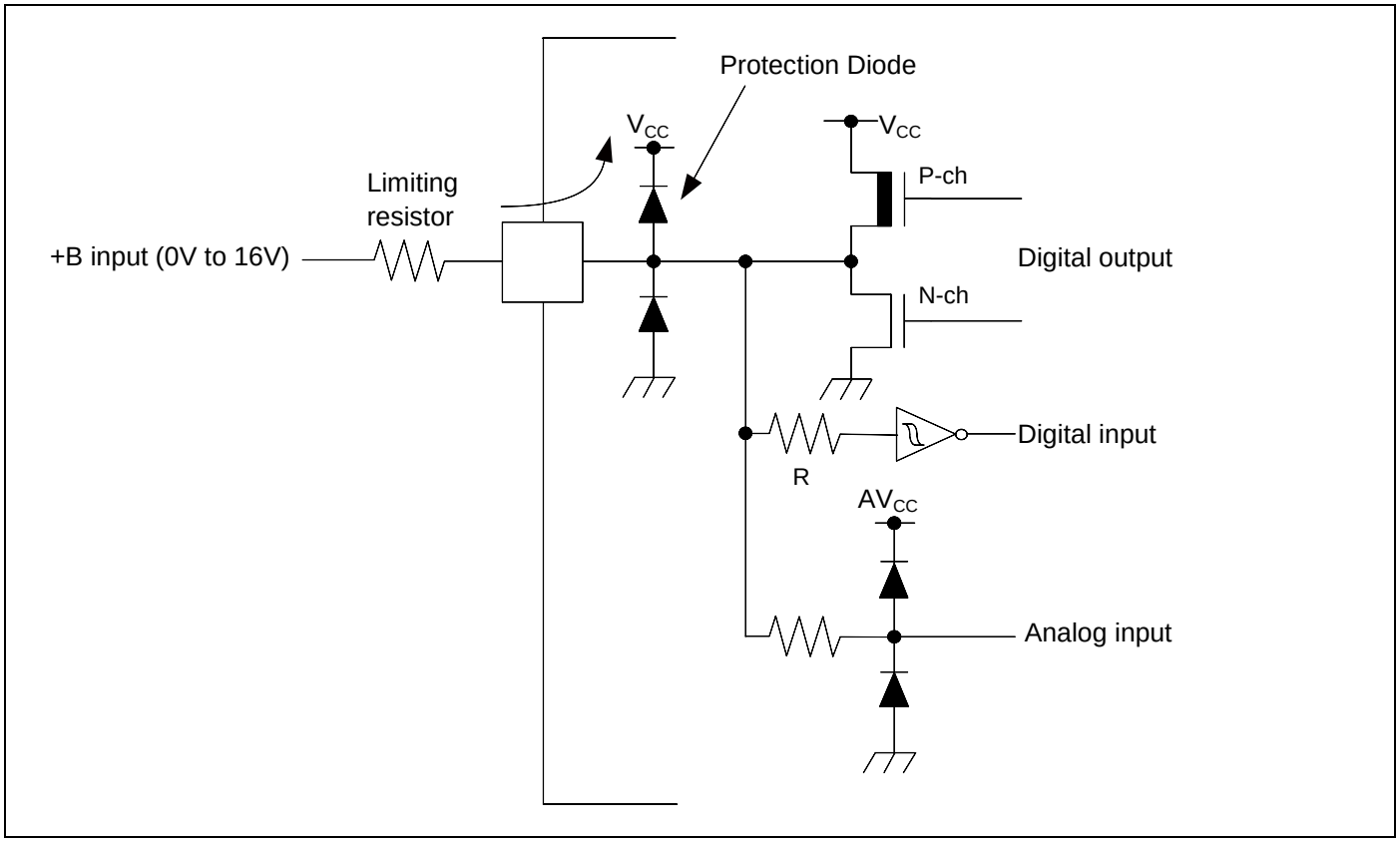
10. Memory Map

Memory Map (1)



*8:

- See "4. List of Pin Functions" and "5. I/O Circuit Type" about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



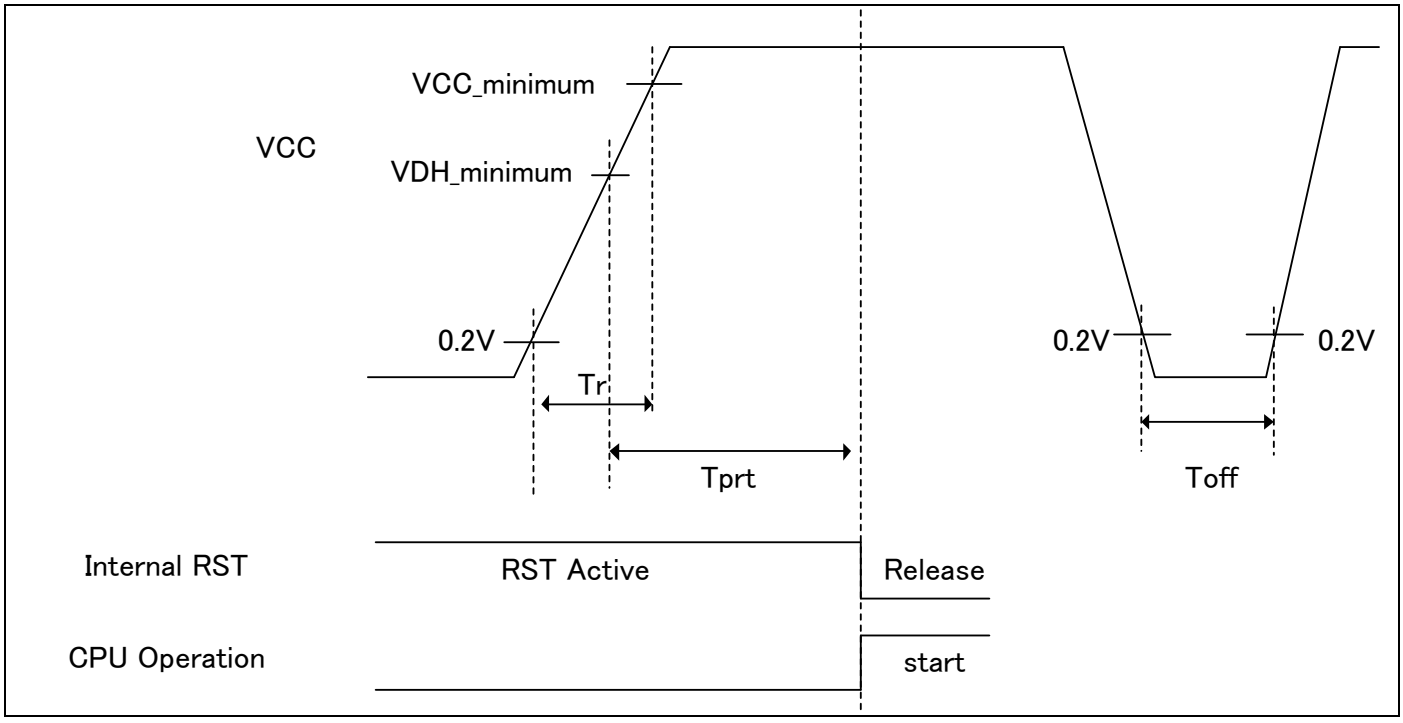
WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

12.4.7 Power-on Reset Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	VCC	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.46	0.76	ms	



Glossary

VCC_minimum : Minimum V_{CC} of recommended operating conditions

VDH_minimum : Minimum release voltage of Low-Voltage detection reset.
See "12.7. Low-Voltage Detection Characteristics"

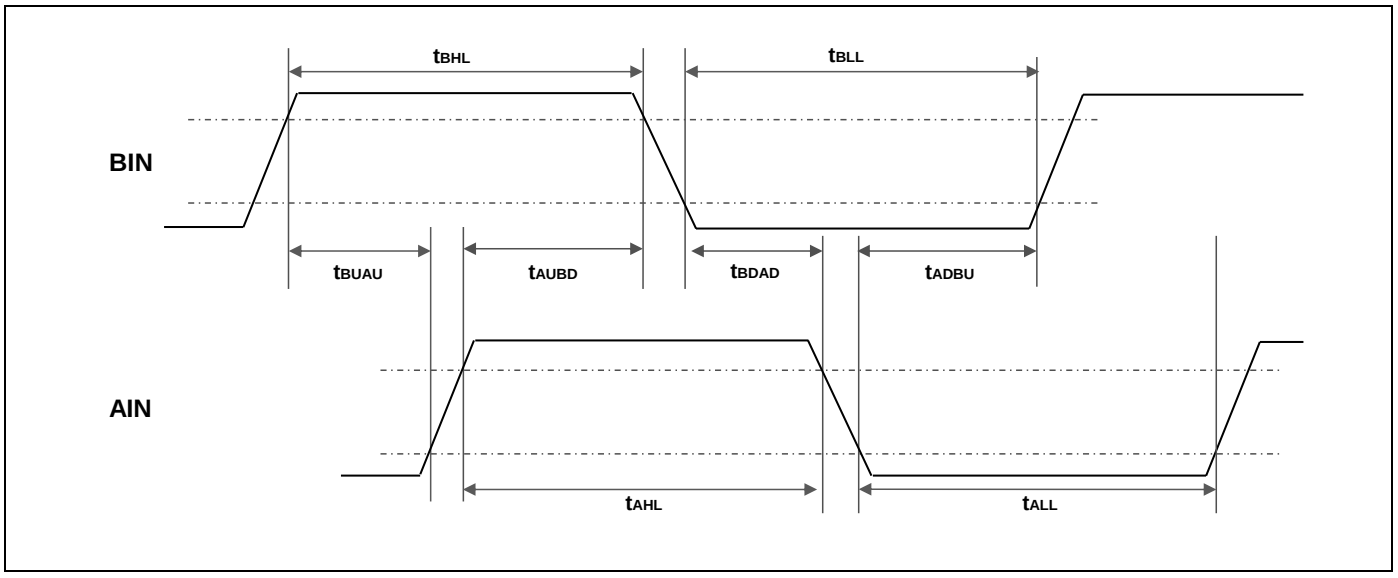
CSIO (SPI = 1, SCINV = 0)

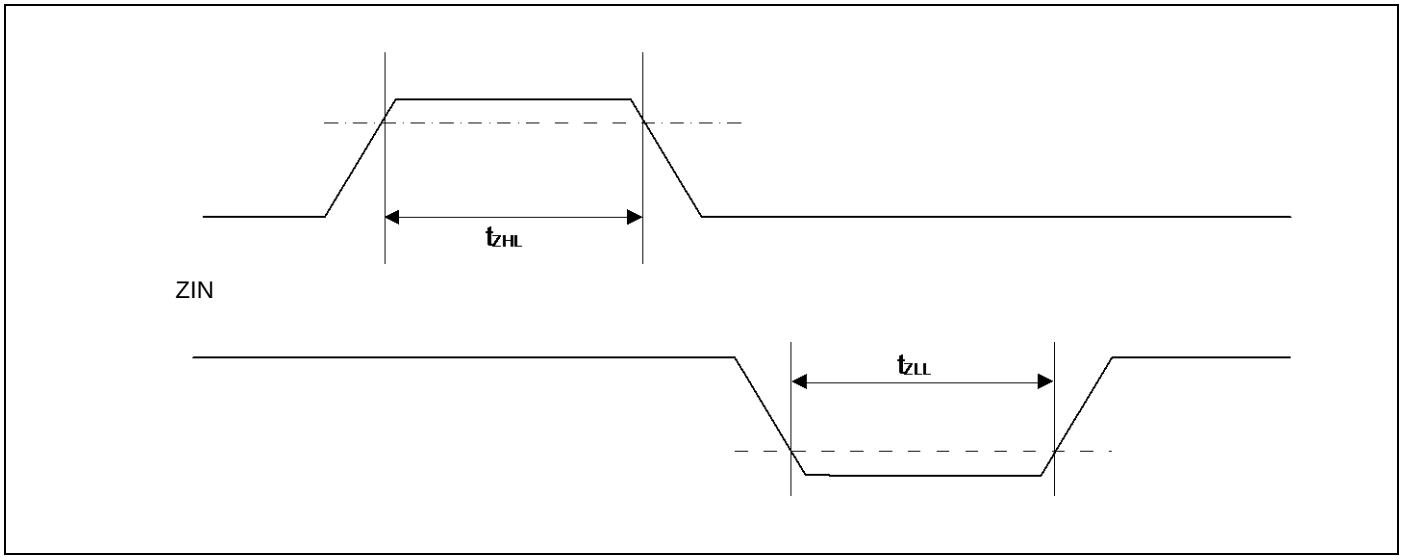
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

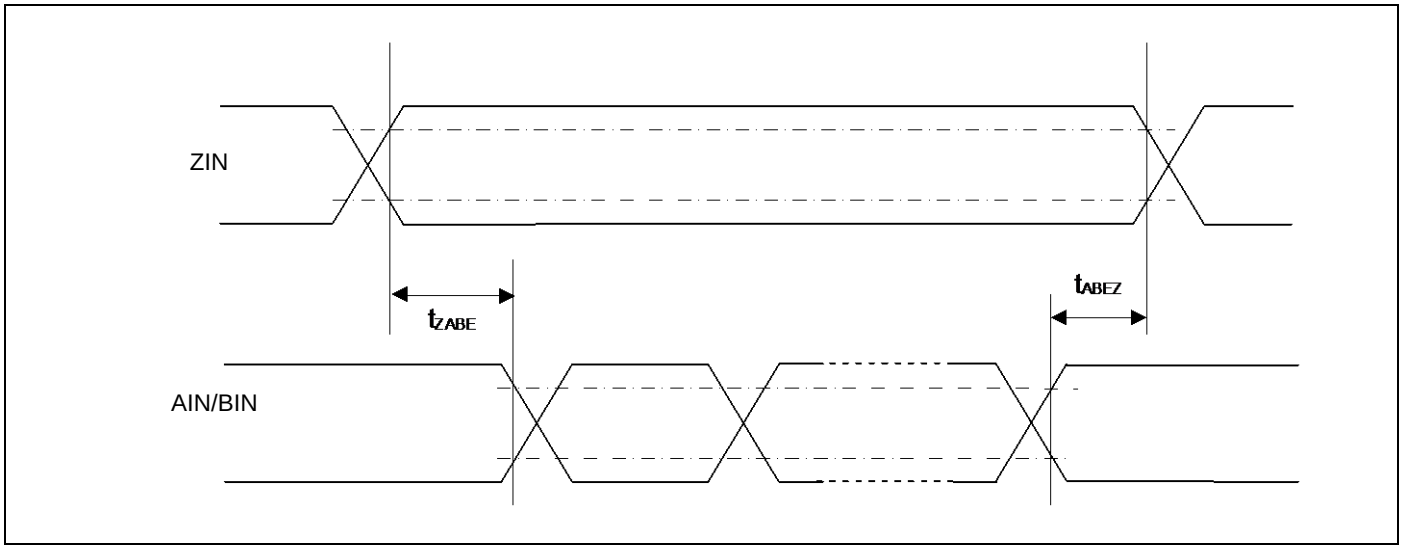
Parameter	Symbol	Pin name	Conditions	Vcc < 4.5 V		Vcc ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance = 30 pF.


tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL

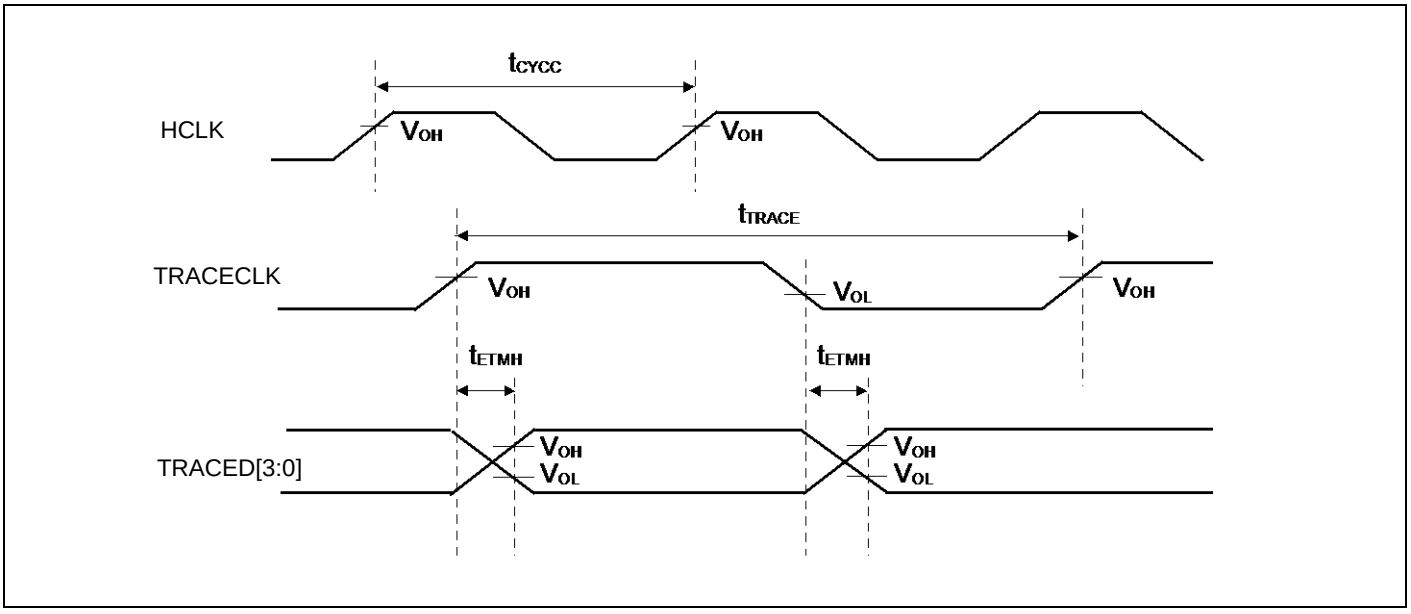

ZIN
tZABE
tABEZ
AIN/BIN

12.4.14 ETM Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	Vcc ≥ 4.5 V	2	9	ns	
			Vcc < 4.5 V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	Vcc ≥ 4.5 V	-	50	MHz	
			Vcc < 4.5 V	-	32	MHz	
TRACECLK cycle time	t_{TRACE}		Vcc ≥ 4.5 V	20	-	ns	
			Vcc < 4.5 V	31.25	-	ns	

Note: When the external load capacitance = 30 pF.



12.6 USB characteristics

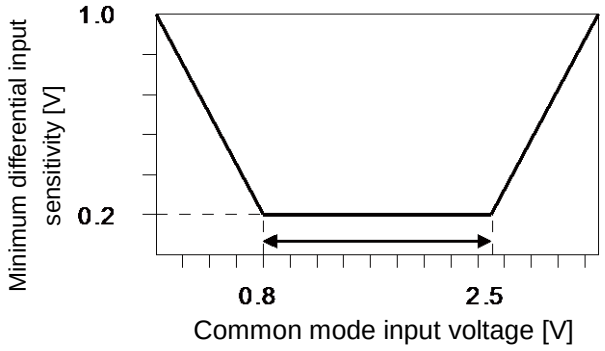
The USB characteristics of ch.0 and those of ch.1 are the same.
USBVcc0 and USBVcc1 are described as USBVcc below.

(Vcc = 2.7V to 5.5V, USBVcc = 3.0V to 3.6V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input "H" level voltage	V_{IH}	UDP0, UDM0	-	2.0	USBVcc + 0.3	V	*1
	Input "L" level voltage	V_{IL}		-	Vss - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output "H" level voltage	V_{OH}		External pull-down resistance= 15kΩ	2.8	3.6	V	*3
	Output "L" level voltage	V_{OL}		External pull-up resistance= 1.5kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rise time	t_{FR}		Full-Speed	4	20	ns	*5
	Fall time	t_{FF}		Full-Speed	4	20	ns	*5
	Rise/ fall time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rise time	t_{LR}		Low-Speed	75	300	ns	*7
	Fall time	t_{LF}		Low-Speed	75	300	ns	*7
	Rise/ fall time matching	t_{LRFM}		Low-Speed	80	125	%	*7

*1: The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.



Page	Section	Change Results
116	7. Low-voltage Detection Characteristics (2) Interrupt of Low-voltage Detection	Corrected the value of "LVD stabilization wait time (T_{LVDW})". Max: 2240×tcyc → 4032×t_{CYCP}
117	8. Flash Memory Write/Erase Characteristics Erase/write cycles and data hold time	Deleted "(targeted value)".
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	Features External Bus Interface	Added the description of Maximum area size
2	Features USB Interface	Added the description of PLL for USB
2	Features USB Interface	Added the size of each EndPoint
9, 10	Pin Assignment	Added SWCLK and SWDIO and SWO
51 to 56	I/O Circuit Type	Added the description of I^2C to the type of E, F, I, L Added about +B input
61	Handling Devices	Added "Stabilizing power supply voltage"
61	Handling Devices Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
62	Handling Devices C Pin	Changed the description
64	Block Diagram	Modified the block diagram
66	Memory Map Memory map(1)	Modified the area of "External Device Area"
67	Memory Map Memory map(2)	Added the summary of Flash memory sector and the note
74, 75	Electrical Characteristics 1. Absolute Maximum Ratings	Added the Clamp maximum current Added the output current of P80, P81, P82, P83 Added about +B input
76	Electrical Characteristics 2. Recommended Operation Conditions	Modified the minimum value of Analog reference voltage Added Smoothing capacitor Added the note about less than the minimum power supply voltage
77, 78	Electrical Characteristics 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Added Flash Memory Current Moved A/D Converter Current
82	Electrical Characteristics 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR
84	Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	Added Time until releasing Power-on reset Changed the figure of timing
86 to 88	Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
95 to 102	Electrical Characteristics 4. AC Characteristics (9) CSIO/UART Timing	Modified from UART Timing to CSIO/UART Timing Changed from Internal shift clock operation to Master mode Changed from External shift clock operation to Slave mode
109	Electrical Characteristics 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage Added Conversion time at AVcc < 4.5 V Modified Stage transition time to operation permission Modified the minimum value of Reference voltage
118 to 121	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
122	Ordering Information	Change to full part number

NOTE: Please see "Document History" about later revised information.

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