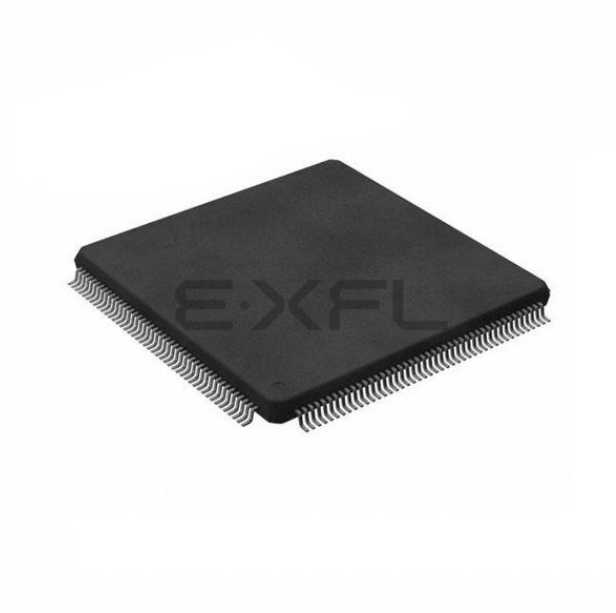

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	154
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf518tpmc-gk7e1

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
11	11	E3	P08 TRACED3 TIOA00_2 CTS4_2	E	G
12	12	E4	P09 TRACECLK TIOB00_2 RTS4_2 DTTI2X_0	E	G
13	13	E5	P50 INT00_0 AIN0_2 SIN3_1 RTO10_0 IC20_0 MOEX_0	E	H
14	14	F1	P51 INT01_0 BIN0_2 SOT3_1 RTO11_0 IC21_0 MWEX_0	E	H
15	15	F2	P52 INT02_0 ZIN0_2 SCK3_1 RTO12_0 IC22_0 MDQM0_0	E	H
16	16	F3	P53 SIN6_0 TIOA01_2 INT07_2 RTO13_0 IC23_0 MDQM1_0	E	H
17	17	F4	P54 SOT6_0 TIOB01_2 RTO14_0 MALE_0	E	I
18	18	F5	P55 SCK6_0 ADTG_1 RTO15_0 MRDY_0	E	I
19	19	F6	P56 SIN1_0 INT08_2 TIOA09_2 DTTI1X_0 MNALE_0	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
31	-	H6	P33 INT04_0 TIOB03_1 SIN6_1 ADTG_6	E	H
32	-	J4	P34 FRCK0_0 TX0_1 TIOB04_1	E	I
33	-	J4	P35 IC03_0 RX0_1 TIOB05_1 INT08_1	E	H
34	26	J3	P36 IC02_0 SIN5_2 INT09_1 TIOA12_2 MCSX2_0	E	H
35	27	J2	P37 IC01_0 SOT5_2 INT10_1 TIOB12_2 MCSX3_0	E	H
36	28	K1	P38 IC00_0 SCK5_2 INT11_1 MCLKOUT_0	E	H
37	29	K2	P39 DTTI0X_0 ADTG_2	E	I
38	30	K3	P3A RTO00_0 TIOA00_1	G	I
39	31	K4	P3B RTO01_0 TIOA01_1	G	I
40	32	L1	P3C RTO02_0 TIOA02_1	G	I
41	33	L2	P3D RTO03_0 TIOA03_1	G	I
42	34	L3	P3E RTO04_0 TIOA04_1	G	I

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
61	53	N6	P4B TIOB02_0 IC12_1 ZIN0_1 MADATA01_0	E	I
62	54	M6	P4C TIOB03_0 IC13_1 SCK7_1 AIN1_2 MADATA02_0	E	I
63	55	L6	P4D TIOB04_0 FRCK1_1 SOT7_1 BIN1_2 MADATA03_0	E	I
64	56	K6	P4E TIOB05_0 INT06_2 SIN7_1 ZIN1_2 MADATA04_0	E	H
65	57	J6	P70 TIOA04_2 TX0_0 MADATA05_0	E	I
66	58	N8	P71 INT13_2 TIOB04_2 RX0_0 MADATA06_0	E	H
67	59	M8	P72 SIN2_0 INT14_2 AIN2_0 MADATA07_0	E	H
68	60	L8	P73 SOT2_0 INT15_2 BIN2_0 MADATA08_0	E	H
69	61	K8	P74 SCK2_0 ZIN2_0 MADATA09_0	E	I
70	62	P8	P75 SIN3_0 ADTG_8 INT07_1 MADATA10_0	E	H

Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
97	81	K14	P17 AN07 SIN2_2 INT04_1 MAD03_0	F	L
-	-	P7	VSS	-	
-	-	P11	VSS	-	
-	-	L14	VSS	-	
98	82	K11	P18 AN08 SOT2_2 INT21_1 MAD04_0	F	L
99	83	J13	P19 AN09 SCK2_2 INT22_1 MAD05_0	F	L
100	84	J12	P1A AN10 SIN4_1 INT05_1 TIOA13_2 IC00_1 MAD06_0	F	L
101	85	J11	P1B AN11 SOT4_1 INT25_1 TIOB13_2 IC01_1 MAD07_0	F	L
102	86	J10	P1C AN12 SCK4_1 INT26_1 TIOA14_2 IC02_1 MAD08_0	F	L
103	87	J9	P1D AN13 CTS4_1 INT27_1 TIOB14_2 IC03_1 MAD09_0	F	L
104	88	H10	P1E AN14 RTS4_1 INT28_1 TIOA15_2 DTTI0X_1 MAD10_0	F	L

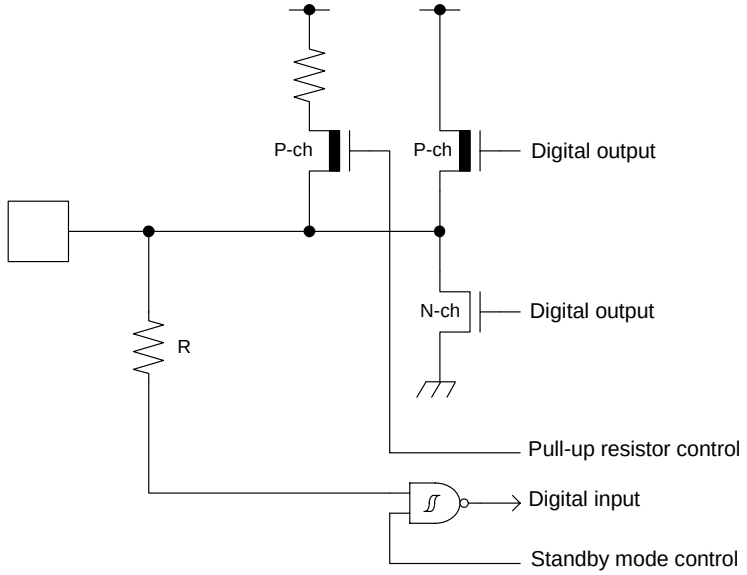
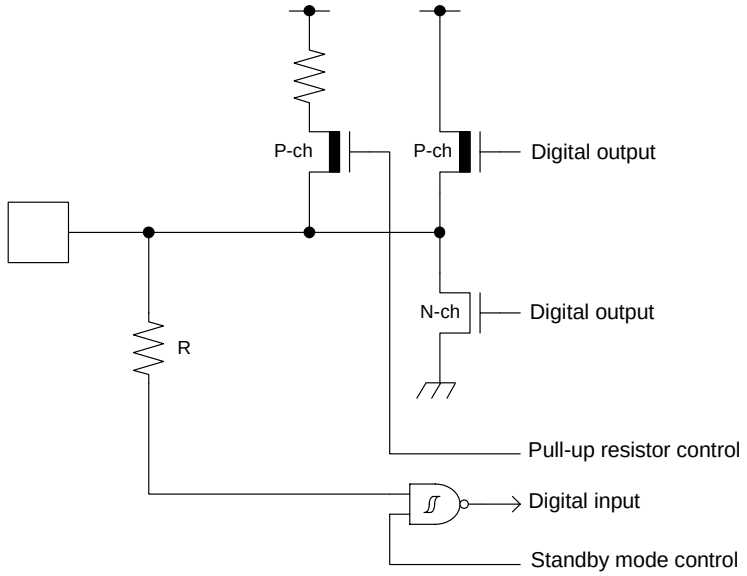
Pin No			Pin name	I/O circuit type	Pin state type
LQFP-176	LQFP-144	BGA-192			
117	-	G9	PB7 AN23 TIOB12_1 INT23_0 ZIN2_2	F	L
118	94	F10	P29 AN24 MAD12_0	F	K
119	95	F11	P28 AN25 ADTG_4 INT09_0 RTO05_1 MAD13_0	F	L
120	96	F12	P27 AN26 INT02_2 RTO04_1 MAD14_0	F	L
121	97	F13	P26 AN27 SCK2_1 RTO03_1 MAD15_0	F	K
122	98	E10	P25 AN28 SOT2_1 TX1_0 RTO02_1 MAD16_0	F	K
123	99	E11	P24 AN29 SIN2_1 RX1_0 INT01_2 RTO01_1 MAD17_0	F	L
124	100	E12	P23 AN30 SCK0_0 TIOA07_1 RTO00_1	F	K
125	101	E13	P22 AN31 SOT0_0 TIOB07_1 ZIN1_1	F	K
126	102	D12	P21 SIN0_0 INT06_1 BIN1_1	E	H

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Base Timer 14	TIOA14_0	Base timer ch.14 TIOA pin	151	121	D8
	TIOA14_1		78	-	N10
	TIOA14_2		102	86	J10
	TIOB14_0	Base timer ch.14 TIOB pin	164	134	B6
	TIOB14_1		79	-	L10
	TIOB14_2		103	87	J9
Base Timer 15	TIOA15_0	Base timer ch.15 TIOA pin	73	65	N9
	TIOA15_1		80	-	K10
	TIOA15_2		104	88	H10
	TIOB15_0	Base timer ch.15 TIOB pin	74	66	M9
	TIOB15_1		81	-	M10
	TIOB15_2		105	89	H9
CAN 0	TX0_0	CAN interface ch.0 TX output	65	57	J6
	TX0_1		32	-	J5
	TX0_2		7	7	D1
	RX0_0	CAN interface ch.0 RX output	66	58	N8
	RX0_1		33	-	J4
	RX0_2		6	6	D2
CAN 1	TX1_0	CAN interface ch.1 TX output	122	98	E10
	TX1_1		23	23	G5
	TX1_2		92	76	L13
	RX1_0	CAN interface ch.1 RX output	123	99	E11
	RX1_1		22	22	G4
	RX1_2		91	75	M12
Debugger	SWCLK	Serial wire debug interface clock input	135	111	A12
	SWDIO	Serial wire debug interface data input / output	137	113	B12
	SWO	Serial wire viewer output	138	114	B11
	TCK	J-TAG test clock input	135	111	A12
	TDI	J-TAG test data input	136	112	C12
	TDO	J-TAG debug data output	138	114	B11
	TMS	J-TAG test mode state input/output	137	113	B12
	TRACECLK	Trace CLK output of ETM	12	12	E4
	TRACED0	Trace data output of ETM	8	8	D3
	TRACED1		9	9	D4
	TRACED2		10	10	E2
	TRACED3		11	11	E3
	TRSTX	J-TAG test reset Input	134	110	B13

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin	16	16	F3
	SIN6_1		31	-	H6
	SIN6_2		170	-	B4
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	17	17	F4
	SOT6_1 (SDA6_1)		30	-	H5
	SOT6_2 (SDA6_2)		171	-	C4
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	18	18	F5
	SCK6_1 (SCL6_1)		29	-	H4
	SCK6_2 (SCL6_2)		172	140	B3
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin	22	22	G4
	SIN7_1		64	56	K6
	SIN7_2		110	-	H13
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	23	23	G5
	SOT7_1 (SDA7_1)		63	55	L6
	SOT7_2 (SDA7_2)		111	-	H12
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	24	24	G6
	SCK7_1 (SCL7_1)		62	54	M6
	SCK7_2 (SCL7_2)		112	-	H11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	37	29	K2
	DTTI0X_1		104	88	H10
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	32	-	J5
	FRCK0_1		105	89	H9
	FRCK0_2		91	75	M12
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0 ICxx describes channel number.	36	28	K1
	IC00_1		100	84	J12
	IC00_2		92	76	L13
	IC01_0		35	27	J2
	IC01_1		101	85	J11
	IC01_2		93	77	L12
	IC02_0		34	26	J3
	IC02_1		102	86	J10
	IC02_2		94	78	L11
	IC03_0		33	-	J4
	IC03_1		103	87	J9
	IC03_2		95	79	K13
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG0 output modes.	38	30	K3
	RTO00_1 (PPG00_1)		124	100	E12
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG00 when it is used in PPG0 output modes.	39	31	K4
	RTO01_1 (PPG00_1)		123	99	E11
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG0 output modes.	40	32	L1
	RTO02_1 (PPG02_1)		122	98	E10
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG02 when it is used in PPG0 output modes.	41	33	L2
	RTO03_1 (PPG02_1)		121	97	F13
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG0 output modes.	42	34	L3
	RTO04_1 (PPG04_1)		120	96	F12
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0 This pin operates as PPG04 when it is used in PPG0 output modes.	43	35	M2
	RTO05_1 (PPG04_1)		119	95	F11

Module	Pin name	Function	Pin No		
			LQFP-176	LQFP-144	BGA-192
Multi Function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	19	19	F6
	DTTI1X_1		58	50	M5
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	2	2	B2
	FRCK1_1		63	55	L6
	IC10_0	16-bit input capture ch.1 input pin of multi-function timer 1. ICxx describes channel number	3	3	C2
	IC10_1		59	51	L5
	IC11_0		4	4	C3
	IC11_1		60	52	K5
	IC12_0		5	5	D5
	IC12_1		61	53	N6
	IC13_0		6	6	D2
	IC13_1		62	54	M6
	RTO10_0 (PPG10_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	13	13	E5
	RTO10_1 (PPG10_1)		46	38	N2
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	14	14	F1
	RTO11_1 (PPG10_1)		47	39	N3
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	15	15	F2
	RTO12_1 (PPG12_1)		48	40	M3
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	16	16	F3
	RTO13_1 (PPG12_1)		49	41	L4
	RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	17	17	F4
	RTO14_1 (PPG14_1)		50	42	M4
	RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	18	18	F5
	RTO15_1 (PPG14_1)		51	43	N4

Type	Circuit	Remarks
K		• CMOS level output • TTL level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
L		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

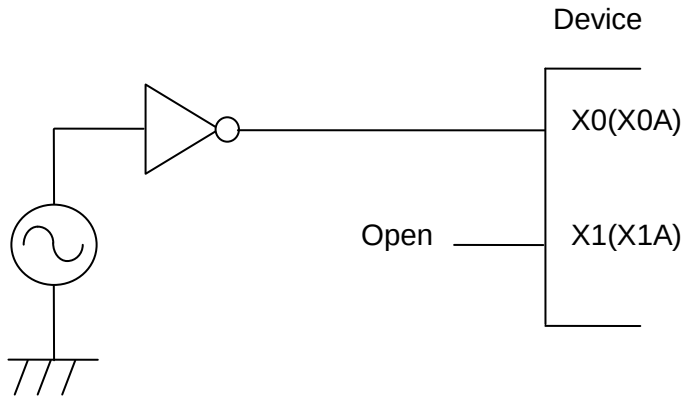
It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Using an external clock

When using an external clock, the clock signal should be input to the X0, X0A pin only and the X1,X1A pin should be kept open.

- **Example of Using an External Clock**



Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Multi-function timer unit2
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low Voltage Detector
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN Prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4005_FFFF		USB ch.1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		CAN ch.0
0x4006_3000	0x4006_3FFF		CAN ch.1
0x4006_4000	0x41FF_FFFF		Reserved

Separate Bus Access Asynchronous SRAM Mode

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MCSX ↓ → Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	Vcc ≥ 4.5 V	-9	+9	ns
			Vcc < 4.5 V	-12	+12	
MOEX ↑ → Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×m-9	MCLK×m+9	ns
			Vcc < 4.5 V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	20	-	ns
			Vcc < 4.5 V	38	-	
MOEX ↑ → Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX Min pulse width	t_{WEW}	MWEX	Vcc ≥ 4.5 V	MCLK×n-3	-	ns
			Vcc < 4.5 V			
MWEX ↑ → Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH-CSH}$		Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	Vcc ≥ 4.5 V	MCLK×n-9	MCLK×n+9	ns
			Vcc < 4.5 V	MCLK×n-12	MCLK×n+12	
MCSX ↓ → Data output time	t_{CSL-DV}	MCSX, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK-9	MCLK+9	ns
			Vcc < 4.5 V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	Vcc ≥ 4.5 V	0	MCLK×m+9	ns
			Vcc < 4.5 V		MCLK×m+12	

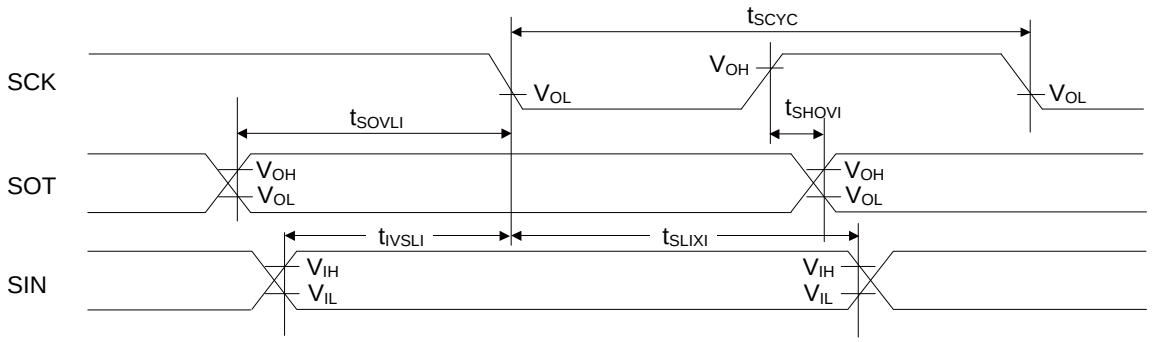
Note: When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)

Separate Bus Access Synchronous SRAM Mode

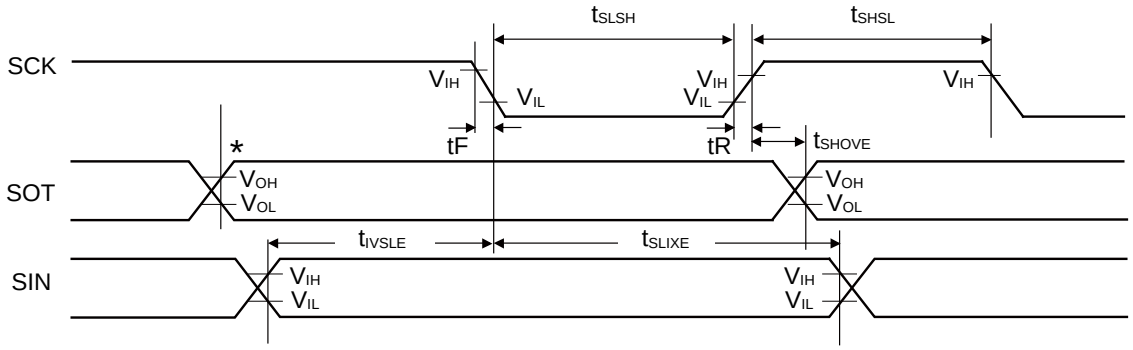
(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{CSH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{REH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	19	-	ns
			Vcc < 4.5 V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	0	-	ns
			Vcc < 4.5 V			
MWEX delay time	t_{WEL}	MCLK, MWEX	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{WEH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
	t_{DQMH}		Vcc ≥ 4.5 V	1	9	ns
			Vcc < 4.5 V		12	
MCLK ↑ → Data output time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	MCLK+1	MCLK+18	ns
			Vcc < 4.5 V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	Vcc ≥ 4.5 V	1	18	ns
			Vcc < 4.5 V		24	

Note: When the external load capacitance = 30 pF.



Master mode



Slave mode

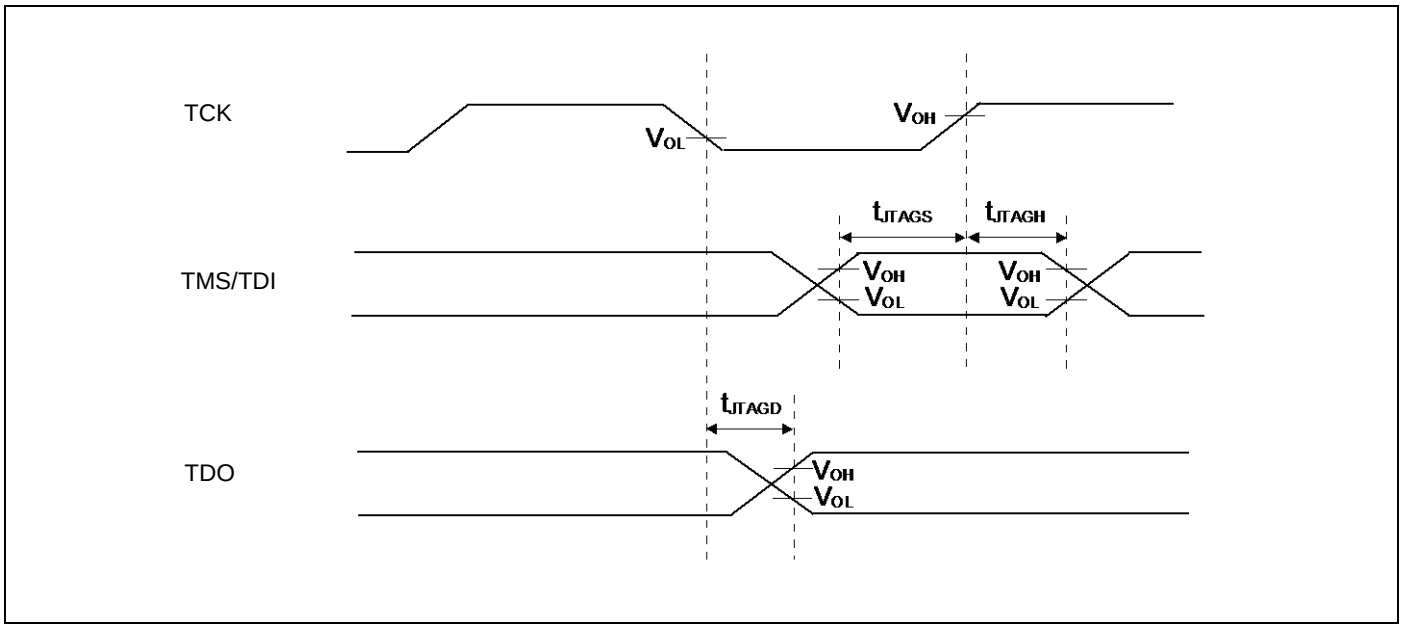
*: Changes when writing to TDR register

12.4.15 JTAG Timing

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	Vcc ≥ 4.5 V	15	-	ns	
			Vcc < 4.5 V				
TDO delay time	t_{JTAGD}	TCK, TDO	Vcc ≥ 4.5 V	-	25	ns	
			Vcc < 4.5 V	-	45		

Note: When the external load capacitance = 30 pF.



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-		± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-		± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-		± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-		AVRH ± 15	mV	
Conversion time	-	-	1.0*1	-	-	µs	AVcc ≥ 4.5 V
			1.2*1	-	-		AVcc < 4.5 V
Sampling time	Ts	-	*2	-	-	ns	AVcc ≥ 4.5 V
			*2	-	-		AVcc < 4.5 V
Compare clock cycle*3	Tcck	-	50	-	2000	ns	
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	12.9	pF	
Analog input resistance	R_{AIN}	-	-	-	2	kΩ	AVcc ≥ 4.5 V
					3.8		AVcc < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	

*1: The Conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is the following.

AVcc ≥ 4.5 V, HCLK=120 MHz sampling time: 300 ns compare time: 700 ns
AVcc < 4.5 V, HCLK=120 MHz sampling time: 500 ns compare time: 700 ns
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

The registers setting of the A/D Converter are reflected in the operation according to the APB bus clock timing.

The sampling clock and compare clock is generated from the Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "8. Block Diagram" in this datasheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: Compare time (Tc) is the value of (Equation 2).

12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	4032 × t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.