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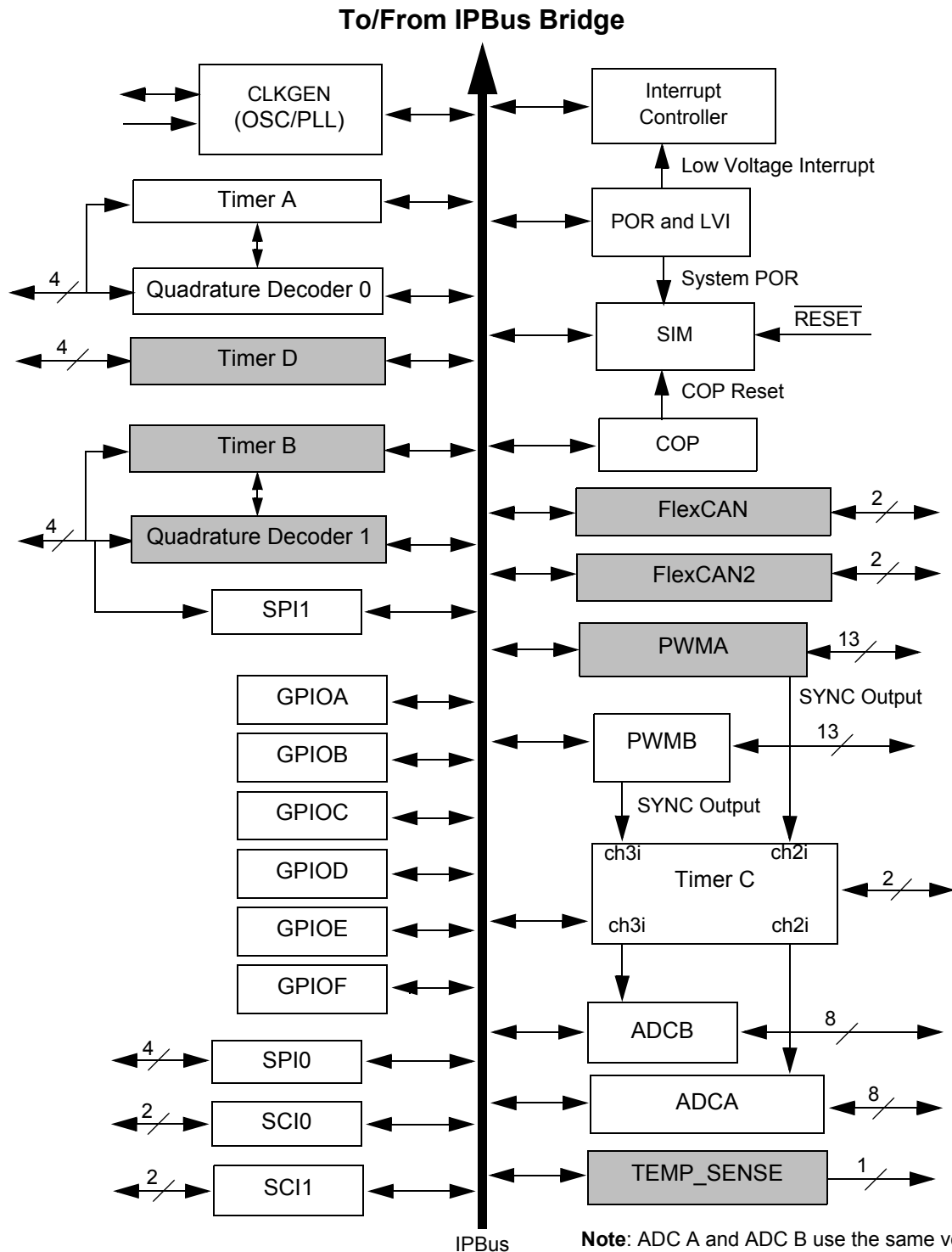
Details

Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8165vfge

- In the 56F8365, two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and four Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- In the 56F8165, one Pulse Width Modulator module with six PWM outputs, three Current Sense inputs and three Fault inputs; fault-tolerant design with dead time insertion; supports both center-aligned and edge-aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized through Timer C, channels 2 and 3
- Quadrature Decoder:
 - In the 56F8365, two four-input Quadrature Decoders or two additional Quad Timers
 - In the 56F8165, one four-input Quadrature Decoder, which works in conjunction with Quad Timer A
- *Temperature Sensor can be connected, on the board, to any of the ADC inputs to monitor the on-chip temperature*
- Quad Timer:
 - In the 56F8365, four dedicated general-purpose Quad Timers totaling six dedicated pins: Timer C with two pins and Timer D with four pins
 - In the 56F8165, two Quad Timers; Timer A and Timer C both work in conjunction with GPIO
- Optional On-Chip Regulator
- *Up to two FlexCAN (CAN Version 2.0 B-compliant) modules with 2-pin port for transmit and receive*
- Two Serial Communication Interfaces (SCIs), each with two pins (or four additional GPIO lines)
- Up to two Serial Peripheral Interfaces (SPIs), both with configurable 4-pin port (or eight additional GPIO lines); SPI1 can also be used as Quadrature Decoder 1 or Quad Timer B
- Computer Operating Properly (COP)/Watchdog timer
- Two dedicated external interrupt pins
- 49 General Purpose I/O (GPIO) pins; 28 pins dedicated to GPIO
- External reset input pin for hardware reset
- External reset output pin for system reset
- Integrated low-voltage interrupt module
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging
- Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer for the core clock

1.1.5 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-board 3.3V down to 2.6V voltage regulator for powering internal logic and memories; can be disabled
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power



NOT available on the 56F8165 device.

Note: ADC A and ADC B use the same voltage reference circuit with V_{REFH} , V_{REFP} , V_{REFMID} , V_{REFN} , and V_{REFLO} pins.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
HOME0 (TA3) (GPIOC7)	2	Schmitt Input Schmitt Input/Output Schmitt Input/Output	Input, pull-up enabled	Home — Quadrature Decoder 0, HOME input TA3 — Timer A, Channel 3 Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is HOME0. To deactivate the internal pull-up resistor, clear bit 7 of the GPIOC_PUR register.
SCLK0 (GPIOE4)	124	Schmitt Input/Output Schmitt Input/Output	Input, pull-up enabled	SPI 0 Serial Clock — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0. To deactivate the internal pull-up resistor, clear bit 4 in the GPIOE_PUR register.
MOSI0 (GPIOE5)	126	Input/Output Input/Output	In reset, output is disabled, pull-up is enabled	SPI 0 Master Out/Slave In — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0. To deactivate the internal pull-up resistor, clear bit 5 in the GPIOE_PUR register.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PHASEB1	10	Schmitt Input	Input, pull-up enabled	Phase B1 — Quadrature Decoder 1, PHASEB input for decoder 1.
(TB1)		Schmitt Input/Output		TB1 — Timer B, Channel 1
(MOSI1)		Schmitt Input/Output		SPI 1 Master Out/Slave In — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see Part 6.5.8 .
(GPIOC1)		Schmitt Input/Output		<p>Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.</p> <p>In the 56F8365, the default state after reset is PHASEB1.</p> <p>In the 56F8165, the default state is not one of the functions offered and must be reconfigured.</p> <p>To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register.</p>

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
PWMB0	32	Output	In reset, output is disabled	PWMB0 - 5 — Six PWMB output pins.
PWMB1	33			
PWMB2	34			
PWMB3	37			
PWMB4	38			
PWMB5	39			
ISB0 (GPIOD10)	48	Schmitt Input	Input, pull-up enabled	ISB0 - 2 — These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB. Port D GPIO — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to ISA functionality. Deactivate pull-up by setting the appropriate bit of the GPIOD_PUR register. See Part 6.5.6 for details.
ISB1 (GPIOD11)	50	Schmitt Input/ Output		
ISB2 (GPIOD12)	51			
FAULTB0	54	Schmitt Input	Input, pull-up enabled	FAULTB0 - 3 — These four fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip. To deactivate the internal pull-up resistor, set the PWMB bit in the SIM_PUDR register. See Part 6.5.6 for details.
FAULTB1	55			
FAULTB2	56			
FAULTB3	57			
ANA0	80	Input	Analog Input	ANA0 - 3 — Analog inputs to ADC A, channel 0
ANA1	81			
ANA2	82			
ANA3	83			
ANA4	84	Input	Analog Input	ANA4 - 7 — Analog inputs to ADC A, channel 1
ANA5	85			
ANA6	86			
ANA7	87			
V _{REFH}	93	Input	Analog Input	V_{REFH} — Analog Reference Voltage High. V _{REFH} must be less than or equal to V _{DDA_ADC} .

Table 4-5 Interrupt Vector Table Contents¹ (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core	14	2	P:\$1C	SW Interrupt 2
core	15	1	P:\$1E	SW Interrupt 1
core	16	0	P:\$20	SW Interrupt 0
core	17	0-2	P:\$22	IRQA
core	18	0-2	P:\$24	IRQB
				Reserved
LVI	20	0-2	P:\$28	Low-Voltage Detector (power sense)
PLL	21	0-2	P:\$2A	PLL
FM	22	0-2	P:\$2C	FM Access Error Interrupt
FM	23	0-2	P:\$2E	FM Command Complete
FM	24	0-2	P:\$30	FM Command, data and address Buffers Empty
				Reserved
<i>FLEXCAN</i>	26	0-2	P:\$34	FLEXCAN Bus Off
<i>FLEXCAN</i>	27	0-2	P:\$36	FLEXCAN Error
<i>FLEXCAN</i>	28	0-2	P:\$38	FLEXCAN Wake Up
<i>FLEXCAN</i>	29	0-2	P:\$3A	FLEXCAN Message Buffer Interrupt
GPIOF	30	0-2	P:\$3C	GPIO F
GPIOE	31	0-2	P:\$3E	GPIO E
GPIOD	32	0-2	P:\$40	GPIO D
GPIOC	33	0-2	P:\$42	GPIO C
GPIOB	34	0-2	P:\$44	GPIO B
GPIOA	35	0-2	P:\$46	GPIO A
				Reserved
SPI1	38	0-2	P:\$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:\$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:\$50	SPI 0 Receiver Full
SPI0	41	0-2	P:\$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:\$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:\$56	SCI 1 Transmitter Idle
				Reserved
SCI1	45	0-2	P:\$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:\$5C	SCI 1 Receiver Full

Table 4-11 Quad Timer A Registers Address Map (Continued)
(TMRA_BASE = \$00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP2	\$1	Compare Register 2
TMRA0_CAP	\$2	Capture Register
TMRA0_LOAD	\$3	Load Register
TMRA0_HOLD	\$4	Hold Register
TMRA0_CNTR	\$5	Counter Register
TMRA0_CTRL	\$6	Control Register
TMRA0_SCR	\$7	Status and Control Register
TMRA0_CMPLD1	\$8	Comparator Load Register 1
TMRA0_CMPLD2	\$9	Comparator Load Register 2
TMRA0_COMSCR	\$A	Comparator Status and Control Register
		Reserved
TMRA1_CMP1	\$10	Compare Register 1
TMRA1_CMP2	\$11	Compare Register 2
TMRA1_CAP	\$12	Capture Register
TMRA1_LOAD	\$13	Load Register
TMRA1_HOLD	\$14	Hold Register
TMRA1_CNTR	\$15	Counter Register
TMRA1_CTRL	\$16	Control Register
TMRA1_SCR	\$17	Status and Control Register
TMRA1_CMPLD1	\$18	Comparator Load Register 1
TMRA1_CMPLD2	\$19	Comparator Load Register 2
TMRA1_COMSCR	\$1A	Comparator Status and Control Register
		Reserved
TMRA2_CMP1	\$20	Compare Register 1
TMRA2_CMP2	\$21	Compare Register 2
TMRA2_CAP	\$22	Capture Register
TMRA2_LOAD	\$23	Load Register
TMRA2_HOLD	\$24	Hold Register
TMRA2_CNTR	\$25	Counter Register
TMRA2_CTRL	\$26	Control Register
TMRA2_SCR	\$27	Status and Control Register
TMRA2_CMPLD1	\$28	Comparator Load Register 1

**Table 4-26 Serial Peripheral Interface 1 Registers Address Map
(SPI1_BASE = \$00 F2B0)**

Register Acronym	Address Offset	Register Description
SPI1_SPSCR	\$0	Status and Control Register
SPI1_SPDSR	\$1	Data Size Register
SPI1_SPDRR	\$2	Data Receive Register
SPI1_SPDTR	\$3	Data Transmitter Register

**Table 4-27 Computer Operating Properly Registers Address Map
(COP_BASE = \$00 F2C0)**

Register Acronym	Address Offset	Register Description
COPCTL	\$0	Control Register
COPTO	\$1	Time Out Register
COPCTR	\$2	Counter Register

**Table 4-28 Clock Generation Module Registers Address Map
(CLKGEN_BASE = \$00 F2D0)**

Register Acronym	Address Offset	Register Description
PLLCR	\$0	Control Register
PLLDB	\$1	Divide-By Register
PLLSR	\$2	Status Register
		Reserved
SHUTDOWN	\$4	Shutdown Register
OSCTL	\$5	Oscillator Control Register

**Table 4-29 GPIOA Registers Address Map
(GPIOA_BASE = \$00 F2E0)**

Register Acronym	Address Offset	Register Description	Reset Value
GPIOA_PUR	\$0	Pull-up Enable Register	0 x 3FFF
GPIOA_DR	\$1	Data Register	0 x 0000
GPIOA_DDR	\$2	Data Direction Register	0 x 0000
GPIOA_PER	\$3	Peripheral Enable Register	0 x 3FFF

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.2 Timer B, Channel 3 Interrupt Priority Level (TMRB3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.3 Timer B, Channel 2 Interrupt Priority Level (TMRB2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.4 Timer B, Channel 1 Interrupt Priority Level (TMRB1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.5 Timer B, Channel 0 Interrupt Priority Level (TMRB0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0

- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.2 SCIO Receiver Error Interrupt Priority Level (SCIO_RERR IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.9.4 SCIO Transmitter Idle Interrupt Priority Level (SCIO_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.5 SCIO Transmitter Empty Interrupt Priority Level (SCIO_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.6 Timer A, Channel 3 Interrupt Priority Level (TMRA3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + \$E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see [Part 5.3.3](#). IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to [Table 4-5](#).

5.6.16 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

Base + \$F	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-18 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

5.6.16.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of the vector address are used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.19.1 IRQ Pending (PENDING)—Bits 32–17

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.20 IRQ Pending 2 Register (IRQP2)

Base + \$13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [48:33]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-22 IRQ Pending 2 Register (IRQP2)

5.6.20.1 IRQ Pending (PENDING)—Bits 48–33

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.21 IRQ Pending 3 Register (IRQP3)

Base + \$14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [64:49]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-23 IRQ Pending 3 Register (IRQP3)

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.3 FlexCAN2 Wake Up Interrupt Priority Level (FlexCAN2_WKUP IPL)—Bits 5 - 4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.4 FlexCAN2 Error Interrupt Priority Level (FlexCAN2_ERR IPL)—Bits 3 - 2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.5 FlexCAN2 Bus-Off Interrupt Priority Level (FlexCAN2_BOFF IPL)—Bits 1 - 0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled except the core IRQs with fixed priorities:

- Illegal Instruction

occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external RESET pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can only be cleared by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown in this section. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + \$2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources (RESET pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads \$01D6.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Part 7 Security Features

The 56F8365/56F8165 offers security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8365/56F8165 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TRST, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port)

Part 8 General Purpose Input/Output (GPIO)

8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F8300 Peripheral User Manual** and contains only chip-specific information. This information supercedes the generic information in the **56F8300 Peripheral User Manual**.

8.2 Memory Maps

The width of the GPIO port defines how many bits are implemented in each of the GPIO registers. Based on this and the default function of each of the GPIO pins, the reset values of the GPIOx_PUR and GPIOx_PER registers change from port to port. Tables 4-29 through 4-34 define the actual reset values of these registers.

8.3 Configuration

There are six GPIO ports defined on the 56F8365/56F8165. The width of each port and the associated peripheral function is shown in Table 8-1 and Table 8-2. The specific mapping of GPIO port pins is shown in Table 8-3.

Table 8-1 56F8365 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8365	Peripheral Function	Reset Function
A	14	6	6 pins - EMI Address pins - Can only be used as GPIO 8 pins - EMI Address pins - Not available in this package	EMI Address N/A
B	8	5	5 pins - EMI Address pins - Can only be used as GPIO 3 pins - EMI Address pins - Not available in this package	GPIO N/A
C	11	11	4 pins -DEC1 / TMRB / SPI1 4 pins -DEC0 / TMRA 3 pins -PWMA current sense	DEC1 / TMRB DEC0 / TMRA PWMA current sense
D	13	11	2 pins - EMI $\overline{\text{CSn}}$ 4 pins - EMI $\overline{\text{CSn}}$ - Can only be used as GPIO 2 pins - SCI1 2 pins - EMI $\overline{\text{CSn}}$ - Not available in this package 3 pins -PWMB current sense	EMI Chip Selects EMI Chip Selects SCI1 N/A PWMB current sense
E	14	12	2 pins - SCI0 2 pins - EMI Address pins - Not available in this package 4 pins - SPI0 2 pins - TMRC 4 pins - TMRD	SCI0 N/A SPI0 TMRC TMRD

Table 8-3 GPIO External Signals Map (Continued)
Pins in shaded rows are not available in 56F8365 / 56F8165
Pins in italics are NOT available in the 56F8165 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOC	0	Peripheral	<i>PhaseA1 / TB0 / SCLK1²</i>	9
	1	Peripheral	<i>PhaseB1 / TB1 / MOSI1²</i>	10
	2	Peripheral	<i>Index1 / TB2 / MISO1²</i>	11
	3	Peripheral	<i>Home1 / TB3 / <math>\overline{SS}1²</math></i>	12
	4	Peripheral	PhaseA0 / TA0	127
	5	Peripheral	PhaseB0 / TA1	128
	6	Peripheral	Index0 / TA2	1
	7	Peripheral	Home0 / TA3	2
	8	Peripheral	<i>ISA0</i>	104
	9	Peripheral	<i>ISA1</i>	105
	10	Peripheral	<i>ISA2</i>	106
GPIO D	0	GPIO	$\overline{CS}2$ / CAN2_TX	42
	1	GPIO	$\overline{CS}3$ / CAN2_RX	43
	2	GPIO	$\overline{CS}41$	44
	3	GPIO	$\overline{CS}51$	45
	4	GPIO	$\overline{CS}61$	46
	5	GPIO	$\overline{CS}71$	47
	6	Peripheral	TXD1	40
	7	Peripheral	RXD1	41
	8	N/A		
	9	N/A		
	10	Peripheral	ISB0	48
	11	Peripheral	ISB1	50
	12	Peripheral	ISB2	51

Table 10-5 DC Electrical Characteristics (Continued)

At Recommended Operating Conditions; see [Table 10-4](#)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Capacitance	C_{OUT}		—	6	—	pF	—

See Pin Groups listed in [Table 10-1](#)

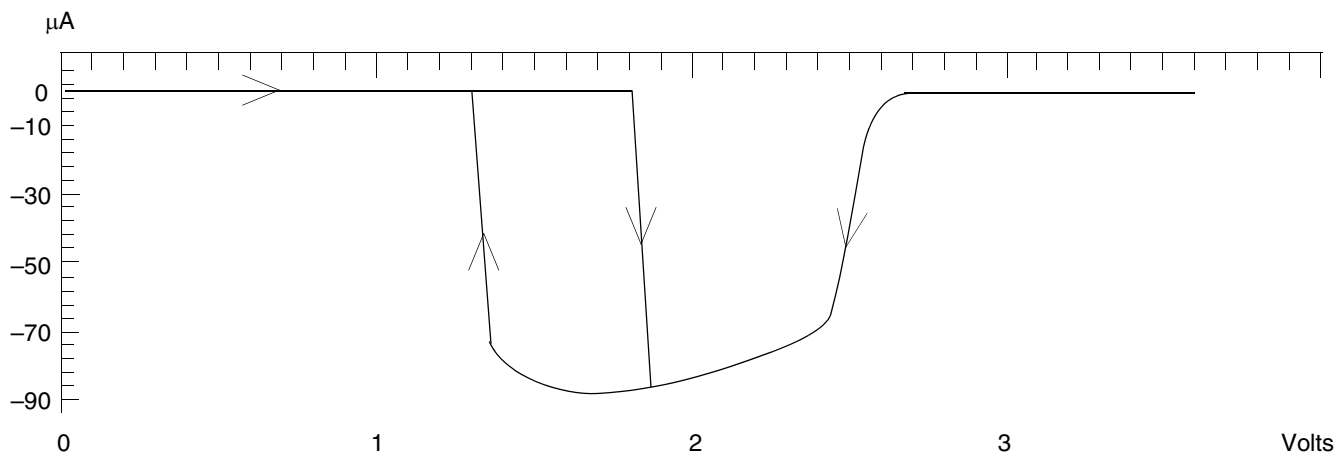


Figure 10-1 Maximum Current — Schmitt Input DC Response –40 °C, 3.6 V

Table 10-6 Power-On Reset Low Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Units
POR Trip Point	POR	1.75	1.8	1.9	V
LVI, 2.5 volt Supply, trip point ¹	$V_{EI2.5}$	—	2.14	—	V
LVI, 3.3 volt supply, trip point ²	$V_{EI3.3}$	—	2.7	—	V
Bias Current	I_{bias}	—	110	130	μA

1. When V_{DD_CORE} drops below $V_{EI2.5}$, an interrupt is generated.

2. When V_{DD_CORE} drops below $V_{EI3.3}$, an interrupt is generated.

Table 11-1 56F8365 128-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
3	V _{SS}	35	V _{SS}	67	FAULTA0	99	ANB3
4	V _{DD_IO}	36	V _{DD_IO}	68	FAULTA1	100	ANB4
5	V _{PP2}	37	PWMB3	69	FAULTA2	101	ANB5
6	CLKO	38	PWMB4	70	FAULTA3	102	ANB6
7	TXD0	39	PWMB5	71	OCR_DIS	103	ANB7
8	RXD0	40	TXD1	72	V _{DDA_OSC_PLL}	104	ISA0
9	PHASEA1	41	RXD1	73	XTAL	105	ISA1
10	PHASEB1	42	GPIOD0	74	EXTAL	106	ISA2
11	INDEX1	43	GPIOD1	75	V _{CAP3}	107	TD0
12	HOME1	44	GPIOD2	76	V _{DD_IO}	108	TD1
13	V _{CAP4}	45	GPIOD3	77	$\overline{\text{RSTO}}$	109	TD2
14	V _{DD_IO}	46	GPIOD4	78	$\overline{\text{RESET}}$	110	TD3
15	GPIOA0 ¹	47	GPIOD5	79	CLKMODE	111	TC0
16	GPIOA1 ¹	48	ISB0	80	ANA0	112	V _{DD_IO}
17	GPIOA2 ¹	49	V _{CAP1}	81	ANA1	113	TC1
18	GPIOA3 ¹	50	ISB1	82	ANA2	114	$\overline{\text{TRST}}$
19	GPIOA4 ¹	51	ISB2	83	ANA3	115	TCK
20	GPIOA5 ¹	52	$\overline{\text{IRQA}}$	84	ANA4	116	TMS
21	V _{SS}	53	$\overline{\text{IRQB}}$	85	AN5	117	TDI
20	GPIOF0 ¹	54	FAULTB0	86	ANA6	118	TDO
23	GPIOF1 ¹	55	FAULTB1	87	ANA7	119	V _{PP1}
24	GPIOF2 ¹	56	FAULTB2	88	TEMP_SENSE	120	CAN_TX
25	V _{DD_IO}	57	FAULTB3	89	V _{REFLO}	121	CAN_RX
1. Primary function is not available in this package configuration; GPIO function must be used instead							
26	GPIOF3 ¹	58	PWMA0	90	V _{REFN}	122	V _{CAP2}
27	GPIOB0	59	V _{SS}	91	V _{REFMID}	123	$\overline{\text{SS0}}$
28	GPIOB1	60	PWMA1	92	V _{REFP}	124	SCLK0

Figure 11-3 128-pin LQFP Mechanical Information

Please see www.freescale.com for the most current case outline.

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = Ambient temperature for the package ($^{\circ}\text{C}$)

$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance $^{\circ}\text{C}/\text{W}$

$R_{\theta JC}$ = Package junction-to-case thermal resistance $^{\circ}\text{C}/\text{W}$

$R_{\theta CA}$ = Package case-to-ambient thermal resistance $^{\circ}\text{C}/\text{W}$

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$