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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	49
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8365mfge

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Figure 1-2 Peripheral Subsystem

Table 1-2 Bus Signal Names

Name	Function
Program Memory Interface	
pdb_m[15:0]	Program data bus for instruction word fetches or read operations.
cdbw[15:0]	Primary core data bus used for program memory writes. (Only these 16 bits of the cdbw[31:0] bus are used for writes to program memory.)
pab[20:0]	Program memory address bus. Data is returned on pdb_m bus.
Primary Data Memory Interface Bus	
cdbr_m[31:0]	Primary core data bus for memory reads. Addressed via xab1 bus.
cdbw[31:0]	Primary core data bus for memory writes. Addressed via xab1 bus.
xab1[23:0]	Primary data address bus. Capable of addressing bytes[1], words, and long data types. Data is written on cdbw and returned on cdbr_m. Also used to access memory-mapped I/O.
Secondary Data Memory Interface	
xdb2_m[15:0]	Secondary data bus used for secondary data address bus xab2 in the dual memory reads.
xab2[23:0]	Secondary data address bus used for the second of two simultaneous accesses. Capable of addressing only words. Data is returned on xdb2_m.
Peripheral Interface Bus	
IPBus [15:0]	Peripheral bus accesses all on-chip peripherals registers. This bus operates at the same clock rate as the Primary Data Memory and therefore generates no delays when accessing the processor. Write data is obtained from cdbw. Read data is provided to cdbr_m.

1. Byte accesses can only occur in the bottom half of the memory address space. The MSB of the address will be forced to 0.

1.5 Product Documentation

The documents listed in **Table 1-3** are required for a complete description and proper design with the 56F8365/56F8165 devices.. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com**.

Table 1-3 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit controller core processor, and the instruction set	DSP56800EERM
56F8300 Peripheral User Manual	Detailed description of peripherals of the 56F8300 family of devices	MC56F8300UM

Table 4-8 EOnCE Memory Map (Continued)

Address	Register Acronym	Register Name
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register
X:$FF FFFD	OTXRXSR (8 bits)	Transmit and Receive Status and Control Register
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register / Receive Register
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word

4.7 Peripheral Memory Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read/written using word accesses only.

Table 4-9 summarizes base addresses for the set of peripherals on the 56F8365 and 56F8165 devices. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Note: *Features in italics are NOT available in the 56F8165 device.*

Table 4-9 Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address	Table Number
External Memory Interface	EMI	X:$00 F020	4-10
Timer A	TMRA	X:$00 F040	4-11
Timer B	TMRB	X:$00 F080	4-12
Timer C	TMRC	X:$00 F0C0	4-13
Timer D	TMRD	X:$00 F100	4-14
PWM A	PWMA	X:$00 F140	4-15
PWM B	PWMB	X:$00 F160	4-16
Quadrature Decoder 0	DEC0	X:$00 F180	4-17
Quadrature Decoder 1	DEC1	X:$00 F190	4-18
ITCN	ITCN	X:$00 F1A0	4-19
ADC A	ADCA	X:$00 F200	4-20
ADC B	ADCB	X:$00 F240	4-21

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIMn register to the appropriate vector number.
3. Setting the FIVALn and FIVAHn registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the ITCN handles it as a fast interrupt. The ITCN takes the vector address from the appropriate FIVALn and FIVAHn registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector adddress and if it is not a JSR, the core starts its fast interrupt handling.

5.4 Block Diagram

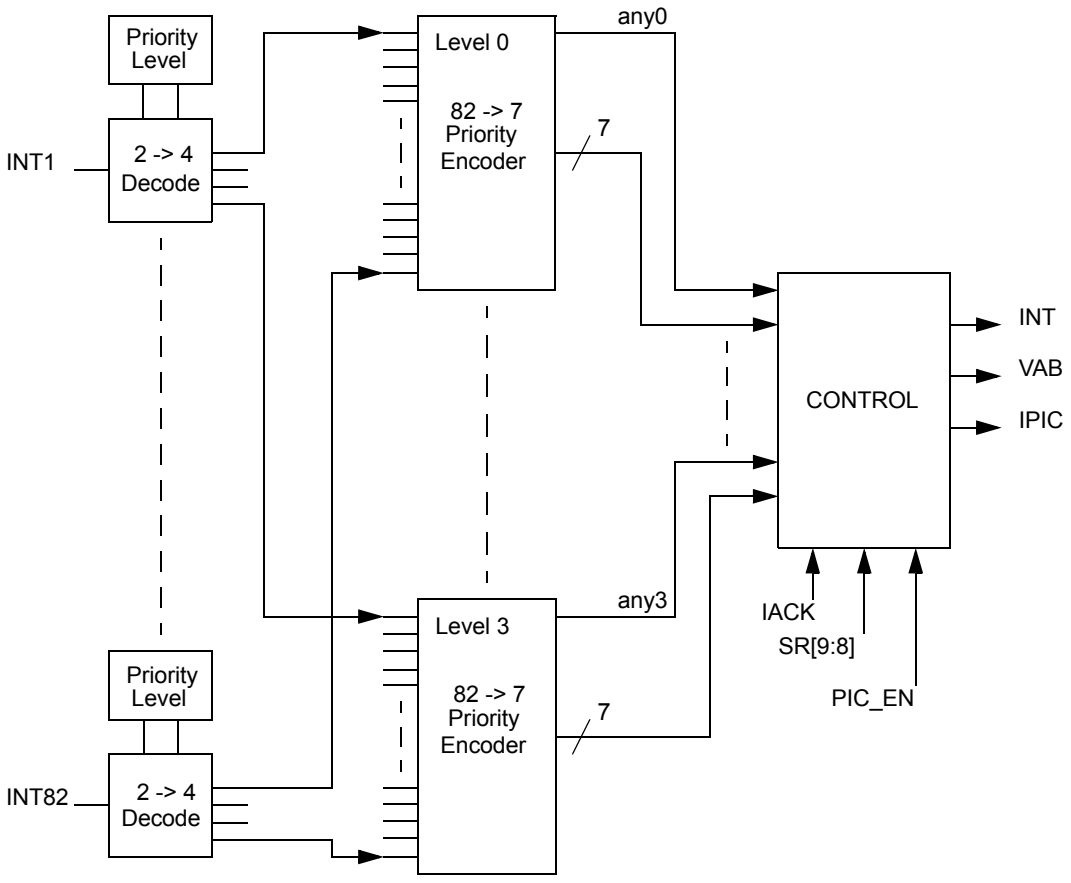

Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

5.6.6.4 SCI 1 Receiver Error Interrupt Priority Level (SCI1_RERR IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.5 Reserved—Bits 7–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.6 SCI 1 Transmitter Idle Interrupt Priority Level (SCI1_TIDL IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.7 SCI 1 Transmitter Empty Interrupt Priority Level (SCI1_XMIT IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.8 SPI 0 Transmitter Empty Interrupt Priority Level (SPI0_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.5 Timer D, Channel 0 Interrupt Priority Level (TMRD0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.7.7 Quadrature Decoder 0 INDEX Pulse Interrupt Priority Level (DEC0_XIRQ IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.8 Quadrature Decoder 0, HOME Signal Transition or Watchdog Timer Interrupt Priority Level (DEC0_HIRQ IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Interrupt Priority Register 7 (IPR7)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Interrupt Priority Register (IPR7)

- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.6 Timer C, Channel 3 Interrupt Priority Level (TMRC3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.7 Timer C, Channel 2 Interrupt Priority Level (TMRC2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.8 Timer C, Channel 1 Interrupt Priority Level (TMRC1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9 Interrupt Priority Register 8 (IPR8)

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-11 Interrupt Priority Register 8 (IPR8)

5.6.9.1 SCI0 Receiver Full Interrupt Priority Level (SCI0_RCV IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)

5.6.29 Reserved—Base + 1C

5.6.30 ITCN Control Register (ICTL)

Base + $1D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
Write																
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-26 ITCN Control Register (ICTL)

5.6.30.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

The reset state for MB and MA will depend on the Flash secured state. See **Part 4.2** and **Part 7** for detailed information on how the Operating Mode Register (OMR) MA and MB bits operate in this device. For additional information on the EX bit, see **Part 4.4**. For all other bits, see the **DSP56F800E Reference Manual**.

Note: The OMR is not a Memory Map register; it is directly accessible in code through the acronym OMR.

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.9
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.10
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10
Base + $F	SIM_PCE2	Peripheral Clock Enable Register 2	6.5.11

occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external RESET pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can only be cleared by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown in this section. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources (RESET pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01D6.

Table 8-1 56F8365 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8365	Peripheral Function	Reset Function
F	16	4	4 pins - EMI Data - Can only be used as GPIO 12 pins - EMI Data - Not available in this package	EMI Data N/A

Table 8-2 56F8165 GPIO Ports Configuration

GPIO Port	Port Width	Available Pins in 56F8165	Peripheral Function	Reset Function
A	14	6	6 pins - EMI Address pins - Can only be used as GPIO 8 pins - EMI Address pins - Not available in this package	EMI Address N/A
B	8	5	5 pins - EMI Address pins - Can only be used as GPIO 3 pins - EMI Address pins - Not available in this package	GPIO N/A
C	11	11	4 pins - SPI1 4 pins - DEC0 / TMRA 3 pins - Dedicated GPIO	DEC1 / TMRB DEC0 / TMRA GPIO
D	13	11	6 pins - EMI $\overline{\text{CSn}}$ - Can only be used as GPIO 2 pins - SCI1 2 pins - EMI $\overline{\text{CSn}}$ - Not available in this package 3 pins - PWMB current sense	EMI Chip Selects SCI1 N/A PWMB current sense
E	14	12	2 pins - SCI0 2 pins - EMI Address pins - Not available in this package 4 pins - SPI0 2 pins - TMRC 4 pins - Dedicated GPIO	SCI0 N/A SPI0 TMRC GPIO
F	16	4	4 pins - EMI Data - Can only be used as GPIO 12 pins - EMI Data - Not available in this package	EMI Data N/A

inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Note: All specifications meet both Automotive and Industrial requirements unless individual specifications are listed.

Note: *The 56F8165 device is guaranteed to 40MHz and specified to meet Industrial requirements only.*

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Note: *The 56F8165 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8165 device.*

Table 10-1 Absolute Maximum Ratings

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply voltage	V_{DD_IO}		- 0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	- 0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		- 0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	- 0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 2, 5, 6, 9, 10	-0.3	6.0	V
Input Voltage (analog)	V_{INA}	Pin Groups 11, 12, 13	-0.3	4.0	V

10.2 DC Electrical Characteristics

Note: *The 56F8165 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8165 device.*

Table 10-5 DC Electrical Characteristics

At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2, 5, 6, 9	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 10	40	80	160	µA	V_{IN} = 3.0V to 5.5V
Analog Input Current High	I_{IHA}	Pin Group 13	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$
ADC Input Current High	I_{IHADC}	Pin Group 12	—	0	+/- 3.5	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 2, 5, 6, 9	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 10	—	0	+/- 2.5	µA	V_{IN} = 0V
Analog Input Current Low	I_{ILA}	Pin Group 13	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 12	—	0	+/- 3.5	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DD}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CKLMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CKLMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3, 4, 5, 6, 7, 8	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 2, 6, 9,10	—	0.3	—	V	—
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	—
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	—
Input Capacitance	C_{IN}		—	6	—	pF	—

Table 10-16 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[3]	t_{IW}	1.5T	—	ns	10-9

1. In the formulas, T = clock cycle. For an operating frequency of 60MHz, T = 16.67ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.

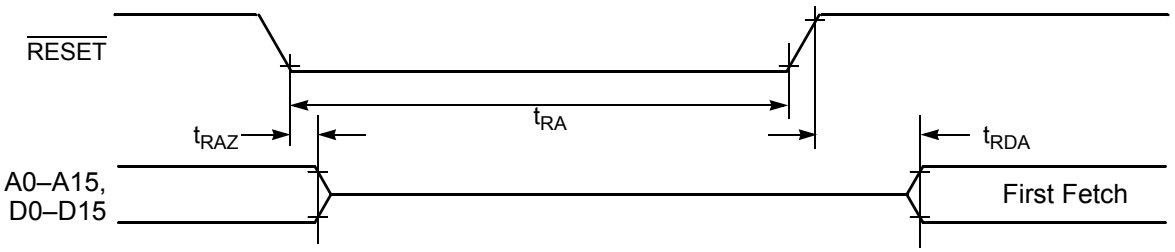

Figure 10-5 Asynchronous Reset Timing

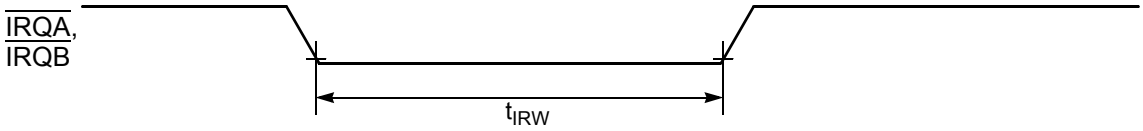

Figure 10-6 External Interrupt Timing (Negative Edge-Sensitive)

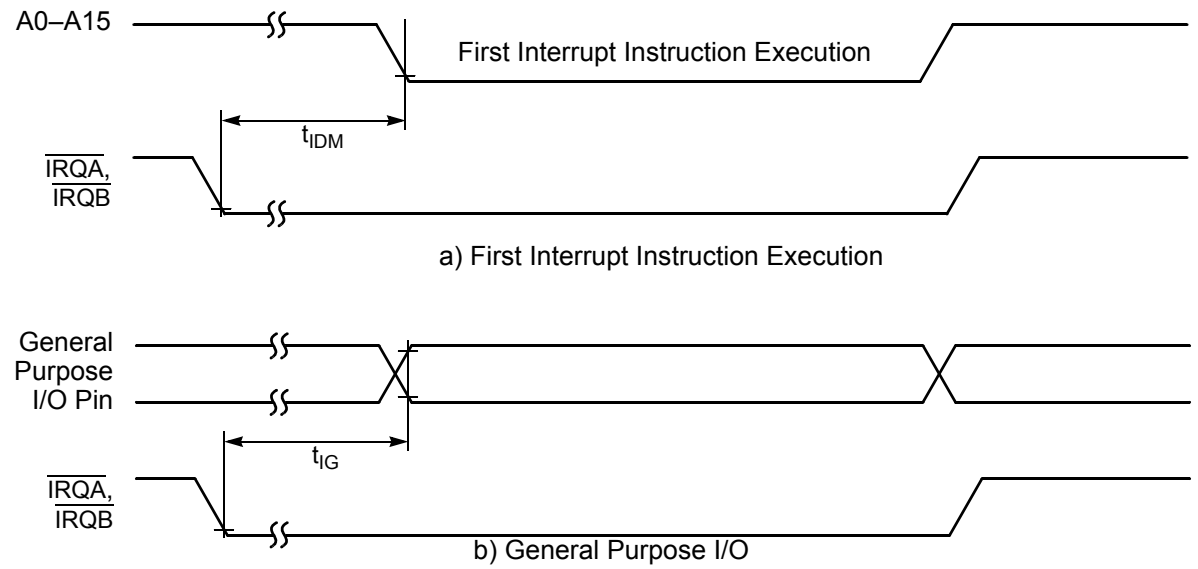

Figure 10-7 External Level-Sensitive Interrupt Timing

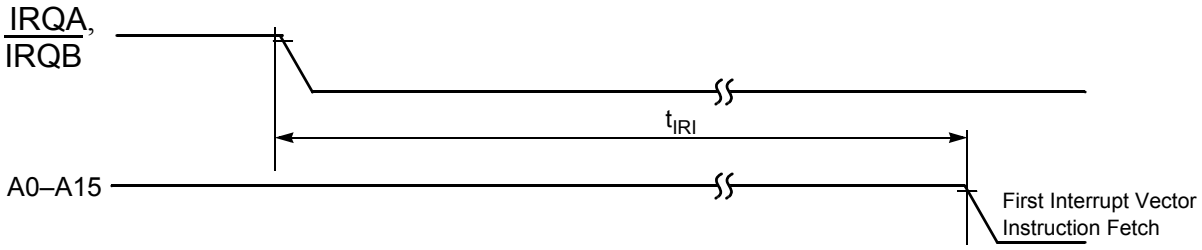

Figure 10-8 Interrupt from Wait State Timing

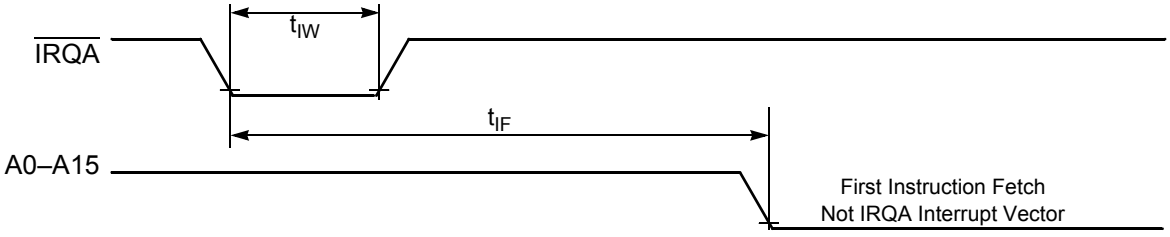

Figure 10-9 Recovery from Stop State Using Asynchronous Interrupt Timing

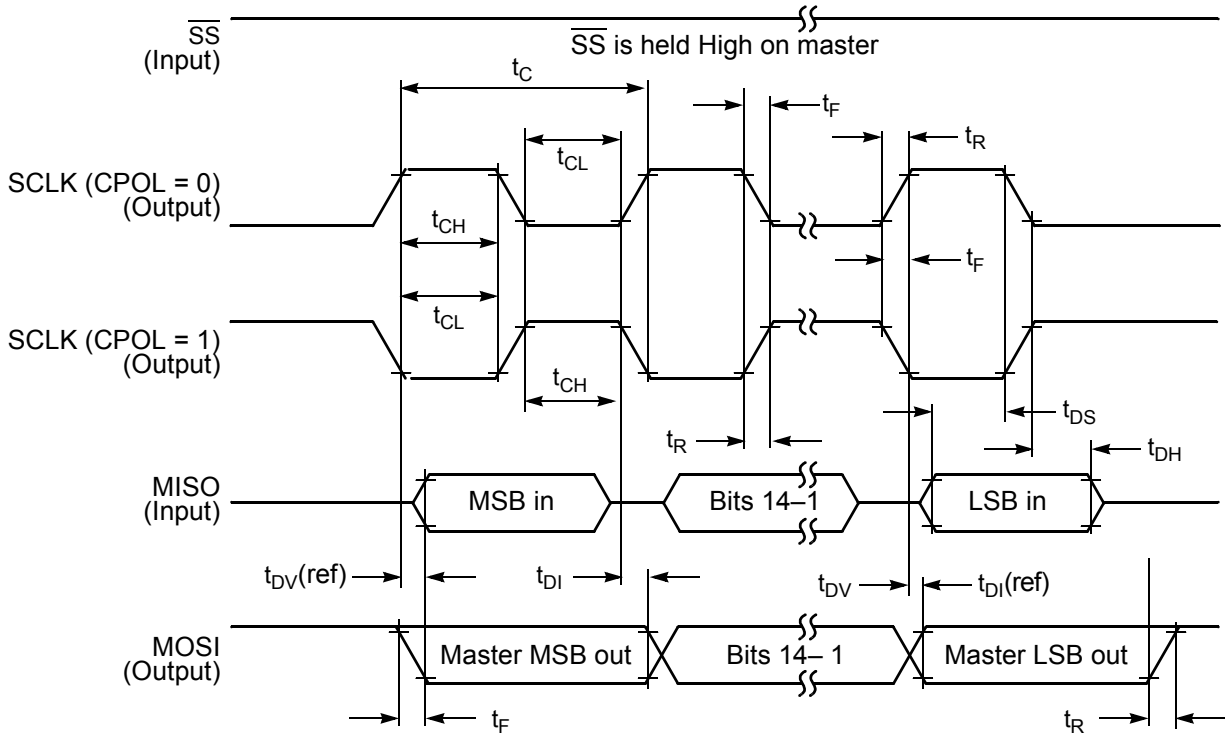

Figure 10-11 SPI Master Timing (CPHA = 1)

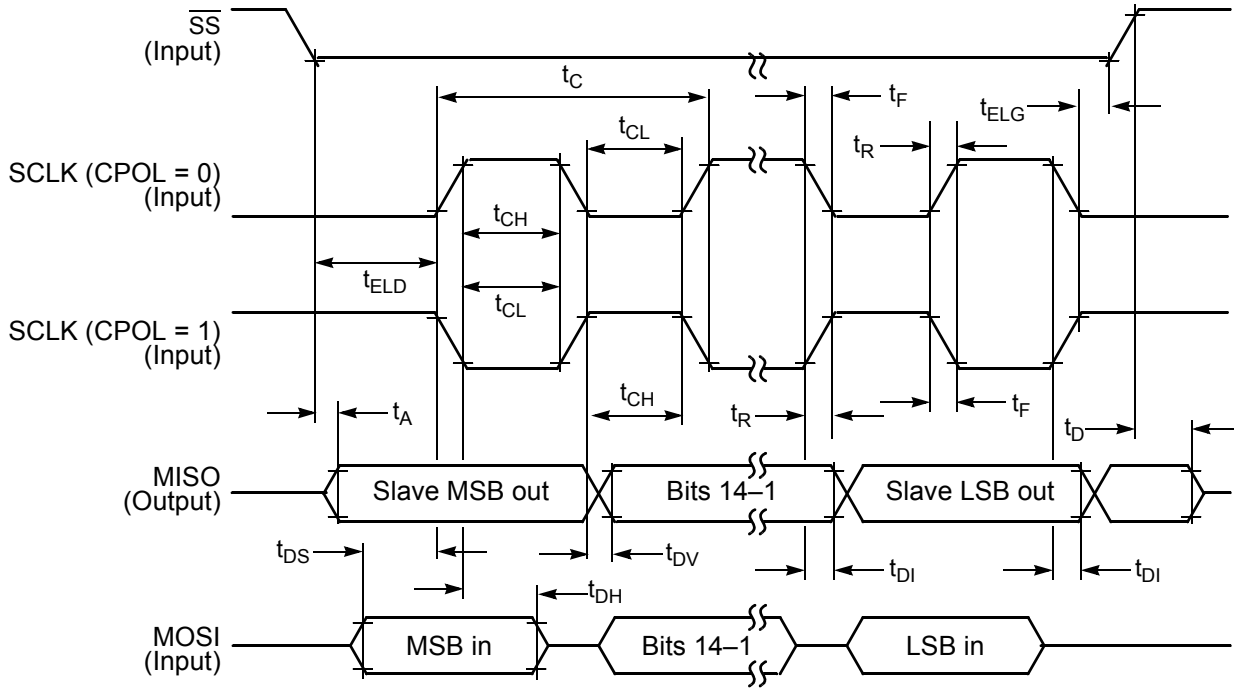

Figure 10-12 SPI Slave Timing (CPHA = 0)

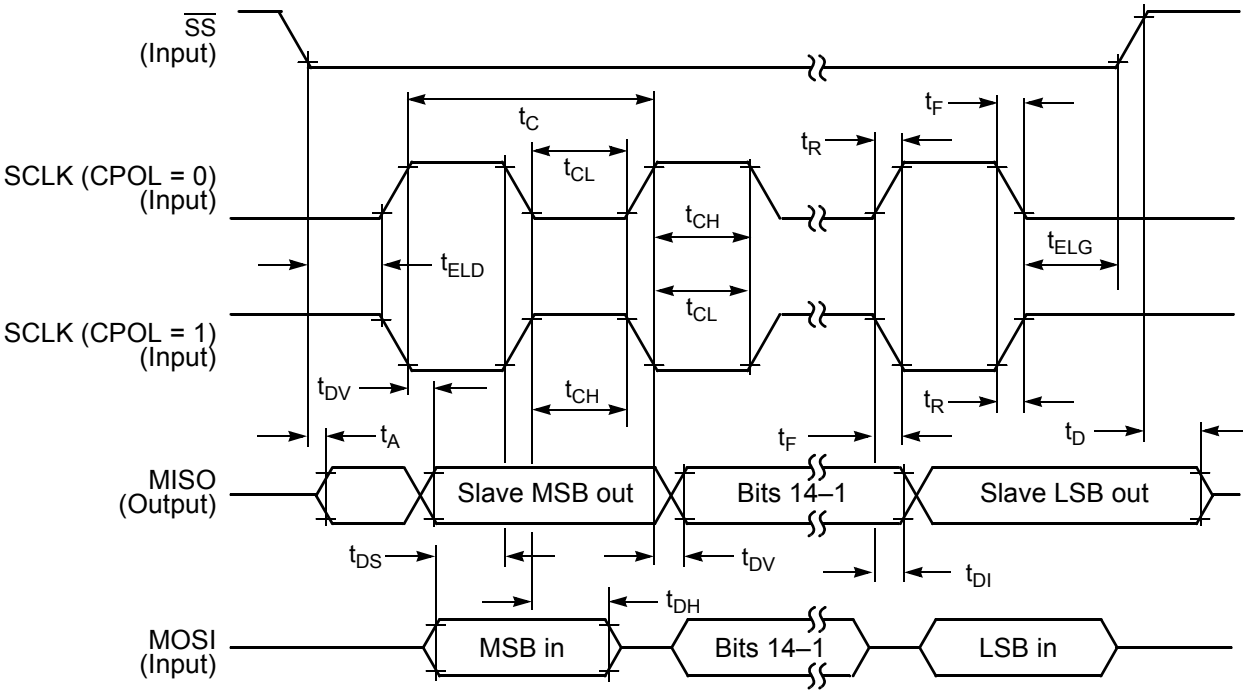

Figure 10-13 SPI Slave Timing (CPHA = 1)

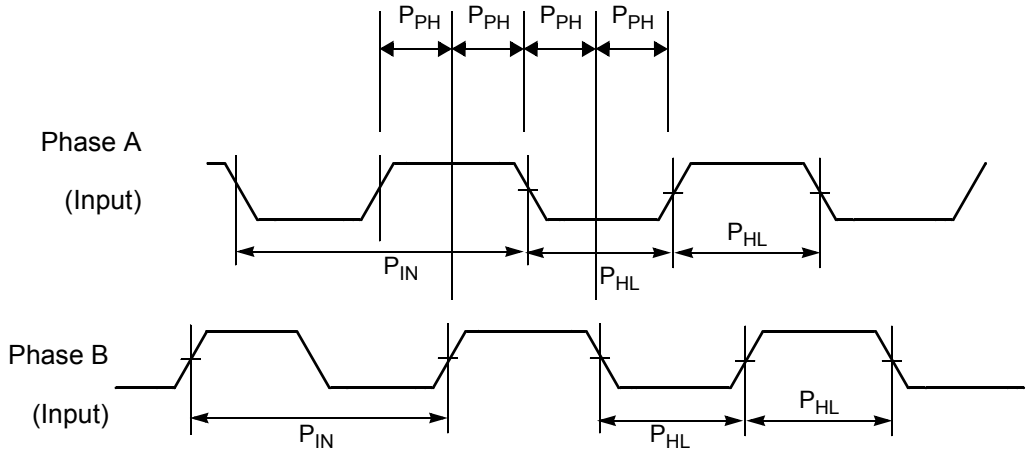

Figure 10-15 Quadrature Decoder Timing

10.12 Serial Communication Interface (SCI) Timing

Table 10-20 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-16
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-17

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock, ZCLK, in MHz, which is 60MHz for the 56F8365 device and 40MHz for the 56F8165 device.
3. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
4. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.

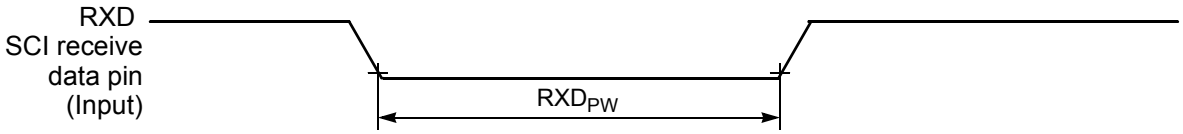

Figure 10-16 RXD Pulse Width

Table 10-22 JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK low to TDO tri-state	t_{TS}	—	30	ns	10-20
$\overline{\text{TRST}}$ assertion time	t_{TRST}	$2T^2$	—	ns	10-21

1. TCK frequency of operation must be less than 1/8 the processor rate.
2. T = processor clock period (nominally 1/60MHz)

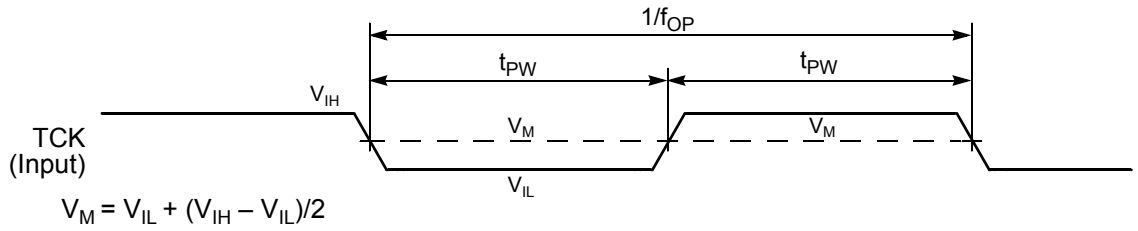

Figure 10-19 Test Clock Input Timing Diagram

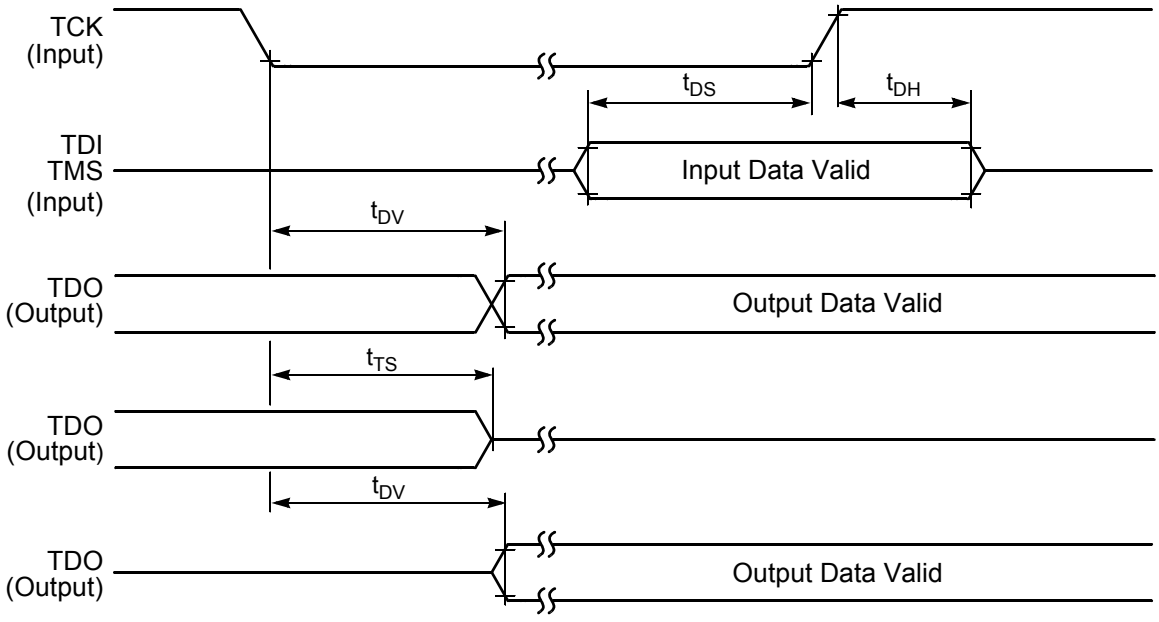

Figure 10-20 Test Access Port Timing Diagram

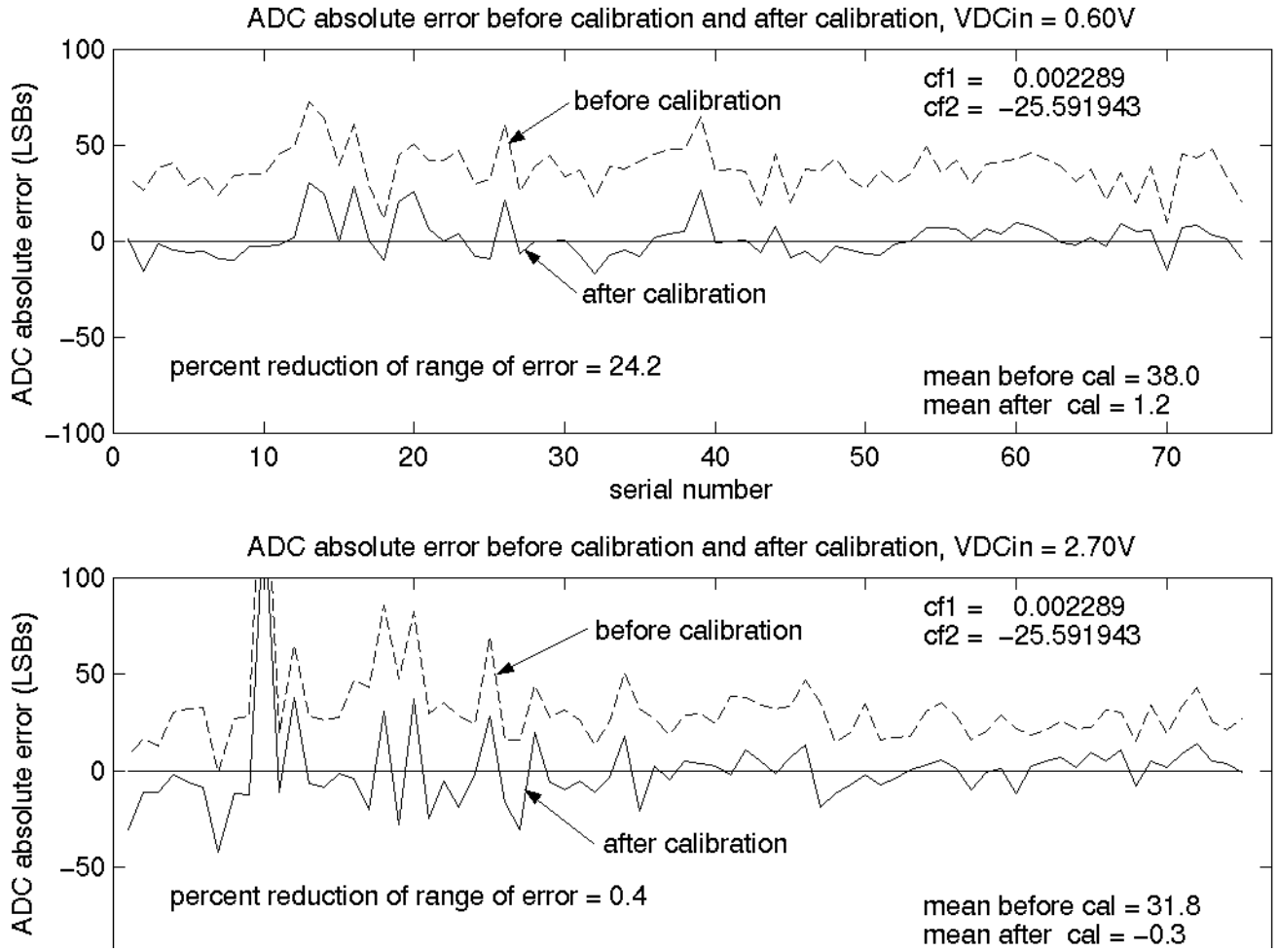

Figure 10-22 ADC Absolute Error Over Processing and Temperature Extremes Before and After Calibration for VDC_{in} = 0.60V and 2.70V

Note: The absolute error data shown in the graphs above reflects the effects of both gain error and offset error. The data was taken on 25 parts: five each from four processing corner lots as well as five from one nominally processed lot, each at three temperatures: -40°C, 27°C, and 150°C (giving the 75 data points shown above), for two input DC voltages: 0.60V and 2.70V. The data indicates that for the given population of parts, calibration significantly reduced (by as much as 24%) the collective variation (spread) of the absolute error of the population. It also significantly reduced (by as much as 38%) the mean (average) of the absolute error and thereby brought it significantly closer to the ideal value of zero. Although not guaranteed, it is believed that calibration will produce results similar to those shown above for any population of parts including those which represent processing and temperature extremes.

10.16 Equivalent Circuit for ADC Inputs

Figure 10-23 illustrates the ADC input circuit during sample and hold. S1 and S2 are always open/closed