Freescale Semiconductor - MC56F8365VFGE Datasheet

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	-
Interface	-
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	-
Voltage - Core	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
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Table 4-35 System Integration Module Registers Address Map (Continued) (SIM_BASE = $00 F350)

Register Acronym	Address Offset	Register Description
SIM_LSH_ID	$7	Least Significant Half JTAG ID
SIM_PUDR	$8	Pull-up Disable Register
		Reserved
SIM_CLKOSR	$A	Clock Out Select Register
SIM_GPS	$B	Quad Decoder 1 / Timer B / SPI 1 Select Register
SIM_PCE	$C	Peripheral Clock Enable Register
SIM_ISALH	$D	I/O Short Address Location High Register
SIM_ISALL	$E	I/O Short Address Location Low Register
SIM_PCE2	$F	Peripheral Clock Enable Register 2

Table 4-36 Power Supervisor Registers Address Map (LVI_BASE = $00 F360)

Register Acronym	Address Offset	Register Description
LVI_CONTROL	$0	Control Register
LVI_STATUS	$1	Status Register

Table 4-37 Flash Module Registers Address Map (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
FMCLKD	$0	Clock Divider Register
FMMCR	$1	Module Control Register
		Reserved
FMSECH	$3	Security High Half Register
FMSECL	$4	Security Low Half Register
		Reserved
		Reserved
FMPROT	$10	Protection Register (Banked)
FMPROTB	$11	Protection Boot Register (Banked)
		Reserved
FMUSTAT	$13	User Status Register (Banked)
FMCMD	$14	Command Register (Banked)

Table 4-38 FlexCAN Registers Address Map (Continued) (FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8165 device

Register Acronym	Address Offset	Register Description
FCMB11_DATA	$9B	Message Buffer 11 Data Register
FCMB11_DATA	$9C	Message Buffer 11 Data Register
FCMB11_DATA	$9D	Message Buffer 11 Data Register
FCMB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved
FCMB12_CONTROL	$A0	Message Buffer 12 Control / Status Register
FCMB12_ID_HIGH	$A1	Message Buffer 12 ID High Register
FCMB12_ID_LOW	$A2	Message Buffer 12 ID Low Register
FCMB12_DATA	$A3	Message Buffer 12 Data Register
FCMB12_DATA	$A4	Message Buffer 12 Data Register
FCMB12_DATA	$A5	Message Buffer 12 Data Register
FCMB12_DATA	$A6	Message Buffer 12 Data Register
		Reserved
FCMB13_CONTROL	$A8	Message Buffer 13 Control / Status Register
FCMB13_ID_HIGH	$A9	Message Buffer 13 ID High Register
FCMB13_ID_LOW	$AA	Message Buffer 13 ID Low Register
FCMB13_DATA	$AB	Message Buffer 13 Data Register
FCMB13_DATA	$AC	Message Buffer 13 Data Register
FCMB13_DATA	$AD	Message Buffer 13 Data Register
FCMB13_DATA	$AE	Message Buffer 13 Data Register
		Reserved
FCMB14_CONTROL	$B0	Message Buffer 14 Control / Status Register
FCMB14_ID_HIGH	$B1	Message Buffer 14 ID High Register
FCMB14_ID_LOW	$B2	Message Buffer 14 ID Low Register
FCMB14_DATA	$B3	Message Buffer 14 Data Register
FCMB14_DATA	$B4	Message Buffer 14 Data Register
FCMB14_DATA	$B5	Message Buffer 14 Data Register
FCMB14_DATA	$B6	Message Buffer 14 Data Register
		Reserved
FCMB15_CONTROL	$B8	Message Buffer 15 Control / Status Register
FCMB15_ID_HIGH	$B9	Message Buffer 15 ID High Register

Table 4-39 FlexCAN2 Registers Address Map (Continued)
(FC2_BASE = $00 FA00)
FlexCAN2 is NOT available in the 56F8165 device

Register Acronym	Address Offset	Register Description
FC2MB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FC2MB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FC2MB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FC2MB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FC2MB4_DATA	$63	Message Buffer 4 Data Register
FC2MB4_DATA	$64	Message Buffer 4 Data Register
FC2MB4_DATA	$65	Message Buffer 4 Data Register
FC2MB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FC2MB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FC2MB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FC2MB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FC2MB5_DATA	$6B	Message Buffer 5 Data Register
FC2MB5_DATA	$6C	Message Buffer 5 Data Register
FC2MB5_DATA	$6D	Message Buffer 5 Data Register
FC2MB5_DATA	$6E	Message Buffer 5 Data Register
		Reserved
FC2MB6_CONTROL	$70	Message Buffer 6 Control / Status Register
FC2MB6_ID_HIGH	$71	Message Buffer 6 ID High Register
FC2MB6_ID_LOW	$72	Message Buffer 6 ID Low Register
FC2MB6_DATA	$73	Message Buffer 6 Data Register
FC2MB6_DATA	$74	Message Buffer 6 Data Register
FC2MB6_DATA	$75	Message Buffer 6 Data Register
FC2MB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FC2MB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FC2MB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FC2MB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FC2MB7_DATA	$7B	Message Buffer 7 Data Register
FC2MB7_DATA	$7C	Message Buffer 7 Data Register

5.6.6.4 SCI 1 Receiver Error Interrupt Priority Level (SCI1_RERR IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.5 Reserved—Bits 7–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.6 SCI 1 Transmitter Idle Interrupt Priority Level (SCI1_TIDL IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.7 SCI 1 Transmitter Empty Interrupt Priority Level (SCI1_XMIT IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.8 SPI 0 Transmitter Empty Interrupt Priority Level (SPI0_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.2 Timer B, Channel 3 Interrupt Priority Level (TMRB3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.3 Timer B, Channel 2 Interrupt Priority Level (TMRB2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.4 Timer B, Channel 1 Interrupt Priority Level (TMRB1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.5 Timer B, Channel 0 Interrupt Priority Level (TMRB0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0

5.6.12 Fast Interrupt 0 Match Register (FIM0)

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-14 Fast Interrupt 0 Match Register (FIM0)

5.6.12.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.12.2 Fast Interrupt 0 Vector Number (FAST INTERRUPT 0)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 0. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-5**.

5.6.13 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-15 Fast Interrupt 0 Vector Address Low Register (FIVAL0)

5.6.13.1 Fast Interrupt 0 Vector Address Low (FIVAL0)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAH0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.29 Reserved—Base + 1C

5.6.30 ITCN Control Register (ICTL)

Base + $1D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	INT	IPIC		VAB							INT_DIS	1	$\overline{\text{IRQB}}$ STATE	$\overline{\text{IRQA}}$ STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
Write																
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0

Figure 5-26 ITCN Control Register (ICTL)

5.6.30.1 Interrupt (INT)—Bit 15

This *read-only* bit reflects the state of the interrupt to the 56800E core.

- 0 = No interrupt is being sent to the 56800E core
- 1 = An interrupt is being sent to the 56800E core

5.6.30.2 Interrupt Priority Level (IPIC)—Bits 14–13

These *read-only* bits reflect the state of the new interrupt priority level bits being presented to the 56800E core at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

- 00 = Required nested exception priority levels are 0, 1, 2, or 3
- 01 = Required nested exception priority levels are 1, 2, or 3
- 10 = Required nested exception priority levels are 2 or 3
- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.3 FlexCAN2 Wake Up Interrupt Priority Level (FlexCAN2_WKUP IPL)—Bits 5 - 4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.4 FlexCAN2 Error Interrupt Priority Level (FlexCAN2_ERR IPL)—Bits 3 - 2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.5 FlexCAN2 Bus-Off Interrupt Priority Level (FlexCAN2_BOFF IPL)—Bits 1 - 0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled except the core IRQs with fixed priorities:

- Illegal Instruction

- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

Part 6 System Integration Module (SIM)

6.1 Introduction

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features. The system integration module is responsible for the following functions:

- Reset sequencing
- Clock generation & distribution
- Stop/Wait control
- Pull-up enables for selected peripherals
- System status registers
- Registers for software access to the JTAG ID of the chip
- Enforcing Flash security

These are discussed in more detail in the sections that follow.

6.2 Features

The SIM has the following features:

- Flash security feature prevents unauthorized access to code/data contained in on-chip Flash memory
- Power-saving clock gating for peripheral
- Three power modes (Run, Wait, Stop) to control power utilization
  - Stop mode shuts down the 56800E core, system clock, peripheral clock, and PLL operation
  - Stop mode entry can optionally disable PLL and Oscillator (low power vs. fast restart); must be explicitly done
  - Wait mode shuts down the 56800E core and unnecessary system clock operation
  - Run mode supports full part operation
- Controls to enable/disable the 56800E core WAIT and STOP instructions
- Calculates base delay for reset extension based upon POR or $\overline{\text{RESET}}$ operations. Reset delay will be 3 x 32 clocks (phased release of reset) for reset, except for POR, which is 2^21 clock cycles

The reset state for MB and MA will depend on the Flash secured state. See **Part 4.2** and **Part 7** for detailed information on how the Operating Mode Register (OMR) MA and MB bits operate in this device. For additional information on the EX bit, see **Part 4.4**. For all other bits, see the **DSP56F800E Reference Manual**.

Note: The OMR is not a Memory Map register; it is directly accessible in code through the acronym OMR.

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00 F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.8
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.9
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.10
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10
Base + $F	SIM_PCE2	Peripheral Clock Enable Register 2	6.5.11

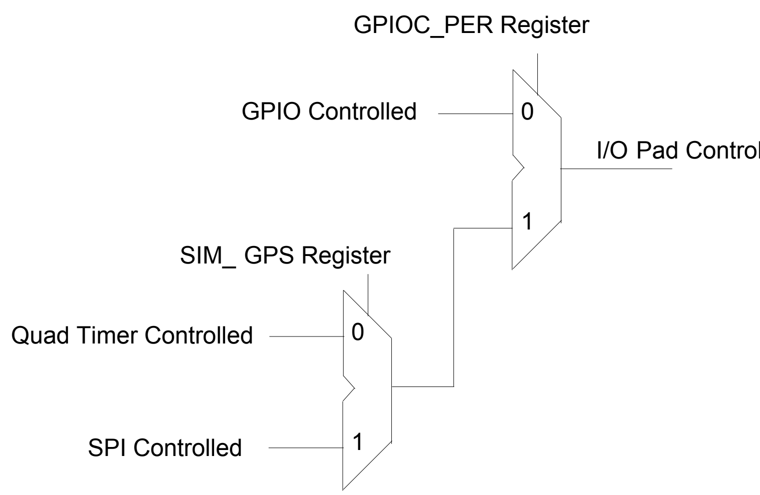

Figure 6-10 Overall Control of GPIOC Pads Using SIM_GPS Control

Table 6-2 Control of GPIOC Pads Using SIM_GPS Control [1]

Pin Function	Control Registers				Comments
	GPIOC_PER	GPIOC_DTR	SIM_GPS	Quad Timer SCR Register OEN bits	
GPIO Input	0	0	—	—	
GPIO Output	0	1	—	—	
Quad Timer Input / Quad Decoder Input [2]	1	—	0	0	See the "Switch Matrix for Inputs to the Timer" table in the **56F8300 Peripheral User Manual** for the definition of timer inputs based on the Quad Decoder mode configuration.
Quad Timer Output / Quad Decoder Input [3]	1	—	0	1	
SPI input	1	—	1	—	See SPI controls for determining the direction of each of the SPI pins.
SPI output	1	—	1	—	

1. This applies to the four pins that serve as Quad Decoder / Quad Timer / SPI / GPIOC functions. A separate set of control bits is used for each pin.
2. Reset configuration
3. Quad Decoder pins are always inputs and function in conjunction with the Quad Timer pins.

Two Input/Output pins associated with GPIOD can function as GPIO, EMI (default peripheral) or CAN2 signals. GPIO is the default and is enabled/disabled via the GPIOD_PER, as shown in **Figure 6-11** and **Table 6-3**. When GPIOD[1:0] are programmed to operate as peripheral input/output, then the choice between EMI and CAN2 inputs/outputs is made here in the GPS.

6.8 Stop and Wait Mode Disable Function

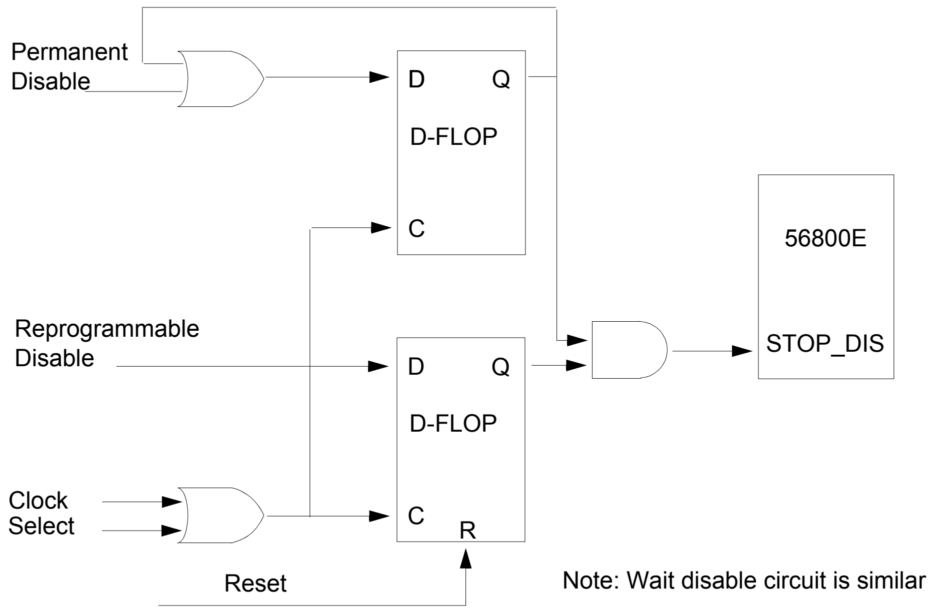

Figure 6-17 Internal Stop Disable Circuit

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the oscillator output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL), described in **Part 6.5.1**. This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is first extended for 2^{21} clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but are always released internally on a rising edge of the system clock.

Part 7 Security Features

The 56F8365/56F8165 offers security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8365/56F8165 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port)

Table 8-3 GPIO External Signals Map (Continued)

Pins in shaded rows are not available in 56F8365 / 56F8165

Pins in italics are NOT available in the 56F8165 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOC	0	Peripheral	*PhaseA1 / TB0* / SCLK1[2]	9
	1	Peripheral	*PhaseB1 / TB1* / MOSI1[2]	10
	2	Peripheral	*Index1 / TB2* / MISO1[2]	11
	3	Peripheral	*Home1 / TB3* / $\overline{SS1}$[2]	12
	4	Peripheral	PhaseA0 / TA0	127
	5	Peripheral	PhaseB0 / TA1	128
	6	Peripheral	Index0 / TA2	1
	7	Peripheral	Home0 / TA3	2
	8	Peripheral	*ISA0*	104
	9	Peripheral	*ISA1*	105
	10	Peripheral	*ISA2*	106
GPIO D	0	GPIO	$\overline{CS2}$ / *CAN2_TX*	42
	1	GPIO	$\overline{CS3}$ / *CAN2_RX*	43
	2	GPIO	$\overline{CS4}$[1]	44
	3	GPIO	$\overline{CS5}$[1]	45
	4	GPIO	$\overline{CS6}$[1]	46
	5	GPIO	$\overline{CS7}$[1]	47
	6	Peripheral	TXD1	40
	7	Peripheral	RXD1	41
	8	N/A		
	9	N/A		
	10	Peripheral	ISB0	48
	11	Peripheral	ISB1	50
	12	Peripheral	ISB2	51

Table 10-16 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
IRQA Width Assertion to Recover from Stop State[3]	t_{IW}	1.5T	—	ns	10-9

1. In the formulas, T = clock cycle. For an operating frequency of 60MHz, T = 16.67ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.

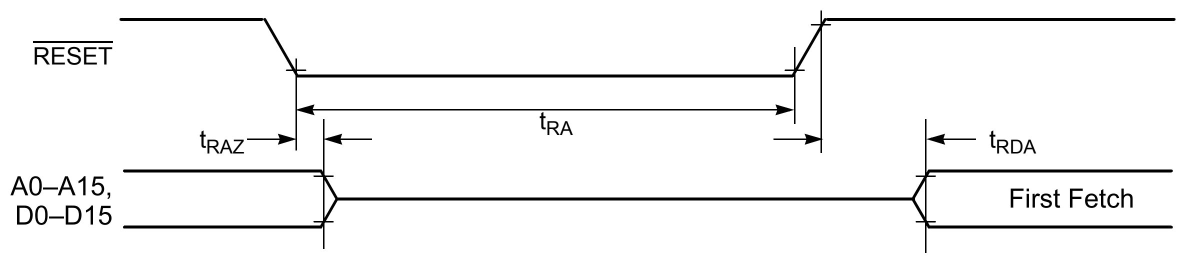

Figure 10-5 Asynchronous Reset Timing

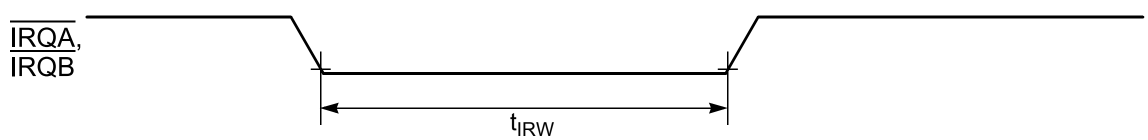

Figure 10-6 External Interrupt Timing (Negative Edge-Sensitive)

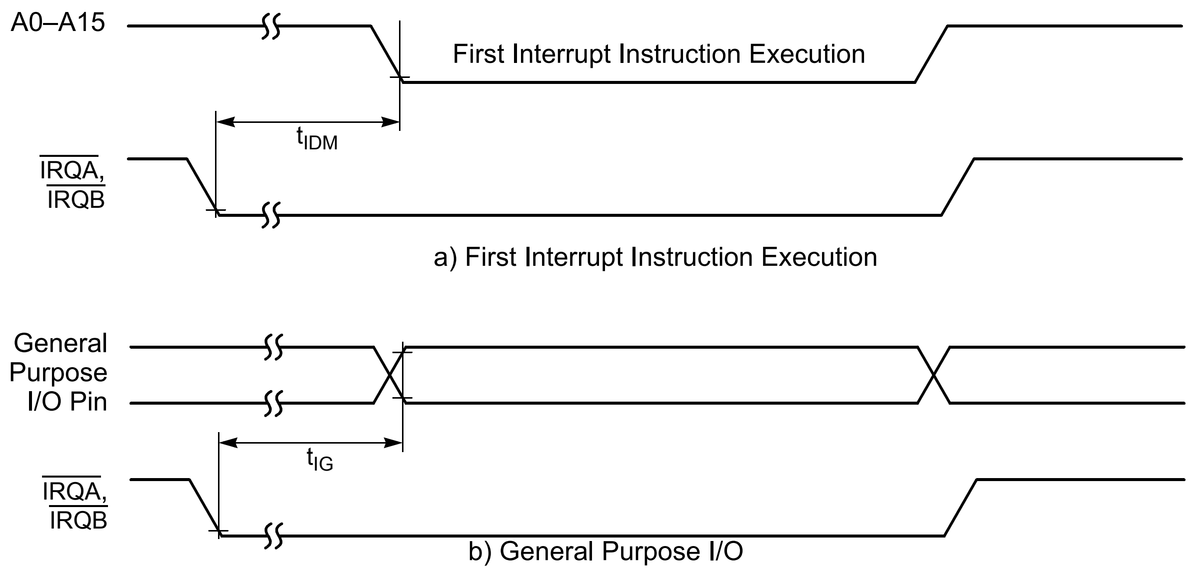

Figure 10-7 External Level-Sensitive Interrupt Timing

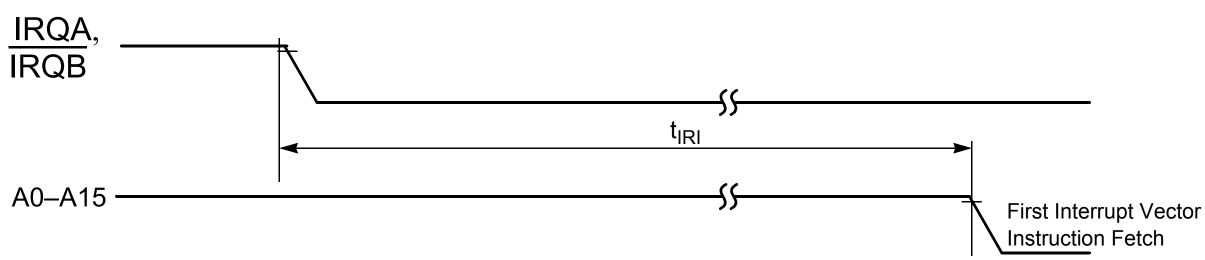

Figure 10-8 Interrupt from Wait State Timing

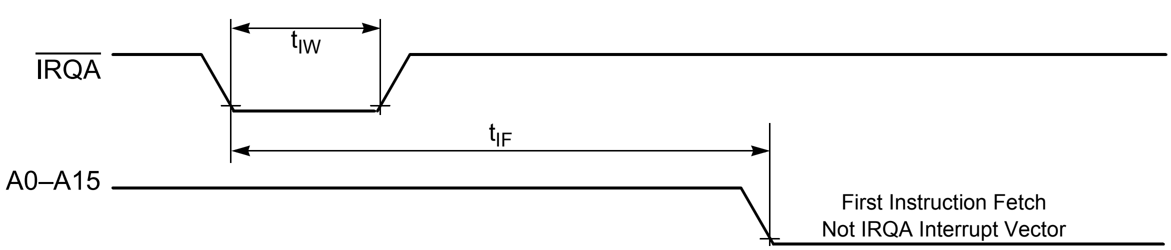

Figure 10-9 Recovery from Stop State Using Asynchronous Interrupt Timing

Table 11-2 56F8165 128-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
2	HOME0	34	PWMB2	66	NC	98	ANB2
3	V_{SS}	35	V_{SS}	67	NC	99	ANB3
4	V_{DD_IO}	36	V_{DD_IO}	68	NC	100	ANB4
5	$V_{PP}2$	37	PWMB3	69	NC	101	ANB5
6	CLKO	38	PWMB4	70	NC	102	ANB6
7	TXD0	39	PWMB5	71	OCR_DIS	103	ANB7
8	RXD0	40	TXD1	72	$V_{DDA\_OSC\_PLL}$	104	GPIOC8
9	SCLK1	41	RXD1	73	XTAL	105	GPIOC9
10	MOSI1	42	GPIOD0	74	EXTAL	106	GPIOC10
11	MISO1	43	GPIOD1	75	$V_{CAP}3$	107	GPIOE10
12	$\overline{SS1}$	44	GPIOD2	76	V_{DD_IO}	108	GPIOE11
13	$V_{CAP}4$	45	GPIOD3	77	$\overline{RSTO}$	109	GPIOE12
14	V_{DD_IO}	46	GPIOD4	78	$\overline{RESET}$	110	GPIOE13
15	GPIOA0[1]	47	GPIOD5	79	CLKMODE	111	TC0
16	GPIOA1[1]	48	ISB0	80	ANA0	112	V_{DD_IO}
17	GPIOA2[1]	49	$V_{CAP}1$	81	ANA1	113	TC1
18	GPIOA3[1]	50	ISB1	82	ANA2	114	$\overline{TRST}$
19	GPIOA4[1]	51	ISB2	83	ANA3	115	TCK
20	GPIOA5[1]	52	$\overline{IRQA}$	84	ANA4	116	TMS
21	V_{SS}	53	$\overline{IRQB}$	85	AN5	117	TDI
220	GPIOF0[1]	54	FAULTB0	86	ANA6	118	TDO
23	GPIOF1[1]	55	FAULTB1	87	ANA7	119	$V_{PP}1$
24	GPIOF2[1]	56	FAULTB2	88	NC	120	NC
25	V_{DD_IO}	57	FAULTB3	89	V_{REFLO}	121	NC
26	GPIOF3[1]	58	NC	90	V_{REFN}	122	$V_{CAP}2$
27	GPIOB0	59	V_{SS}	91	V_{REFMID}	123	$\overline{SS0}$
28	GPIOB1	60	NC	92	V_{REFP}	124	SCLK0

1. Primary function is not available in this package configuration; GPIO function must be used instead

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8365/56F8165:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1μF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8365	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8365VFG60
MC56F8365	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8365MFG60
MC56F8165	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8165VFG
MC56F8365	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 105° C	MC56F8365VFGE*
MC56F8365	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	60	-40° to + 125° C	MC56F8365MFGE*
MC56F8165	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	128	40	-40° to + 105° C	MC56F8165VFGE*

*This package is RoHS compliant.