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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	99512
Total RAM Bits	3637248
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m2gl100t-1fc1152

1.9 Revision 3.0

In revision 3.0 of this document, the Theta B/C columns and FCS325 package was updated. For more information, see Table 9, page 10 (SAR 62002).

1.10 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Table 1, page 4 was updated (SAR 59056).
- Table 7, page 8 temperature and data retention information was updated SAR (61363).
- Storage Operating Table was updated and split into three tables – Table 5, page 7, Table 7, page 8 (SAR 58725).
- Updated Theta B/C columns and FCS325 package in Table 9, page 10 (SAR 62002).
- Added 090-FCS325 thermal resistance to Table 9, page 10 (SAR 59384).
- TQ144 package was added to Table 9, page 10 (SAR 57708).
- Added PLL jitter data for the VF400 package (SAR 53162).
- Added Additional Worst Case IDD to Table 11, page 12 and Table 12, page 13 (SAR 59077).
- Table 13, page 13, Table 14, page 13, and Table 15, page 14 were added to verify Inrush currents (SAR 56348).
- Table 18, page 19 and Table 21, page 20 – I/O speeds were replaced.
- Max speed was changed in Table 41, page 26 (SAR 57221) and in Table 52, page 29 (SAR 57113).
- Minimum and Maximum DC/AC Input and Output Levels Specification, page 29 and Table 49, page 29–Table 57, page 31 were added.
- Added Cload to Table 89, page 39 (SAR 56238).
- Removed "Rs" information in DDR Timing Measurement Table 123, page 47, Table 133, page 49, and Table 144, page 52.
- Updated drive programming for M/B-LVDS outputs (SAR 58154).
- Added an inverter bubble to DDR_IN latch in Figure 10, page 70 (SAR 61418).
- QF waveform in Figure 11, page 71 was updated (SAR 59816).
- uSRAM Write Clock minimum values were updated in Table 237, page 86–Table 243, page 93 (SAR 55236).
- Fixed typo in the 32 kHz Crystal (XTAL) oscillator accuracy data section (SAR 59669).
- The "On-Chip Oscillator" section was split, and the Embedded NVM (eNVM) Characteristics, page 104 was added. Table 277, page 107–Table 281, page 109 were revised.(SARs 57898 and 59669).
- PLL VCP Frequency and conditions were added to Table 282, page 110 (SAR 57416).
- Fixed typo for PLL jitter data in the 100-400 MHz range (SAR 60727).
- Updated FCCC information in Table 282, page 110 and Table 283, page 111 (SAR 60799).
- Device 025 specifications were added to Table 283, page 111 (SAR 51625).
- JTAG Table 284, page 112 was replaced (SAR 51188).
- Flash*Freeze Table 293, page 119 was replaced (SAR 57828).
- Added support for HCSL I/O Standard for SERDES reference clocks in Table 300, page 123 and Table 301, page 123 (SAR 50748).
- Tir and Tif parameters were added to Table 303, page 124 (SAR 52203).
- Speed grade consistency was fixed in tables throughout the datasheet (SAR 50722).
- Added jitter attenuation information (SAR 59405).

1.11 Revision 1.0

The following is a summary of the changes in revision 1.0 of this document.

- The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.

2.2 References

The following documents are recommended references:

- *PB0121: IGLOO2 Product Brief*
- *DS0124: IGLOO2 Pin Descriptions*
- *PB0115: SmartFusion2 SoC FPGA Product Brief*
- *DS0115: SmartFusion2 Pin Descriptions*

All product documentation for IGLOO2 and SmartFusion2 is available at:

<http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>

<http://www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#overview>

2.3 Electrical Specifications

2.3.1 Operating Conditions

The following table lists the stress limits. Stress applied above the specified limit may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table are not implied.

Table 3 • Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC core supply voltage. Must always power this pin.	V _{DD}	−0.3	1.32	V
Power supply for charge pumps (for normal operation and programming). Must always power this pin.	V _{PP}	−0.3	3.63	V
Analog power pad for MDDR PLL	MSS_MDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	HPMS_MDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for FDDR PLL	FDDR_PLL_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_MSS_MDDR_VDDA	−0.3	3.63	V
Analog power pad for MDDR PLL	PLL0_PLL1_HPMS_MDDR_VDDA	−0.3	3.63	V
Analog power pad for PLL0–5	CCC_XX[01]_PLL_VDDA	−0.3	3.63	V
High supply voltage for PLL SerDes[01]	SERDES_[01]_PLL_VDDA	−0.3	3.63	V
Analog power for SerDes[01] PLL lane0 to lane3. This is a 2.5 V SerDes internal PLL supply.	SERDES_[01]_L[0123]_VDDAPLL	−0.3	2.75	V
TX/RX analog I/O voltage. Low voltage power for the lanes of SerDesIF0. This is a 1.2 V SerDes PMA supply.	SERDES_[01]_L[0123]_VDDAIO	−0.3	1.32	V
PCIe/PCS power supply	SERDES_[01]_VDD	−0.3	1.32	V
DC FPGA I/O buffer supply voltage for MSIO I/O bank	V _{DDI_x}	−0.3	3.63	V
DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	V _{DDI_x}	−0.3	2.75	V
I/O Input voltage for MSIO I/O bank	V _I	−0.3	3.63	V
I/O Input voltage for MSIOD/DDRIO I/O bank	V _I	−0.3	2.75	V
Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to V _{PP} .	V _{PPNVM}	−0.3	3.63	V
Storage temperature ¹	T _{STG}	−65	150	°C
Junction temperature	T _J	−55	135	°C

Figure 1 • High Temperature Data Retention (HTR)**2.3.1.1 Overshoot/Undershoot Limits**

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to $V_{CCI} + 1.0$ V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specifications do not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant with the PCI standard including the PCI overshoot/undershoot specifications.

2.3.1.2 Thermal Characteristics

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ1 through EQ3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

Table 15 • Inrush Currents at Power up, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
V_{DD}	1.26	25	32	38	48	45	77	109	mA
V_{PP}	3.46	33	49	36	180	13	36	51	mA
V_{DDI}	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to $T_J = 85\text{ }^{\circ}\text{C}$, in worst-case $V_{DD} = 1.14\text{ V}$.

Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays

Array Voltage V_{DD} (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	1.00	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

Table 95 • HSTL DC Output Voltage Specification Applicable to DDRIO I/O Bank Only

Parameter	Symbol	Min	Max	Unit
HSTL Class I				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current (MSIO and DDRIO I/O banks)	I_{OH} at V_{OH}	-8.0		mA
Output minimum sink current (MSIO and DDRIO I/O banks)	I_{OL} at V_{OL}	8.0		mA
HSTL Class II				
DC output logic high	V_{OH}	$V_{DDI} - 0.4$		V
DC output logic low	V_{OL}		0.4	V
Output minimum source DC current	I_{OH} at V_{OH}	-16.0		mA
Output minimum sink current	I_{OL} at V_{OL}	16.0		mA

Table 96 • HSTL DC Differential Voltage Specification

Parameter	Symbol	Min	Unit
DC input differential voltage	V_{ID} (DC)	0.2	V

Table 97 • HSTL AC Differential Voltage Specifications

Parameter	Symbol	Min	Max	Unit
AC input differential voltage	V_{DIFF}	0.4		V
AC differential cross point voltage	V_x	0.68	0.9	V

Table 98 • HSTL Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate	D_{MAX}	400	Mbps	AC loading: per JEDEC specifications

Table 99 • HSTL Impedance Specification

Parameter	Symbol	Typ	Unit	Conditions
Supported output driver calibrated impedance (for DDRIO I/O bank)	R_{REF}	25.5, 47.8	Ω	Reference resistance = 191 Ω
Effective impedance value (ODT for DDRIO I/O bank only)	R_{TT}	47.8	Ω	Reference resistance = 191 Ω

Table 150 • LPDDR Full Drive for DDRIO I/O Bank (Output and Tristate Buffers)

	T_{DP}		T_{ENZL}		T_{ENZH}		T_{ENHZ}		T_{ENLZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns

Minimum and Maximum DC/AC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 151 • LPDDR-LVCMOS 1.8 V Mode Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	1.710	1.8	1.89	V

Table 152 • LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high (for MSIOD and DDRIO I/O banks)	V_{IH} (DC)	$0.65 \times V_{DDI}$	1.89	V
DC input logic high (for MSIO I/O bank)	V_{IH} (DC)	$0.65 \times V_{DDI}$	3.45	V
DC input logic low	V_{IL} (DC)	-0.3	$0.35 \times V_{DDI}$	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 153 • LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC output logic high	V_{OH}	$V_{DDI} - 0.45$		V
DC output logic low	V_{OL}		0.45	V

Table 154 • LPDDR-LVCMOS 1.8 V Minimum and Maximum AC Switching Speeds

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for DDRIO I/O bank)	D_{MAX}	400	Mbps	AC loading: 17pf load, 8 ma drive and above/all slew

Table 155 • LPDDR-LVCMOS 1.8 V Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 33, 25, 20	Ω

2.3.7.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 173 • B-LVDS Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	2.375	2.5	2.625	V

Table 174 • B-LVDS DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input voltage	V_I	0	2.925	V
Input current high ¹	I_{IH} (DC)			
Input current low ¹	I_{IL} (DC)			

1. See Table 24, page 22.

Table 175 • B-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)

Parameter	Symbol	Min	Typ	Max	Unit
DC output logic high	V_{OH}	1.25	1.425	1.6	V
DC output logic low	V_{OL}	0.9	1.075	1.25	V

Table 176 • B-LVDS DC Differential Voltage Specification

Parameter	Symbol	Min	Max	Unit
Differential output voltage swing (for MSIO I/O bank only)	V_{OD}	65	460	mV
Output common mode voltage (for MSIO I/O bank only)	V_{OCM}	1.1	1.5	V
Input common mode voltage	V_{ICM}	0.05	2.4	V
Input differential voltage	V_{ID}	0.1	V_{DDI}	V

Table 177 • B-LVDS Minimum and Maximum AC Switching Speed

Parameter	Symbol	Max	Unit	Conditions
Maximum data rate (for MSIO I/O bank)	D_{MAX}	500	Mbps	AC loading: 2 pF / 100 Ω differential load

Table 178 • B-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	27	Ω

Table 179 • B-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 210 • RSDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns

Table 211 • RSDS AC Switching Characteristics for Receiver (for MSIOD I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 212 • RSDS AC Switching Characteristics for Transmitter (for MSIO I/O Bank - Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns

Table 213 • RSDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

2.3.7.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels (Applicable to MSIO I/O Bank Only)

Table 214 • LVPECL Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DDI}	3.15	3.3	3.45	V

2.3.9.4 Output DDR Module

Figure 12 • Output DDR Module

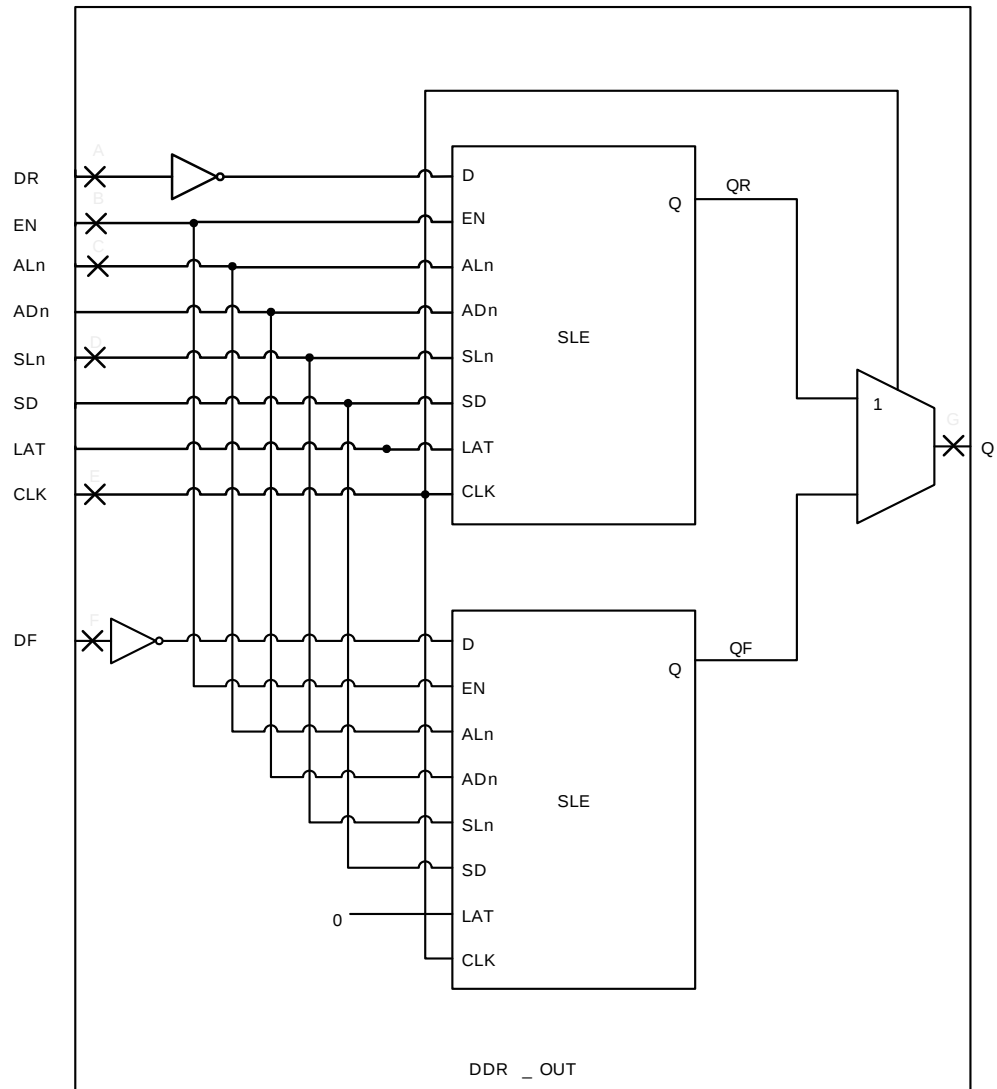
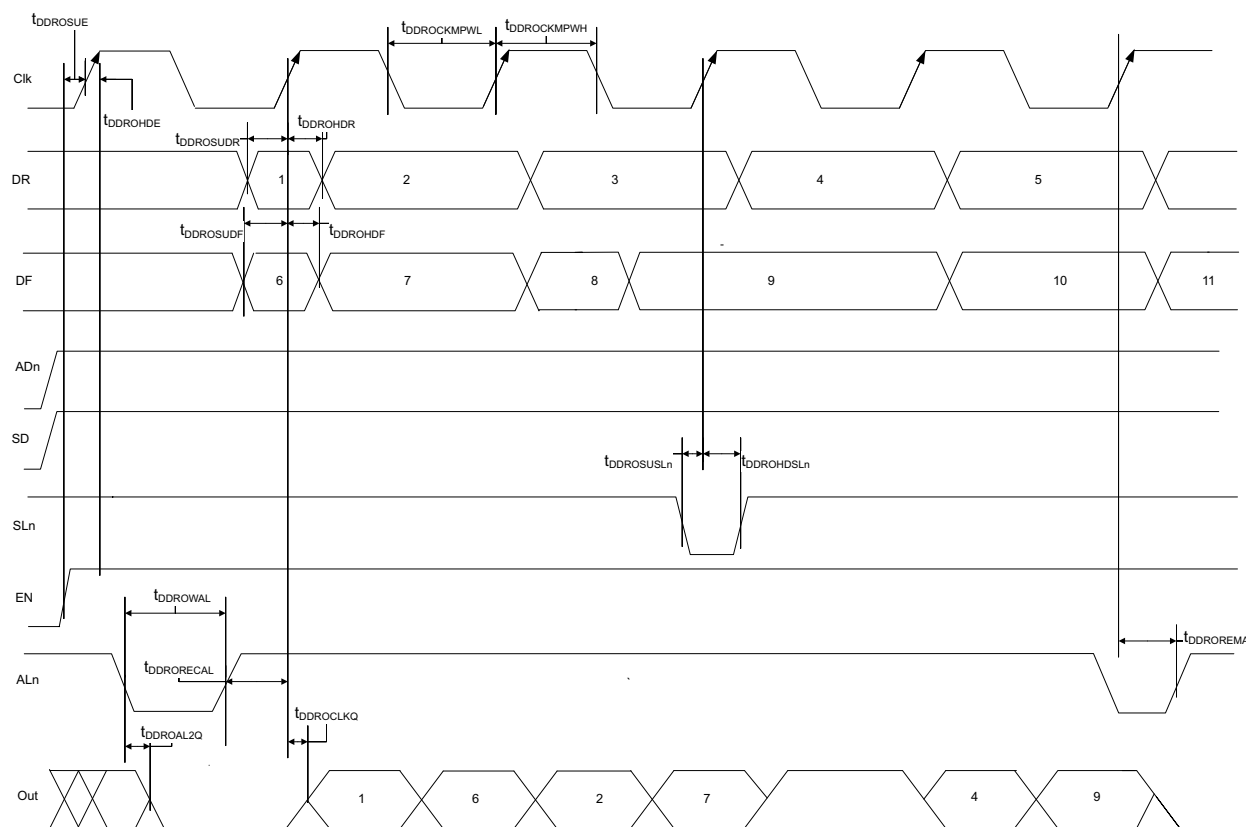


Figure 13 • Output DDR Timing Diagram



2.3.9.5 Timing Characteristics

The following table lists the output DDR propagation delays in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 222 • Output DDR Propagation Delays

Symbol	Description	Measuring Nodes (from, to)	–1	–Std	Unit
T _{DDROCLKQ}	Clock-to-out of DDR for output DDR	E, G	0.263	0.309	ns
T _{DDROSUDF}	Data_F data setup for output DDR	F, E	0.143	0.168	ns
T _{DDROSUDR}	Data_R data setup for output DDR	A, E	0.19	0.223	ns
T _{DDROHDF}	Data_F data hold for output DDR	F, E	0	0	ns
T _{DDROHDR}	Data_R data hold for output DDR	A, E	0	0	ns
T _{DDROSUE}	Enable setup for input DDR	B, E	0.419	0.493	ns
T _{DDROHE}	Enable hold for input DDR	B, E	0	0	ns
T _{DDROSUSLN}	Synchronous load setup for input DDR	D, E	0.196	0.231	ns
T _{DDROHSLN}	Synchronous load hold for input DDR	D, E	0	0	ns
T _{DDROAL2Q}	Asynchronous load-to-out for output DDR	C, G	0.528	0.621	ns
T _{DDROREMA}	Asynchronous load removal time for output DDR	C, E	0	0	ns
T _{DDRORECA}	Asynchronous load recovery time for output DDR	C, E	0.034	0.04	ns

2.3.12.2 FPGA Fabric Micro SRAM (μ SRAM)

The following table lists the μ SRAM in 64×18 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 237 • μ SRAM (RAM64x18) in 64×18 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}	0.266		0.313		ns
Read access time without pipeline register		1.677		1.973		ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}	2.036		2.396		ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}	0.839		0.987		ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns

Table 237 • μ SRAM (RAM64x18) in 64 × 18 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 64 × 16 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 238 • μ SRAM (RAM64x16) in 64 × 16 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.091		0.107		ns
Read address hold time in asynchronous mode		–0.778		–0.915		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	–0.65		–0.765		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.036		2.396	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.983	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns

Table 241 • μ SRAM (RAM256x4) in 256 × 4 Mode (continued)

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Write address hold time	$T_{ADDRCHD}$	0.245		0.288		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	-0.03		-0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 512 × 2 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 242 • μ SRAM (RAM512x2) in 512 × 2 Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.27		0.31	ns
Read access time without pipeline register			1.76		2.08	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.96		2.306		ns
Read address hold time in synchronous mode	T_{ADDRHD}	0.137		0.161		ns
Read address hold time in asynchronous mode		-0.58		-0.68		ns
Read enable setup time	T_{RDENSU}	0.278		0.327		ns
Read enable hold time	T_{RDENHD}	0.057		0.067		ns
Read block select setup time	T_{BLKSU}	1.839		2.163		ns
Read block select hold time	T_{BLKHD}	-0.65		-0.77		ns
Read block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		2.14		2.52	ns
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	-0.02		-0.03		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.83		0.98	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns

Table 259 • 2 Step IAP Programming (Fabric Only)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	302672	4	39	6	Sec	
010	568784	7	45	12	Sec	
025	1223504	14	55	23	Sec	
050	2424832	29	74	40	Sec	
060	2418896	39	83	50	Sec	
090	3645968	60	106	73	Sec	
150	6139184	100	154	120	Sec	

Table 260 • 2 Step IAP Programming (eNVM Only)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	137536	2	59	5	Sec	
010	274816	4	98	11	Sec	
025	274816	4	100	10	Sec	
050	2,78,528	3	107	9	Sec	
060	268480	5	98	22	Sec	
090	544496	10	174	43	Sec	
150	544496	10	175	44	Sec	

Table 261 • 2 Step IAP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size		Authenticate	Program	Verify	Unit
	Bytes					
005	439296	6	78	11	Sec	
010	842688	11	122	21	Sec	
025	1497408	19	135	32	Sec	
050	2695168	32	158	48	Sec	
060	2686464	43	159	70	Sec	
090	4190208	68	258	115	Sec	
150	6682768	109	308	162	Sec	

The following table lists the IGLOO2 DEVRST_N to functional times in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 292 • DEVRST_N to Functional Times for IGLOO2

Symbol	From	To	Description	Maximum Power-up to Functional Time for IGLOO2 (uS)						
				005	010	025	050	060	090	150
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	116	113	113	115	115	114
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	V_{DD} at its minimum threshold level to output	314	353	314	307	343	341	341
$T_{DEVRST2POR}$	DEVRST_N	POWER_ON_RESET_N	V_{DD} at its minimum threshold level to fabric	200	238	201	195	230	229	227
$T_{DEVRST2WPU}$	DEVRST_N	DDRIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIO Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215
	DEVRST_N	MSIOD Inbuf weak pull	DEVRST_N to Inbuf weak pull	208	202	197	193	216	215	215

Table 293 • Flash*Freeze Entry and Exit Times (continued)

Parameter	Symbol	Entry/Exit Timing FCLK = 100MHz		Entry/Exit Timing FCLK = 3 MHz	Unit	Conditions
		005, 010, 025, 060, 090, and 150	050	All Devices		
Exit time with respect to the fabric PLL lock ¹	TFF_EXIT	1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = ON during F*F
		1.5	1.5	1.5	ms	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit
Exit time with respect to the fabric buffer output	TFF_EXIT	21	15	21	μs	eNVM and MSS/HPMS PLL = ON during F*F
		65	55	65	μs	eNVM and MSS/HPMS PLL = OFF during F*F and both are turned back on at exit

1. PLL Lock Delay set to 1024 cycles (default).

2.3.28 DDR Memory Interface Characteristics

The following table lists the DDR memory interface characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 294 • DDR Memory Interface Characteristics

Standard	Supported Data Rate		Unit
	Min	Max	
DDR3	667	667	Mbps
DDR2	667	667	Mbps
LPDDR	50	400	Mbps

2.3.29 SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

The following table lists the SFP transceiver electrical characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 295 • SFP Transceiver Electrical Characteristics

Pin	Direction	Differential Peak-Peak Voltage		Unit
		Min	Max	
RD+/- ¹	Output	1600	2400	mV
TD+/- ²	Input	350	2400	mV

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance—differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	μs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV

The following table lists the SerDes reference clock AC specifications in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 299 • SerDes Reference Clock AC Specifications

Parameter	Symbol	Min	Max	Unit
Reference clock frequency	F_{REFCLK}	100	160	MHz
Reference clock rise time	T_{RISE}	0.6	4	V/ns
Reference clock fall time	T_{FALL}	0.6	4	V/ns
Reference clock duty cycle	T_{CYC}	40	60	%
Reference clock mismatch	$M_{MREFCLK}$	-300	300	ppm
Reference spread spectrum clock	SSC_{ref}	0	5000	ppm

Table 300 • HCSL Minimum and Maximum DC Input Levels (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
Recommended DC Operating Conditions					
Supply voltage	V_{DDI}	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
DC Input voltage	V_I	0		2.625	V
HCSL Differential Voltage Specification					
Input common mode voltage	V_{ICM}	0.05		2.4	V
Input differential voltage	V_{IDIFF}	100		1100	mV

Table 301 • HCSL Minimum and Maximum AC Switching Speeds (Applicable to SerDes REFCLK Only)

Parameter	Symbol	Min	Typ	Max	Unit
HCSL AC Specifications					
Maximum data rate (for MSIO I/O bank)	F_{MAX}			350	Mbps
HCSL Impedance Specifications					
Termination resistance	R_t		100		Ω

2.3.31 SmartFusion2 Specifications

2.3.31.1 MSS Clock Frequency

The following table lists the maximum frequency for MSS main clock in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 302 • Maximum Frequency for MSS Main Clock

Symbol	Description	-1	-Std	Unit
M3_CLK	Maximum frequency for the MSS main clock	166	142	MHz

2.3.31.2 SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, see Figure 21, page 125.

The following table lists the I²C characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Table 303 • I²C Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	-0.3		0.8	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Input high voltage	V_{IH}	2		3.45	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Hysteresis of schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	V_{HYS}	$0.05 \times V_{DDI}$			V	See Table 28, page 23 for more information.
Input current high	I_{IL}			10	μA	See Single-Ended I/O Standards, page 24 for more information.
Input current low	I_{IH}			10	μA	See Single-Ended I/O Standards, page 24 for more information.
Input rise time	T_{ir}			1000	ns	Standard mode
				300	ns	Fast mode
Input fall time	T_{if}			300	ns	Standard mode
				300	ns	Fast mode
Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	V_{OL}			0.4	V	See Single-Ended I/O Standards, page 24 for more information. I/O standard used for illustration: MSIO bank-LVTTL 8 mA low drive.
Pin capacitance	C_{in}			10	pF	$V_{IN} = 0$, $f = 1.0\text{ MHz}$
Output fall time from V_{IHMin} to V_{ILMax}^1	t_{OF}^1		21.04		ns	V_{IHmin} to V_{ILMax} , $C_{LOAD} = 400\text{ pF}$
			5.556		ns	V_{IHmin} to V_{ILMax} , $C_{LOAD} = 100\text{ pF}$
Output rise time from V_{ILMax} to V_{IHMin}^1	t_{OR}^1		19.887		ns	V_{ILMax} to V_{IHmin} , $C_{LOAD} = 400\text{ pF}$
			5.218		ns	V_{ILMax} to V_{IHmin} , $C_{LOAD} = 100\text{ pF}$
Output buffer maximum pull-down resistance ^{2, 3}	$R_{pull-up}^{2,3}$			50	Ω	
Output buffer maximum pull-up resistance ^{2, 4}	$R_{pull-down}^{2,4}$			131.25	Ω	

2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 308 • MMUART Characteristics

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

2.3.35 IGLOO2 Specifications

2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 309 • Maximum Frequency for HPMS Main Clock

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 310 • SPI Characteristics for All Devices

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			μs	
	SPI_[0 1]_CLK = PCLK/32	0.19			μs	
	SPI_[0 1]_CLK = PCLK/64	0.39			μs	
	SPI_[0 1]_CLK = PCLK/128	0.77			μs	