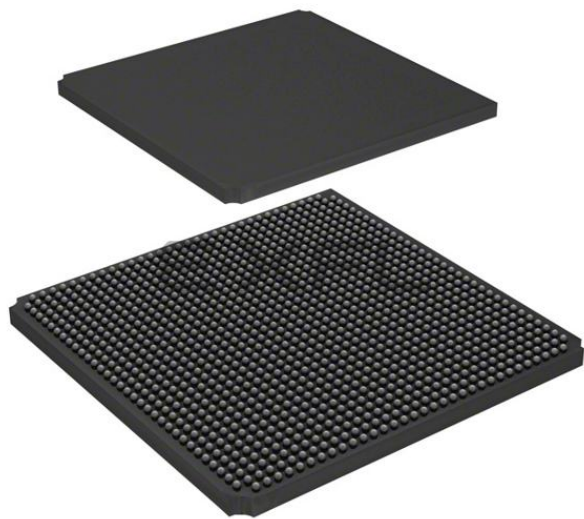




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	99512
Total RAM Bits	3637248
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m2gl100ts-1fcg1152i

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Table 15 • Inrush Currents at Power up, $-40\text{ }^{\circ}\text{C} \leq T_J \leq 100\text{ }^{\circ}\text{C}$ – Typical Process

Power Supplies	Voltage (V)	005	010	025	050	060	090	150	Unit
V_{DD}	1.26	25	32	38	48	45	77	109	mA
V_{PP}	3.46	33	49	36	180	13	36	51	mA
V_{DDI}	2.62	134	141	161	187	93	272	388	mA
Number of banks		7	8	8	10	10	9	19	

2.3.3 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delays normalized to $T_J = 85\text{ }^{\circ}\text{C}$, in worst-case $V_{DD} = 1.14\text{ V}$.

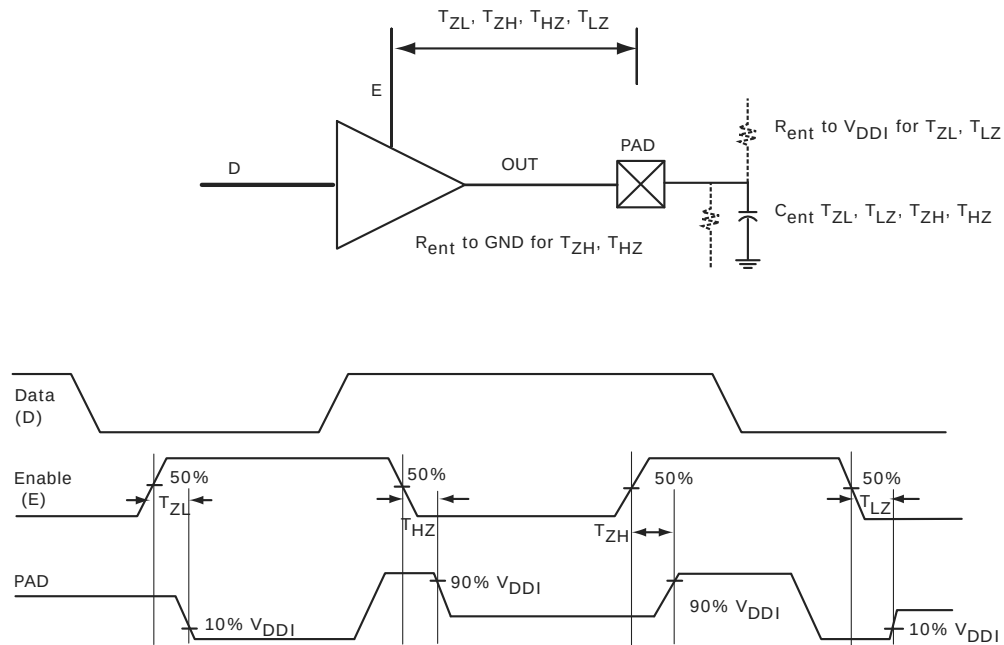
Table 16 • Average Junction Temperature and Voltage Derating Factors for Fabric Timing Delays

Array Voltage V_{DD} (V)	$-40\text{ }^{\circ}\text{C}$	$0\text{ }^{\circ}\text{C}$	$25\text{ }^{\circ}\text{C}$	$70\text{ }^{\circ}\text{C}$	$85\text{ }^{\circ}\text{C}$	$100\text{ }^{\circ}\text{C}$
1.14	0.83	0.89	0.92	0.98	1.00	1.02
1.2	0.75	0.80	0.83	0.89	0.91	0.93
1.26	0.69	0.73	0.76	0.81	0.83	0.85

2.3.5.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 5 • Tristate Buffer for Enable Path Test Point



2.3.5.4 I/O Speeds

This section describes the maximum data rate summary of I/O in worst-case industrial conditions. See the individual I/O standards for operating conditions.

Table 18 • Maximum Data Rate Summary Table for Single-Ended I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
PCI 3.3 V	630			Mbps
LVTTL 3.3 V	600			Mbps
LVC MOS 3.3 V	600			Mbps
LVC MOS 2.5 V	410	420	400	Mbps
LVC MOS 1.8 V	295	400	400	Mbps
LVC MOS 1.5 V	160	220	235	Mbps
LVC MOS 1.2 V	120	160	200	Mbps
LPDDR-LVC MOS 1.8 V mode			400	Mbps

Table 22 • Maximum Frequency Summary Table for Voltage-Referenced I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	DDRIO	Unit
LPDDR			200	MHz
HSTL1.5 V			200	MHz
SSTL 2.5 V	255	350	200	MHz
SSTL 1.8 V			334	MHz
SSTL 1.5 V			334	MHz

Table 23 • Maximum Frequency Summary Table for Differential I/O in Worst-Case Industrial Conditions

I/O	MSIO	MSIOD	Unit
LVPECL (input only)	450		MHz
LVDS 3.3 V	267.5		MHz
LVDS 2.5 V	267.5	350	MHz
RSDS	260	350	MHz
BLVDS	250		MHz
MLVDS	250		MHz
Mini-LVDS	260	350	MHz

Table 58 • LVCMOS 1.8 V Transmitter Characteristics for MSIO I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

Table 59 • LVCMOS 1.8 V Transmitter Characteristics for MSIOD I/O Bank

Output Drive Selection	Slew Control	T _{DP}		T _{ZL}		T _{ZH}		T _{HZ} ¹		T _{LZ} ¹		Unit
		-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

1. Delay increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

2.3.5.9 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • LVCMOS 1.5 V DC Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DDI}	1.425	1.5	1.575	V

Table 61 • LVCMOS 1.5 V DC Input Voltage Specification

Parameter	Symbol	Min	Max	Unit
DC input logic high for (MSIOD and DDRIO I/O banks)	V _{IH} (DC)	0.65 × V _{DDI}	1.575	V
DC input logic high (for MSIO I/O bank)	V _{IH} (DC)	0.65 × V _{DDI}	3.45	V
DC input logic low	V _{IL} (DC)	-0.3	0.35 × V _{DDI}	V
Input current high ¹	I _{IH} (DC)			–
Input current low ¹	I _{IL} (DC)			–

1. See Table 24, page 22.

Table 77 • LVCMOS 1.2 V AC Calibrated Impedance Option

Parameter	Symbol	Typ	Unit
Supported output driver calibrated impedance (for DDRIO I/O bank)	RODT_CAL	75, 60, 50, 40	Ω

Table 78 • LVCMOS 1.2 V AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point	V_{TRIP}	0.6	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF
Capacitive loading for data path (T_{DP})	C_{LOAD}	5	pF

Table 79 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			V_{OH} (V)	V_{OL} (V)	IOH (at V_{OH}) mA	IOL (at V_{OL}) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min	Max		
2 mA	2 mA	2 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	2	2
4 mA	4 mA	4 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	4	4
		6 mA	$V_{DDI} \times 0.75$	$V_{DDI} \times 0.25$	6	6

Note: For a detailed I/V curve, use the corresponding IBIS models:
www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.14\text{ V}$

Table 80 • LVCMOS 1.2 V Receiver Characteristics for DDRIO I/O Bank with Fixed Code (Input Buffers)

On-Die Termination (ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	2.448	2.88	2.466	2.901	ns

Table 81 • LVCMOS 1.2 V Receiver Characteristics for MSIO I/O Bank (Input Buffers)

On-Die Termination ODT)	T_{PY}		T_{PYS}		Unit
	-1	-Std	-1	-Std	
None	4.714	5.545	4.675	5.5	ns
50	6.668	7.845	6.579	7.74	ns
75	5.832	6.862	5.76	6.777	ns
150	5.162	6.073	5.111	6.014	ns

Table 198 • Mini-LVDS AC Impedance Specifications

Parameter	Symbol	Typ	Unit
Termination resistance	R_T	100	Ω

Table 199 • Mini-LVDS AC Test Parameter Specifications

Parameter	Symbol	Typ	Unit
Measuring/trip point for data path	V_{TRIP}	Cross point	V
Resistance for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	R_{ENT}	2K	Ω
Capacitive loading for enable path (T_{ZH} , T_{ZL} , T_{HZ} , T_{LZ})	C_{ENT}	5	pF

AC Switching Characteristics

Worst commercial-case conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$.

Table 200 • Mini-LVDS AC Switching Characteristics for Receiver (for MSIO I/O Bank - Input Buffers)

On-Die Termination (ODT)	T_{PY}		Unit
	-1	-Std	
None	2.855	3.359	ns
100	2.85	3.353	ns
None	2.602	3.061	ns
100	2.597	3.055	ns

Table 201 • Mini-LVDS AC Switching Characteristics for Transmitter for MSIO I/O Bank (Output and Tristate Buffers)

T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns

Table 202 • Mini-LVDS AC Switching Characteristics for Transmitter (for MSIOD I/O Bank - Output and Tristate Buffers)

	T_{DP}		T_{ZL}		T_{ZH}		T_{HZ}		T_{LZ}		Unit
	-1	-Std	-1	-Std	-1	-Std	-1	-Std	-1	-Std	
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

The following table lists the input data register propagation delays in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 219 • Input Data Register Propagation Delays

Parameter	Symbol	Measuring Nodes (from, to) ¹	-1	-Std	Unit
Bypass delay of the input register	T_{IBYP}	F, G	0.353	0.415	ns
Clock-to-Q of the input register	T_{ICLKQ}	E, G	0.16	0.188	ns
Data setup time for the input register	T_{ISUD}	A, E	0.357	0.421	ns
Data hold time for the input register	T_{IHD}	A, E	0	0	ns
Enable setup time for the input register	T_{ISUE}	B, E	0.46	0.542	ns
Enable hold time for the input register	T_{IHE}	B, E	0	0	ns
Synchronous load setup time for the input register	T_{ISUSL}	D, E	0.46	0.542	ns
Synchronous load hold time for the input register	T_{IHSL}	D, E	0	0	ns
Asynchronous clear-to-Q of the input register (ADn=1)	T_{IALN2Q}	C, G	0.625	0.735	ns
Asynchronous preset-to-Q of the input register (ADn=0)		C, G	0.587	0.69	ns
Asynchronous load removal time for the input register	$T_{IREMALN}$	C, E	0	0	ns
Asynchronous load recovery time for the input register	$T_{IRECALN}$	C, E	0.074	0.087	ns
Asynchronous load minimum pulse width for the input register	T_{IWALN}	C, C	0.304	0.357	ns
Clock minimum pulse width high for the input register	$T_{ICKMPWH}$	E, E	0.075	0.088	ns
Clock minimum pulse width low for the input register	$T_{ICKMPWL}$	E, E	0.159	0.187	ns

1. For the derating values at specific junction temperature and voltage supply levels, see Table 16, page 14 for derating values.

Table 221 • Input DDR Propagation Delays (continued)

Symbol	Description	Measuring Nodes (from, to)	-1	-Std	Unit
T _{DDRIWAL}	Asynchronous load minimum pulse width for input DDR	F, F	0.304	0.357	ns
T _{DDRICKMPWH}	Clock minimum pulse width high for input DDR	B, B	0.075	0.088	ns
T _{DDRICKMPWL}	Clock minimum pulse width low for input DDR	B, B	0.159	0.187	ns

2.3.9.4 Output DDR Module

Figure 12 • Output DDR Module

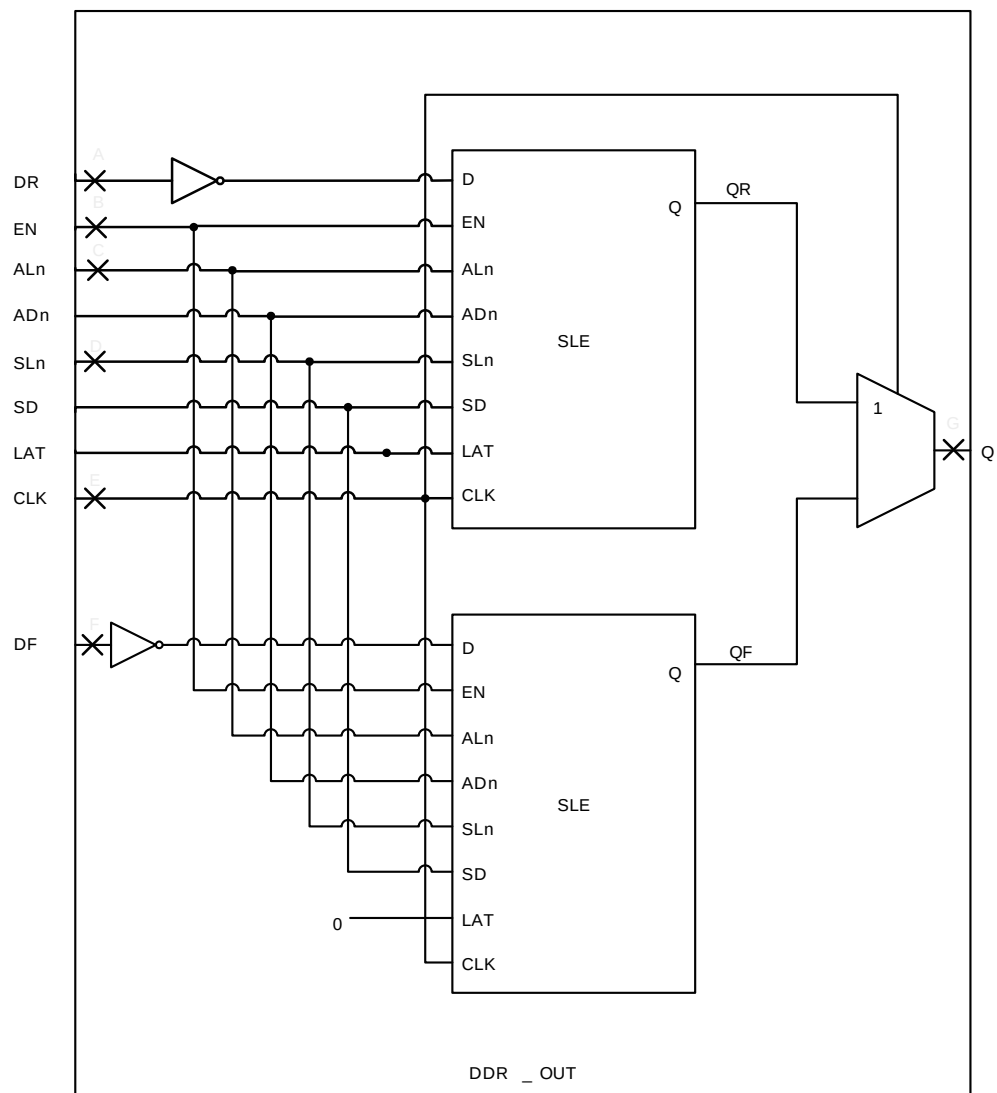


Table 231 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18 (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Block select hold time	$T_{BLKH D}$	0.216		0.254		ns
Block select to out disable time (when pipelined register is disabled)	T_{BLK2Q}		1.529		1.799	ns
Block select minimum pulse width	T_{BLKMPW}	0.186		0.219		ns
Read enable setup time	$T_{RDES U}$	0.449		0.528		ns
Read enable hold time	$T_{RDEH D}$	0.167		0.197		ns
Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLE S U}$	0.248		0.291		ns
Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	$T_{RDPLEH D}$	0.102		0.12		ns
Asynchronous reset to output propagation delay	T_{R2Q}	–	1.506	–	1.772	ns
Asynchronous reset removal time	$T_{RSTRE M}$	0.506		0.595		ns
Asynchronous reset recovery time	$T_{RSTRE C}$	0.004		0.005		ns
Asynchronous reset minimum pulse width	T_{RSTMPW}	0.301		0.354		ns
Pipelined register asynchronous reset removal time	$T_{PLRSTRE M}$	–0.279		–0.328		ns
Pipelined register asynchronous reset recovery time	$T_{PLRSTRE C}$	0.327		0.385		ns
Pipelined register asynchronous reset minimum pulse width	$T_{PLRSTMPW}$	0.282		0.332		ns
Synchronous reset setup time	$T_{SRSTS U}$	0.226		0.265		ns
Synchronous reset hold time	$T_{SRSTH D}$	0.036		0.043		ns
Write enable setup time	$T_{WES U}$	0.39		0.458		ns
Write enable hold time	$T_{WEH D}$	0.242		0.285		ns
Maximum frequency	F_{MAX}		400		340	MHz

The following table lists the RAM1K18 – dual-port mode for depth × width configuration 2K × 9 in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 232 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Clock period	T_{CY}	2.5		2.941		ns
Clock minimum pulse width high	$T_{CLKMPWH}$	1.125		1.323		ns
Clock minimum pulse width low	$T_{CLKMPWL}$	1.125		1.323		ns
Pipelined clock period	T_{PLCY}	2.5		2.941		ns
Pipelined clock minimum pulse width high	$T_{PLCLKMPWH}$	1.125		1.323		ns
Pipelined clock minimum pulse width low	$T_{PLCLKMPWL}$	1.125		1.323		ns
Read access time with pipeline register			0.334		0.393	ns
Read access time without pipeline register	T_{CLK2Q}		2.273		2.674	ns
Access time with feed-through write timing			1.529		1.799	ns

Table 239 • μ SRAM (RAM128x9) in 128 × 9 Mode (continued)

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read asynchronous reset removal time (pipelined clock)	T_{RSTREM}	–0.023		–0.027		ns
Read asynchronous reset removal time (non-pipelined clock)		0.046		0.054		ns
Read asynchronous reset recovery time (pipelined clock)	T_{RSTREC}	0.507		0.597		ns
Read asynchronous reset recovery time (non-pipelined clock)		0.236		0.278		ns
Read asynchronous reset to output propagation delay (with pipelined register enabled)	T_{R2Q}		0.835		0.982	ns
Read synchronous reset setup time	T_{SRSTSU}	0.271		0.319		ns
Read synchronous reset hold time	T_{SRSTHD}	0.061		0.071		ns
Write clock period	T_{CCY}	4		4		ns
Write clock minimum pulse width high	$T_{CCLKMPWH}$	1.8		1.8		ns
Write clock minimum pulse width low	$T_{CCLKMPWL}$	1.8		1.8		ns
Write block setup time	T_{BLKCSU}	0.404		0.476		ns
Write block hold time	T_{BLKCHD}	0.007		0.008		ns
Write input data setup time	T_{DINCSU}	0.115		0.135		ns
Write input data hold time	T_{DINCHD}	0.15		0.177		ns
Write address setup time	$T_{ADDRCSU}$	0.088		0.104		ns
Write address hold time	$T_{ADDRCHD}$	0.128		0.15		ns
Write enable setup time	T_{WECSU}	0.397		0.467		ns
Write enable hold time	T_{WECHD}	–0.026		–0.03		ns
Maximum frequency	F_{MAX}		250		250	MHz

The following table lists the μ SRAM in 128 × 8 mode in worst commercial-case conditions when $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 240 • μ SRAM (RAM128x8) in 128 × 8 Mode

Parameter	Symbol	–1		–Std		Unit
		Min	Max	Min	Max	
Read clock period	T_{CY}	4		4		ns
Read clock minimum pulse width high	$T_{CLKMPWH}$	1.8		1.8		ns
Read clock minimum pulse width low	$T_{CLKMPWL}$	1.8		1.8		ns
Read pipeline clock period	T_{PLCY}	4		4		ns
Read pipeline clock minimum pulse width high	$T_{PLCLKMPWH}$	1.8		1.8		ns
Read pipeline clock minimum pulse width low	$T_{PLCLKMPWL}$	1.8		1.8		ns
Read access time with pipeline register	T_{CLK2Q}		0.266		0.313	ns
Read access time without pipeline register			1.677		1.973	ns
Read address setup time in synchronous mode	T_{ADDRSU}	0.301		0.354		ns
Read address setup time in asynchronous mode		1.856		2.184		ns

Table 262 • SmartFusion2 Cortex-M3 ISP Programming (Fabric Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	302672	6	41	8	Sec
010	568784	10	48	14	Sec
025	1223504	21	61	29	Sec
050	2424832	39	82	50	Sec
060	2418896	44	87	54	Sec
090	3645968	66	112	79	Sec
150	6139184	108	162	128	Sec

Table 263 • SmartFusion2 Cortex-M3 ISP Programming (eNVM Only)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	137536	3	64	4	Sec
010	274816	4	104	7	Sec
025	274816	4	104	8	Sec
050	2,78,528	4	102	8	Sec
060	268480	6	102	8	Sec
090	544496	10	179	15	Sec
150	544496	10	180	15	Sec

Table 264 • SmartFusion2 Cortex-M3 ISP Programming (Fabric and eNVM)

M2S/M2GL Device	Image size Bytes	Authenticate	Program	Verify	Unit
005	439296	9	83	11	Sec
010	842688	15	129	21	Sec
025	1497408	26	143	35	Sec
050	2695168	43	163	55	Sec
060	2686464	48	165	60	Sec
090	4190208	75	266	91	Sec
150	6682768	117	318	141	Sec

The following table lists the math blocks with input register used and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 270 • Math Block with Input Register Used and Output in Bypass Mode

Parameter	Symbol	-1		-Std		Unit
		Min	Max	Min	Max	
Input register setup time	T_{MISU}	0.149		0.176		ns
Input register hold time	T_{MIHD}	0.185		0.218		ns
Synchronous reset/enable setup time	$T_{MSRSTENSU}$	0.08		0.094		ns
Synchronous reset/enable hold time	$T_{MSRSTENHD}$	-0.012		-0.014		ns
Asynchronous reset removal time	$T_{MARSTREM}$	-0.005		-0.005		ns
Asynchronous reset recovery time	$T_{MARSTREC}$	0.088		0.104		ns
Input register clock to output delay	T_{MICQ}		2.52		2.964	ns
CDIN to output delay	$T_{MCDIN2Q}$		1.951		2.295	ns

The following table lists the math blocks with input and output in bypass mode in worst commercial-case conditions when $T_J = 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 271 • Math Block with Input and Output in Bypass Mode

Parameter	Symbol	-1	-Std	Unit
		Max	Max	
Input to output delay	T_{MIQ}	2.568	3.022	ns
CDIN to output delay	$T_{MCDIN2Q}$	1.951	2.295	ns

2.3.15 Embedded NVM (eNVM) Characteristics

The following table lists the eNVM read performance in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 272 • eNVM Read Performance

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$F_{MAXREAD}$	eNVM maximum read frequency	25	25	25	25	25	25	MHz

The following table lists the eNVM page programming in worst-case conditions when $V_{DD} = 1.14\text{ V}$, $V_{PPNVM} = V_{PP} = 2.375\text{ V}$.

Table 273 • eNVM Page Programming

Symbol	Description	Operating Temperature Range						Unit
		-1	-Std	-1	-Std	-1	-Std	
T_J	Junction temperature range	-55 °C to 125 °C		-40 °C to 100 °C		0 °C to 85 °C		°C
$T_{PAGEPGM}$	eNVM page programming time	40	40	40	40	40	40	ms

2.3.17 Non-Deterministic Random Bit Generator (NRBG) Characteristics

For more information about NRBG, see *AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note*. The following table lists the NRBG in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 275 • Non-Deterministic Random Bit Generator (NRBG)

Service	Timing	Unit	Conditions	
			Prediction Resistance	Additional Input
Instantiate	85	ms	OFF	X
Generate (after Instantiate) ¹	4.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	6.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	7.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (after Instantiate)	47	ms	ON	X
Generate (subsequent) ¹	0.5 ms + (6.25 us/byte x No. of Bytes)		OFF	0
	2.0 ms + (6.25 us/byte x No. of Bytes)		OFF	64
	3.0 ms + (6.25 us/byte x No. of Bytes)		OFF	128
Generate (subsequent)	43	ms	ON	X
Reseed	40	ms		
Uninstantiate	0.16	ms		
Reset	0.10	ms		
Self test	20	ms	First time after power-up	
	6	ms	Subsequent	

1. If PUF_OFF, generate will incur additional PUF delay time for consecutive service calls.

2.3.18 Cryptographic Block Characteristics

For more information about cryptographic block and associated services, see *AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note* and *AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note*.

The following table lists the cryptographic block characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 276 • Cryptographic Block Characteristics

Service	Conditions	Timing	Unit
Any service	First certificate check penalty at boot	11.5	ms
AES128/256 (encoding / decoding) ¹	100 blocks up to 64k blocks	700	kbps

2.3.21 Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case industrial conditions when $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 282 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Parameter	Min	Typ	Max	Unit	Conditions
Clock conditioning circuitry input frequency F_{IN_CCC}	1		200	MHz	All CCC
	0.032		200	MHz	32 kHz capable CCC
Clock conditioning circuitry output frequency $F_{OUT_CCC}^1$	0.078		400	MHz	
PLL VCO frequency ²	500		1000	MHz	
Delay increments in programmable delay blocks		75	100	ps	
Number of programmable values in each programmable delay block			64		
Acquisition time		70	100	μs	$F_{IN} \geq 1\text{ MHz}$
		1	16	ms	$F_{IN} = 32\text{ kHz}$
Input duty cycle (reference clock)					Internal Feedback
	10		90	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	25		75	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 100\text{ MHz}$
	35		65	%	$100\text{ MHz} \leq F_{IN_CCC} \leq 150\text{ MHz}$
	45		55	%	$150\text{ MHz} \leq F_{IN_CCC} \leq 200\text{ MHz}$
					External Feedback (CCC, FPGA, Off-chip)
	25		75	%	$1\text{ MHz} \leq F_{IN_CCC} \leq 25\text{ MHz}$
	35		65	%	$25\text{ MHz} \leq F_{IN_CCC} \leq 35\text{ MHz}$
	45		55	%	$35\text{ MHz} \leq F_{IN_CCC} \leq 50\text{ MHz}$
	48		52	%	050 devices $F_{OUT} \leq 400\text{ MHz}$
	48		52	%	005, 010, and 025 devices $F_{OUT} < 350\text{ MHz}$
	46		54	%	005, 010, and 025 devices $350\text{ MHz} \leq F_{out} \leq 400\text{ MHz}$
Output duty cycle	48		52	%	060 and 090 devices $F_{OUT} \leq 100\text{ MHz}$
	44		52	%	060 and 090 devices $100\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
	48		52	%	150 devices $F_{OUT} \leq 120\text{ MHz}$
	45		52	%	150 devices $120\text{ MHz} \leq F_{OUT} \leq 400\text{ MHz}$
Spread Spectrum Characteristics					
Modulation frequency range	25	35	50	k	
Modulation depth range	0		1.5	%	
Modulation depth control		0.5		%	

2.3.30 SerDes Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low-pin-count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

The following table lists the transmitter parameters in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 296 • Transmitter Parameters

Symbol	Description	Min	Max	Unit
VTX-DIFF-PP	Differential swing (2.5 Gbps, 5.0 Gbps)	0.8	1.2	V
VTX-CM-AC-P	Output common mode voltage (2.5 Gbps)		20	mV
VTX-CM-AC-PP	Output common mode voltage (5.0 Gbps)		100	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%, 2.5 Gbps)	0.125		UI
	Rise and fall time (20% to 80%, 5.0 Gbps)	0.15		UI
ZTX-DIFF-DC	Output impedance—differential	80	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SerDes block (2.5 Gbps)		500 ps + 2 UI	ps
	Lane-to-lane TX skew within a SerDes block (5.0 Gbps)		500 ps + 4 UI	ps
RLTX-DIFF	Return loss differential mode (2.5 Gbps)	–10		dB
	Return loss differential mode (5.0 Gbps) 0.05 GHz to 1.25 GHz	–10		dB
	1.25 GHz to 2.5 GHz	–8		dB
RLTX-CM	Return loss common mode (2.5 Gbps, 5.0 Gbps)	–6		dB
TX-LOCK-RST	Transmit PLL lock time from reset		10	μs
VTX-AMP	100 mV setting	90	150	mV
	400 mV setting	320	480	mV
	800 mV setting	660	940	mV
	1200 mV setting	950	1400	mV

Table 303 • I2C Characteristics (continued)

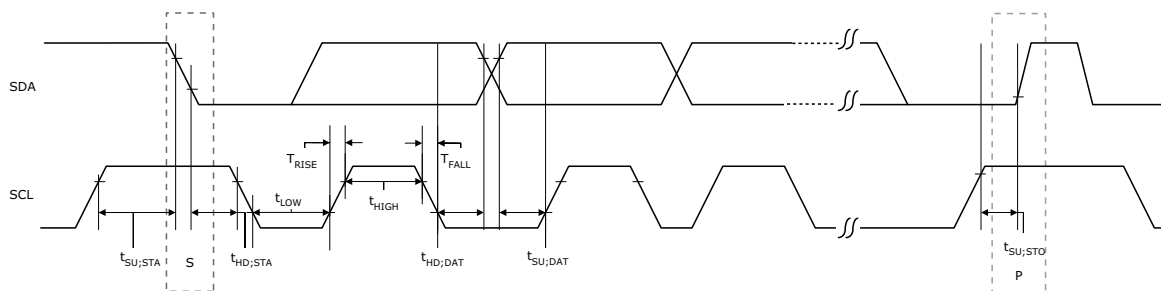
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Maximum data rate	D_{MAX}			400	Kbps	Fast mode
				100	Kbps	Standard mode
Pulse width of spikes which must be suppressed by the input filter	T_{FILT}		50		ns	Fast mode

1. These values are provided for MSIO Bank–LVTTL 8 mA Low Drive at 25 °C, typical conditions. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIX} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3. $R(PULL-DOWN-MAX) = (VOL_{spec})/IOL_{spec}$.
4. $R(PULL-UP-MAX) = (VDDImax - VOH_{spec})/IOH_{spec}$.

The following table lists the I²C switching characteristics in worst-case industrial conditions when $T_J = 100\text{ °C}$, $V_{DD} = 1.14\text{ V}$

Table 304 • I2C Switching Characteristics

Parameter	Symbol	–1	Std	Unit
		Min	Min	
Low period of I2C_x_SCL	T_{LOW}	1	1	PCLK cycles
High period of I2C_x_SCL	T_{HIGH}	1	1	PCLK cycles
START hold time	$T_{HD;STA}$	1	1	PCLK cycles
START setup time	$T_{SU;STA}$	1	1	PCLK cycles
DATA hold time	$T_{HD;DAT}$	1	1	PCLK cycles
DATA setup time	$T_{SU;DAT}$	1	1	PCLK cycles
STOP setup time	$T_{SU;STO}$	1	1	PCLK cycles

Figure 21 • I²C Timing Parameter Definition

2.3.34 MMUART Characteristics

The following table lists the MMUART characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 308 • MMUART Characteristics

Parameter	Description	–1	–Std	Unit
FMMUART_REF_CLK	Internally sourced MMUART reference clock frequency.	166	142	MHz
BAUDMMUARTTx	Maximum transmit baud rate	10.375	8.875	Mbps
BAUDMMUARTRx	Maximum receive baud rate	10.375	8.875	Mbps

2.3.35 IGLOO2 Specifications

2.3.35.1 HPMS Clock Frequency

The following table lists the maximum frequency for HPMS main clock in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 309 • Maximum Frequency for HPMS Main Clock

Symbol	Description	–1	–Std	Unit
HPMS_CLK	Maximum frequency for the HPMS main clock	166	142	MHz

2.3.35.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, see Figure 23, page 131.

The following table lists the SPI characteristics in worst-case industrial conditions when $T_J = 100\text{ }^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 310 • SPI Characteristics for All Devices

Symbol	Description	Min	Typ	Max	Unit	Conditions
SPIFMAX	Maximum operating frequency of SPI interface			20	MHz	
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12			ns	
	SPI_[0 1]_CLK = PCLK/4	24.1			ns	
	SPI_[0 1]_CLK = PCLK/8	48.2			ns	
	SPI_[0 1]_CLK = PCLK/16	0.1			μs	
	SPI_[0 1]_CLK = PCLK/32	0.19			μs	
	SPI_[0 1]_CLK = PCLK/64	0.39			μs	
	SPI_[0 1]_CLK = PCLK/128	0.77			μs	

Table 310 • SPI Characteristics for All Devices (continued)

Symbol	Description	Min	Typ	Max	Unit	Conditions
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6			ns	
	SPI_[0 1]_CLK = PCLK/4	12.05			ns	
	SPI_[0 1]_CLK = PCLK/8	24.1			ns	
	SPI_[0 1]_CLK = PCLK/16	0.05			µs	
	SPI_[0 1]_CLK = PCLK/32	0.095			µs	
	SPI_[0 1]_CLK = PCLK/64	0.195			µs	
	SPI_[0 1]_CLK = PCLK/128	0.385			µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) ¹		2.77		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) ¹		2.906		ns	I/O Configuration: LVCMOS 2.5 V - 8 mA AC loading: 35 pF test conditions: Typical voltage, 25 °C
SPI master configuration (applicable for 005, 010, 025, and 050 devices)						
sp6m	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 8.0			ns	
sp7m	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) – 2.5			ns	
sp8m	SPI_[0 1]_DI setup time ²	12			ns	
sp9m	SPI_[0 1]_DI hold time ²	2.5			ns	
SPI slave configuration (applicable for 005, 010, 025, and 050 devices)						
sp6s	SPI_[0 1]_DO setup time ²	(SPI_x_CLK_period/2) – 17.0			ns	
sp7s	SPI_[0 1]_DO hold time ²	(SPI_x_CLK_period/2) + 3.0			ns	
sp8s	SPI_[0 1]_DI setup time ²	2			ns	
sp9s	SPI_[0 1]_DI hold time ²	7			ns	