NXP USA Inc. - MK22DX128VLH5 Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22dx128vlh5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



ran identification

Field	Description	Values
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB 2M0 = 2 MB
R	Silicon revision	 Z = Initial (Blank) = Main A = Revision after main
Т	Temperature range (°C)	 V = -40 to 105 C = -40 to 85
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LF = 48 LQFP (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) LK = 80 LQFP (12 mm x 12 mm) LL = 100 LQFP (14 mm x 14 mm) MC = 121 MAPBGA (8 mm x 8 mm) LQ = 144 LQFP (20 mm x 20 mm) MD = 144 MAPBGA (13 mm x 13 mm)
СС	Maximum CPU frequency (MHz)	 5 = 50 MHz 7 = 72 MHz 10 = 100 MHz 12 = 120 MHz 15 = 150 MHz 18 = 180 MHz
N	Packaging type	 R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

MK22DN512VLH5

2.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):



reminology and guidelines

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	_	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.



3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements





3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + $(V_{IH} - V_{IL})/2$.

Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	
V _{IH}	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	_	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	—	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	—	$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I _{ICIO}	I/O pin DC injection current — single pin				1
	 V_{IN} < V_{SS}-0.3V (Negative current injection) 			mA	
	 V_{IN} > V_{DD}+0.3V (Positive current injection) 	-3	—		
		—	+3		

Table continues on the next page ...



Notes

1. Rising threshold is the sum of falling threshold and hysteresis voltage

		porating	roquiron			
Symbol	Description	Min.	Тур.	Max.	Unit	
V _{POR VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Table 3. VBAT power operating requirements

5.2.3 Voltage and current operating behaviors Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = - 9 mA	V _{DD} – 0.5	—	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -3 mA	V _{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -2 mA	V _{DD} – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -0.6 \text{ mA}$	V _{DD} – 0.5	—	V	
I _{OHT}	Output high current total for all ports	_	100	mA	
V _{OL}	Output low voltage — high drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 9 mA	—	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 3 \text{ mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 2 mA	—	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 0.6 \text{ mA}$	—	0.5	V	
I _{OLT}	Output low current total for all ports		100	mA	
l _{IN}	Input leakage current (per pin)				
	@ full temperature range	_	1.0	μA	1
	• @ 25 °C	—	0.1	μΑ	
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	_	1	μA	
I _{OZ}	Total Hi-Z (off-state) leakage current (all input pins)		4	μΑ	
R _{PU}	Internal pullup resistors	22	50	kΩ	2
R _{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method

- 2. Measured at Vinput = V_{SS}
- 3. Measured at Vinput = V_{DD}



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ -40 to 25°C	_	1.03	1.8	μA	
	• @ 50°C		1.92	7.5		
	• @ 70°C • @ 105°C		4.03	15.9		
			17.43	28.7		
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled	_	0.543	1.1	μA	
	• @ -40 to 25°C		1.36	7.58		
	• @ 50°C • @ 70°C		3.39	14.3		
	• @ 105°C		16.52	24.1		
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled		0.359	0.95	μA	
	 @ -40 to 25°C 		1.03	6.8		
	• @ 50°C • @ 70°C		2.87	15.4		
	• @ 105°C		15.20	25.3		
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V	_	0.91	1.1	μA	9
	• @ –40 to 25°C		1.1	1.35		
	• @ 50°C • @ 70°C		1.5	1.85		
	• @ 105°C		4.3	5.7		

 Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 4. Max values are measured with CPU executing DSP instructions
- 5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Includes 32 kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL





Figure 2. Run mode supply current vs. core frequency



- 3. $V_{DD} = 3.3 \text{ V}, T_A = 25 \text{ °C}, f_{OSC} = 12 \text{ MHz} \text{ (crystal)}, f_{SYS} = 48 \text{ MHz}, f_{BUS} = 48 \text{ MHz}$
- 4. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Normal run mode	9		•	
f _{SYS}	System and core clock	—	50	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f _{BUS}	Bus clock	—	50	MHz	
f _{FLASH}	Flash clock	—	25	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	
	VLPR mode ¹			•	
f _{SYS}	System and core clock	—	4	MHz	
f _{BUS}	Bus clock	—	4	MHz	
f _{FLASH}	Flash clock	—	1	MHz	
f _{ERCLK}	External reference clock	—	16	MHz	
f _{LPTMR_pin}	LPTMR clock		25	MHz	

Table continues on the next page...



Board type	Symbol	Description	64 LQFP	Unit	Notes
_	Ψ _{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	6

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air) with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
- 3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions Forced Convection (Moving Air)* with the board horizontal.
- 4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
- 5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 6. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 JTAG electricals

 Table 12. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	25	
	Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	20	—	ns
	Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns

Table continues on the next page...



4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	_	3.6	V
R _F	Internal feedback resistor	_	100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation		0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t _{start}	Crystal start-up time	—	1000	—	ms	1
V _{ec_extal32}	Externally provided input clock amplitude	700	—	V _{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The
oscillator remains enabled and XTAL32 must be left unconnected.

3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.



6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	_	7.5	18	μs	
t _{hversscr}	Sector Erase high-voltage time	—	13	113	ms	1
t _{hversblk256k}	Erase Block high-voltage time for 256 KB		104	904	ms	1

Table 19. NVM program/erase timing specifications

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands Table 20. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Read 1s Block execution time					
t _{rd1blk64k}	• 64 KB data flash	—	—	0.9	ms	
t _{rd1blk256k}	• 256 KB program flash	—	—	1.7	ms	
t _{rd1sec2k}	Read 1s Section execution time (flash sector)	_	_	60	μs	1
t _{pgmchk}	Program Check execution time	_	_	45	μs	1
t _{rdrsrc}	Read Resource execution time	_	_	30	μs	1
t _{pgm4}	Program Longword execution time	_	65	145	μs	
	Erase Flash Block execution time					2
t _{ersblk64k}	• 64 KB data flash	—	58	580	ms	
t _{ersblk256k}	• 256 KB program flash	—	122	985	ms	
t _{ersscr}	Erase Flash Sector execution time	_	14	114	ms	2
	Program Section execution time					
t _{pgmsec512}	 512 bytes flash 	—	2.4	_	ms	
t _{pgmsec1k}	• 1 KB flash	_	4.7	_	ms	
t _{pgmsec2k}	• 2 KB flash	—	9.3		ms	
t _{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t _{rdonce}	Read Once execution time	_	—	25	μs	1
t _{pgmonce}	Program Once execution time		65		μs	
t _{ersall}	Erase All Blocks execution time		250	2000	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time			30	μs	1

Table continues on the next page ...



- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 9. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 25. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t _{ADACK} = 1/
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	f _{ADACK}
TADACK		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample t	imes			
TUE	Total unadjusted	12-bit modes	—	±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	—	±1.4	±2.1		
DNL	Differential non-	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
	linearity				-0.3 to 0.5		
		 <12-bit modes 	—	±0.2			

Table continues on the next page ...



Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
INL	Integral non-	12-bit modes	—	±1.0	-2.7 to +1.9	LSB ⁴	5
	linearity				-0.7 to +0.5		
		 <12-bit modes 	—	±0.5			
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	_	-1.4	-1.8		V _{DDA}
EQ	Quantization	16-bit modes	—	-1 to 0	—	LSB ⁴	
	error	• ≤13-bit modes	_		±0.5		
ENOB	Effective number	16-bit differential mode					6
	of bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	_	bits	
		• Avg = 4	11.4	13.1	_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02	2 × ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode					7
	distortion	• Avg = 32	_	-94	_	dB	
		16-bit single-ended mode	_	-85	_	dB	
		• Avg = 32					
SFDR	Spurious free	16-bit differential mode					7
	dynamic range	• Avg = 32	82	95	—	dB	
		16-bit single-ended mode	79	90		dB	
		• Avg = 32		30		ЧD	
E _{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 25. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$



Peripheral operating requirements and behaviors



Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements Table 27. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	_	100	pF	2
١L	Output load current		1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC



Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns

Table 39. I2S/SAI master mode timing (continued)



Figure 20. I2S/SAI timing — master modes

Table 40. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





Figure 21. I2S/SAI timing — slave modes

6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

 Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	-	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns





Figure 22. I2S/SAI timing — master modes

Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



ensions



Figure 23. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W

8 Pinout

8.1 K22 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

• The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11,

K22 Sub-Family Data Sheet, Rev. 4, 08/2013.







Figure 24. K22 64 LQFP Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

K22 Sub-Family Data Sheet, Rev. 4, 08/2013.