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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 18x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pk22dn512vlh5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK22 and MK22.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K22
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
Μ	Flash memory type	 N = Program flash only X = Program flash and FlexMemory

Table continues on the next page...



reminology and guidelines

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	_	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.







3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	٥C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.



4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

- 2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
- 3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	155	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3		V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V _{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General



General

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.			μs	1
	 1.71 V/(V_{DD} slew rate) ≤ 300 μs 	—	300		
	 1.71 V/(V_{DD} slew rate) > 300 μs 	—	1.7 V / (V _{DD} slew rate)		
	VLLS0 → RUN	—	135	μs	
	• VLLS1 → RUN	—	135	μs	
	• VLLS2 → RUN		85	μs	
	• VLLS3 → RUN	—	85	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN		5.2	μs	
	• STOP \rightarrow RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8 V	_	12.98	14	mA	
	• @ 3.0 V	_	12.93	13.8	mA	

Table continues on the next page ...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ -40 to 25°C	_	1.03	1.8	μA	
	• @ 50°C		1.92	7.5		
	• @ 70°C • @ 105°C		4.03	15.9		
			17.43	28.7		
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled	_	0.543	1.1	μA	
	• @ -40 to 25°C		1.36	7.58		
	• @ 50°C • @ 70°C		3.39	14.3		
	• @ 105°C		16.52	24.1		
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled		0.359	0.95	μA	
	 @ -40 to 25°C 		1.03	6.8		
	• @ 50°C • @ 70°C		2.87	15.4		
	• @ 105°C		15.20	25.3		
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V	_	0.91	1.1	μA	9
	• @ –40 to 25°C		1.1	1.35		
	• @ 50°C • @ 70°C		1.5	1.85		
	• @ 105°C		4.3	5.7		

 Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 4. Max values are measured with CPU executing DSP instructions
- 5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Includes 32 kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



rempheral operating requirements and behaviors



Figure 4. Test clock input timing



Figure 5. Boundary scan (JTAG) timing





Figure 6. Test Access Port timing





6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
J _{cyc_fll}	FLL period jitter	_	180	_	ps	
	 f_{DCO} = 48 MHz f_{DCO} = 98 MHz 	_	150	_		
t _{fll_acquire}	FLL target frequency acquisition time	—	—	1	ms	7
	PI	L				
f _{vco}	VCO operating frequency	48.0	—	100	MHz	
I _{pll}	PLL operating current • PLL @ 96 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 48)	_	1060	_	μA	8
I _{pll}	PLL operating current • PLL @ 48 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 24)	_	600	_	μA	8
f _{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS)					9
	• f _{vco} = 48 MHz	_	120	_	ps	
	• f _{vco} = 100 MHz	_	50	—	ps	
J _{acc_pll}	PLL accumulated jitter over 1µs (RMS)					9
	• f _{vco} = 48 MHz	_	1350	_	ps	
	• f _{vco} = 100 MHz	_	600	—	ps	
D _{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time	_	_	150 × 10 ⁻⁶ + 1075(1/ f _{pll_ref})	S	10

Table 14. MCG specifications (continued)

- 1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2. 2 V <= VDD <= 3.6 V.
- 3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
- The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
- 5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
- 6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- 7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
- 9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications



6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	_	7.5	18	μs	
t _{hversscr}	Sector Erase high-voltage time	—	13	113	ms	1
t _{hversblk256k}	Erase Block high-voltage time for 256 KB		104	904	ms	1

Table 19. NVM program/erase timing specifications

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands Table 20. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Read 1s Block execution time					
t _{rd1blk64k}	• 64 KB data flash	_	—	0.9	ms	
t _{rd1blk256k}	256 KB program flash	_	—	1.7	ms	
t _{rd1sec2k}	Read 1s Section execution time (flash sector)	_	—	60	μs	1
t _{pgmchk}	Program Check execution time	_	—	45	μs	1
t _{rdrsrc}	Read Resource execution time	_	_	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	
	Erase Flash Block execution time					2
t _{ersblk64k}	• 64 KB data flash	_	58	580	ms	
t _{ersblk256k}	• 256 KB program flash	_	122	985	ms	
t _{ersscr}	Erase Flash Sector execution time	_	14	114	ms	2
	Program Section execution time					
t _{pgmsec512}	 512 bytes flash 	_	2.4	_	ms	
t _{pgmsec1k}	• 1 KB flash	_	4.7	_	ms	
t _{pgmsec2k}	• 2 KB flash	_	9.3	_	ms	
t _{rd1all}	Read 1s All Blocks execution time	_	—	1.8	ms	
t _{rdonce}	Read Once execution time	_	—	25	μs	1
t _{pgmonce}	Program Once execution time	_	65	_	μs	
t _{ersall}	Erase All Blocks execution time		250	2000	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time			30	μs	1

Table continues on the next page ...



rempheral operating requirements and behaviors

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 9. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 25. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/$
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	f _{ADACK}
TADACK		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter	for sample t	imes			
TUE	Total unadjusted	12-bit modes	—	±4	±6.8	LSB ⁴	5
	error	 <12-bit modes 	—	±1.4	±2.1		
DNL	Differential non-	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
	linearity				-0.3 to 0.5		
		 <12-bit modes 	—	±0.2			

Table continues on the next page ...



Symbol	Description	Conditions ¹ .	Min.	Typ. ²	Max.	Unit	Notes
INL	Integral non-	12-bit modes	—	±1.0	-2.7 to +1.9	LSB ⁴	5
	linearity				-0.7 to +0.5		
		 <12-bit modes 	—	±0.5			
E _{FS}	Full-scale error	12-bit modes	—	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	_	-1.4	-1.8		V _{DDA}
EQ	Quantization	16-bit modes	—	-1 to 0	—	LSB ⁴	
	error	• ≤13-bit modes	_		±0.5		
ENOB	Effective number	16-bit differential mode					6
	of bits	• Avg = 32	12.8	14.5	_	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
		• Avg = 32	12.2	13.9	_	bits	
		• Avg = 4	11.4	13.1	_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02	2 × ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode					7
	distortion	• Avg = 32	_	-94	_	dB	
		16-bit single-ended mode	_	-85	_	dB	
		• Avg = 32					
SFDR	Spurious free	16-bit differential mode					7
	dynamic range	• Avg = 32	82	95	—	dB	
		16-bit single-ended mode	79	90		dB	
		• Avg = 32		30		ЧD	
E _{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 25. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$



rempheral operating requirements and behaviors

- Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz



Typical ADC 16-bit Differential ENOB vs ADC Clock 100Hz, 90% FS Sine Input

Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode





Typical ADC 16-bit Single-Ended ENOB vs ADC Clock 100Hz, 90% FS Sine Input

Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	_	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	_	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	_	20	μA
V _{AIN}	Analog input voltage	V _{SS} – 0.3	_	V _{DD}	V
V _{AIO}	Analog input offset voltage	—	_	20	mV
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	_	5	_	mV
	• CR0[HYSTCTR] = 01		10	_	mV
	• CR0[HYSTCTR] = 10		20	_	mV
	 CR0[HYSTCTR] = 11 	_	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5			V
V _{CMPOI}	Output low	—	_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	_	40	μs

Table continues on the next page ...





Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

	Table 29.	VREF full-range	operating	requirements
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Symbol	Description	Min. Max.		Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.



- 1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
- 2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to ILoad.

6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation		25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	_	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid		8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15		ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

Table 35. Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].







Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	_	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	_	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	_	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	_	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		14	ns





Figure 17. DSPI classic SPI timing — slave mode

6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t _{BUS}	_	ns	

Table 37. Master mode DSPI timing (full voltage range)

Table continues on the next page...



rempheral operating requirements and behaviors



Figure 21. I2S/SAI timing — slave modes

6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

 Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	-	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Peripheral operating requirements and behaviors



Figure 22. I2S/SAI timing — master modes

Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



ensions



Figure 23. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W

8 Pinout

8.1 K22 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

• The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11,