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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, QSPI, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	105
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602sf2vlq6r

Table 1. MPC5606S family device comparison (continued)

Feature	MPC5602S	MPC5604S	MPC5606S
Real-Time Counter and Autonomous Periodic Interrupt	Yes	Yes	Yes
Periodic Interrupt Timer (PIT)	4 ch, 32-bit		
Software Watchdog Timer (SWT)	Yes		
System Timer Module (STM)	4 ch, 32-bit		
Timed I/O[2]	8 ch, 16-bit IC/OC		
	16 ch, 16-bit OPWM/IC/OC[3]		
ADC[4]	16 channels, 10-bit		
CAN (64 mailboxes)	1 × FlexCAN	2 × FlexCAN	2 × FlexCAN
CAN sampler	Yes		
SCI	2 × LINFlex		
SPI	2 × DSPI	2 × DSPI	3[5] × DSPI
QuadSPI serial flash interface	No	No	Yes
I^2C	2	2	4
GPIO	105	105	105 (144-pin package) 133 (176-pin package)
Debug	Nexus 1	Nexus 1	Nexus 2+[6]
Package	144 LQFP	144 LQFP	144 LQFP[7] 176 LQFP 208 MAPBGA[8]

1 Configuration is software-programmable.
2 IC-Input Capture, OC-Output Compare, OPWM-Output Pulse Width Modulation.
3 This functionality is split over two eMIOS blocks.
4 Support for external multiplexer enabling up to 23 channels.
5 QuadSPI serial Flash controller can be optionally used as a third DSPI.
6 Nexus2+ available on 176 LQFP as alternate pin function and on 208 MAPBGA.
7 Not all features are available simultaneously in 144 LQFP package option.
8 The 208-pin package is not a production package; it is available in limited quantities for tool development only.

1.4 MPC5606S series blocks

1.4.1 Block diagram

Figure 1 shows a high-level block diagram of the MPC5606S series.

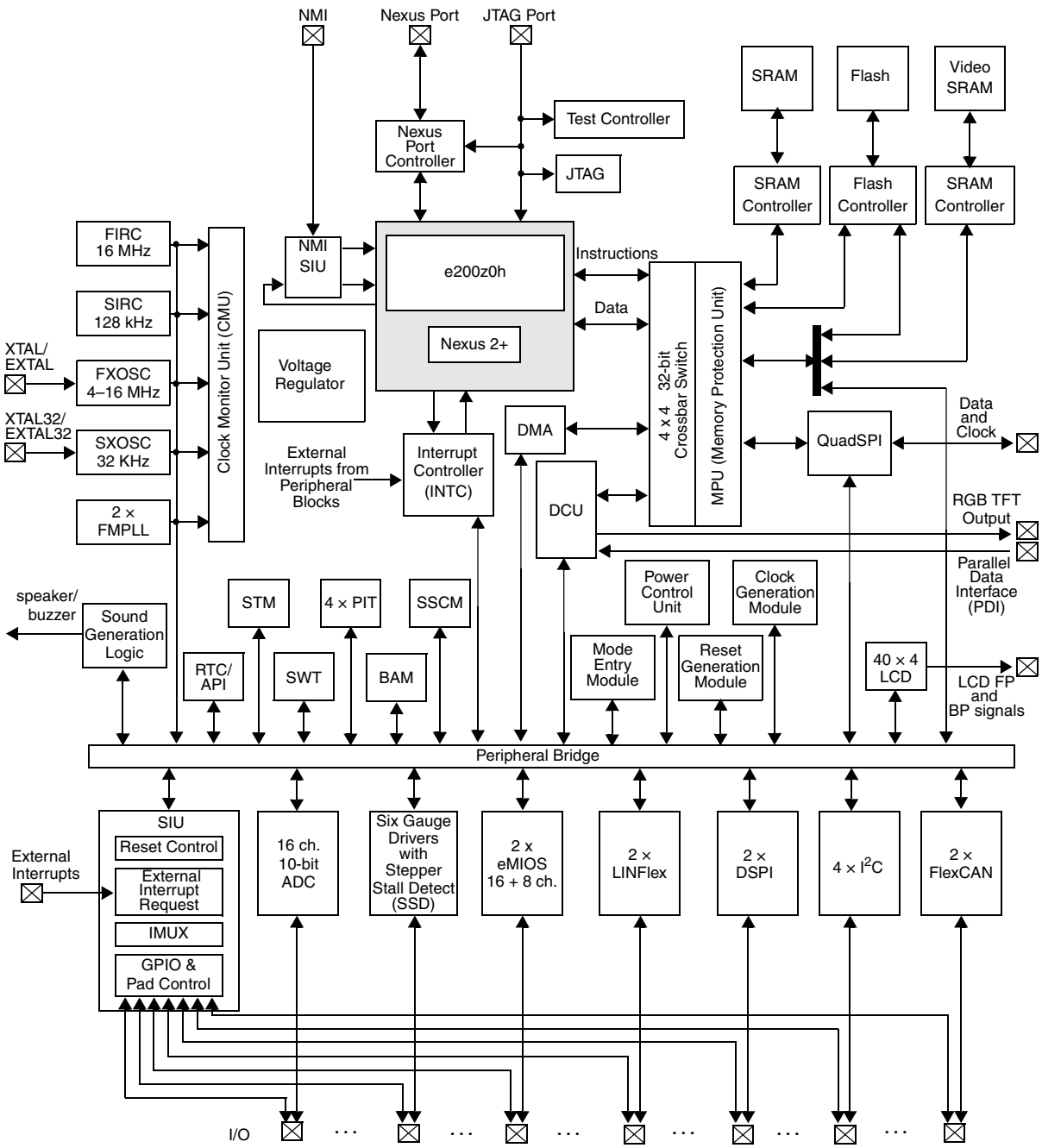


Figure 1. MPC5606S series block diagram

1.5 Details

1.5.1 Low-power operation

MPC5606S devices are designed for optimized low-power operation and dynamic power management of the core processor and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are two static low-power modes, Standby and Stop, and six dynamic power modes—five Run modes and Halt. Both low-power modes use clock gating to halt the clock for all or part of the device. Standby mode also uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

Standby mode turns off the power to the majority of the chip to offer the lowest power consumption mode. The contents of the cores, on-chip peripheral registers, and potentially some of the volatile memory are lost. Standby mode is configurable to make certain features available, with the disadvantage that these consume additional current:

- It is possible to retain the contents of the full RAM or only 8 KB.
- It is possible to enable the internal 16 MHz or 128 kHz RC oscillator, the external 4–16 MHz oscillator, or the external 32 KHz oscillator.
- It is possible to keep the LCD module active.

The device can be awakened from Standby mode from any of as many as 19 I/O pins, from a reset, or from a periodic wakeup using a low-power oscillator.

Stop mode maintains power to the entire device, thus allowing the retention of all on-chip registers and memory, and providing a faster recovery low-power mode than the lowest Standby mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower startup time.

Stop mode is entered from Run mode only. Wakeup from Stop mode is triggered by an external event or by the internal periodic wakeup, if enabled.

Run modes are the primary operating modes where the entire device can be powered and clocked. In Run modes most processing activity is done. One default (Drun) and four dynamic Run modes are supported—Run0...3. The ability to configure and select different Run modes enables different clocks and power configurations to be supported with respect to each other, and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed, and system clock prescalers can be independently configured for each of the four Run modes of the device.

Halt mode is a reduced activity, low-power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wakeup latency. The system returns to a Run mode as soon as an event or interrupt is pending.

Table 2 summarizes the operating modes of MPC5606S devices.

Table 2. Operating mode summary[1]

	Operating modes:	Run	Halt	Stop	Standby		POR
SoC features	Core	On	CG	CG	Off	Off	—
	Peripherals	OP	OP	CG	Off[2]	Off	—
	Flash memory	OP	OP	CG	Off	Off	—
	SRAM	On	On	CG	CG[3]	8 KB[4]	—
	Graphics RAM	On	On	CG	Off	Off	—
Clock sources	Main PLL	OP	OP	CG	Off	Off	—
	Auxiliary PLL	OP	OP	CG	Off	Off	—
	16 MHz IRC	On	On	OP	OP	OP	—
	FXOSC	OP	OP	OP	OP	OP	—
	128 kHz IRC	On	On	On	On	On	—
	32 KHz XOSC	OP	OP	OP	OP	OP	—
Periodic wakeup		—	OP	OP	OP	OP	—
Wakeup input		—	OP	OP	OP	OP	—
VREG mode		FP	FP	LP	LP	LP	—
Wakeup times[5]	VREG startup	—	—	50 µs	250 µs	250 µs	250 µs[6]
	IRC wakeup	—	—	4 µs	4 µs	8 µs	8 µs
	Flash memory recovery	—	—	20 µs	100 µs	100 µs	100 µs
	OSC stabilization	—	—	1 ms	1 ms	1 ms	1 ms
	PLL lock	—	—	200 µs	200 µs	200 µs	200 µs
	S/W reconfig	—	—	—	Var	Var	—
	Mode switch over	—	200.69 µs	24 µs	28 µs	28 µs	BAM

1 Table Key:
On—Powered and clocked
OP—Optionally configurable to be enabled or disabled (clock gated)
CG—Clock Gated, Powered but clock stopped
Off—Powered off and clock gated
FP—VREG Full Performance mode
LP—VREG low-power mode, reduced output capability of VREG but lower power consumption
Var—Variable duration, based on the required reconfiguration and execution clock speed
BAM—Boot Assist Module Software and Hardware used for device startup and configuration

2 The LCD can optionally be kept running while the device is in Standby mode.

3 All of the RAM content is retained, but not accessible in Standby mode.

4 8 KB of the RAM content is retained, but not accessible in Standby mode.

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

1.5.6 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software-configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

Multiple processors can assert interrupt requests to each other through software-settable interrupt requests. These same software-settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high-priority portion and a low-priority portion. The high-priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software-settable interrupt request to finish the servicing in a lower priority ISR. Therefore these software-settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External NMI directly accessing the main core critical interrupt mechanism
- 32 external interrupts

1.5.7 QuadSPI serial flash controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Memory mapping of external serial flash memory
- Automatic serial flash read command generation by CPU, DMA, or DCU read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Flexible buffering scheme to maximize read bandwidth of serial flash

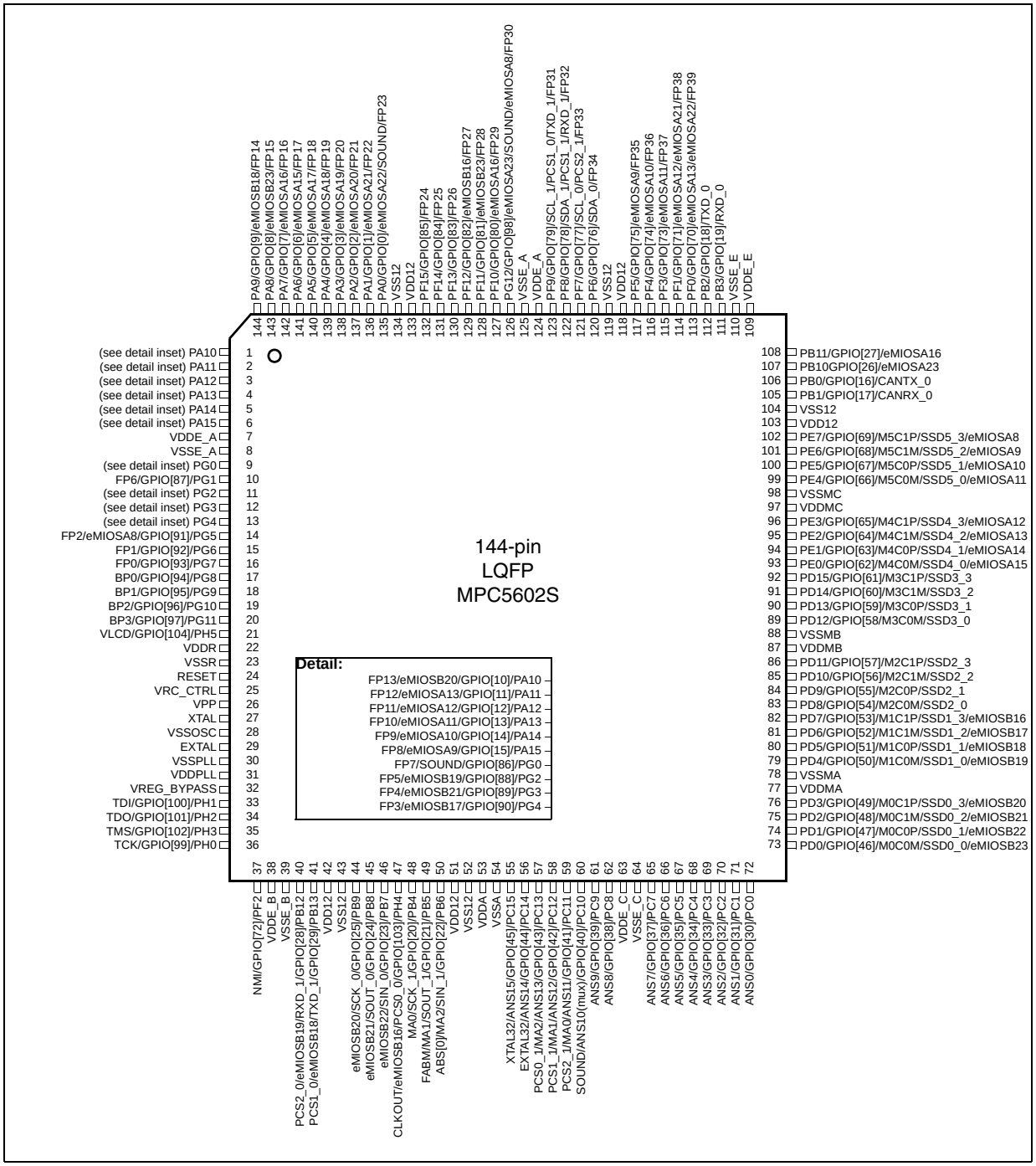


Figure 4. 144-pin LQFPpinout for MPC5602S

2.2 176 LQFP package pinout

Figure 5 shows the pinout for the 176-pin LQFP package.

CAUTION

Any pins labeled “NC” must not be connected to any external circuit.

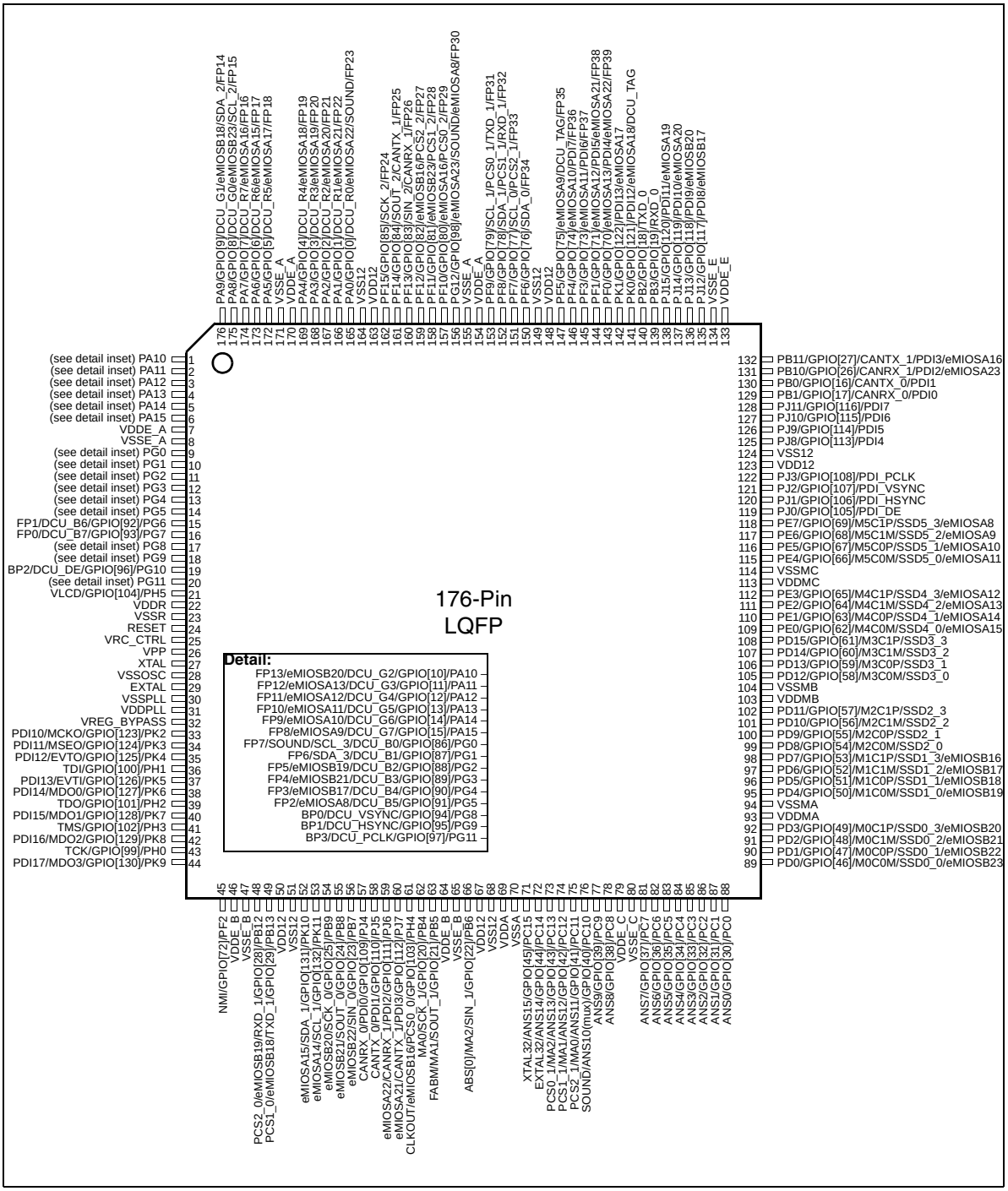


Figure 5. 176-pin LQFP Pinout

3.4.1 Recommended operating conditions

NOTE

Maximum slew time for the supplies to ramp up should be 1 second, which is the slowest ramp-up time.

CAUTION

V_{DDE_C} and V_{DDA} must be the same voltage.

V_{DDMB} and V_{DDMC} must be the same voltage.

Table 15. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{DDA}[1]	SR	C	Voltage on VDDA pin (ADC reference) with respect to ground (V_{SS})	—	3.0	3.6	V
		C		Relative to V_{DDE_C}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SSA}	SR	C	Voltage on VSSA (ADC reference) pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{SSPLL}	SR	C	Voltage on VSSPLL pin with respect to V_{SS12}	—	0	0	V
V_{DDR}[2]	SR	C	Voltage on VDDR pin (regulator supply) with respect to ground (V_{SSR})	—	3.0	3.6	V
V_{SSR}	SR	C	Voltage on VSSR (regulator ground) pin with respect to V_{SS12}	—	0	0	V
V_{SS12}[4]	CC	C	Voltage on VSS12 pin with respect to V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD}[3,4,5]	SR	C	Voltage on VDD pins (VDDE_A, VDDE_B, VDDE_C, VDDE_E, VDDMA, VDDMB, VDDMC) with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS}[6]	SR	C	I/O supply ground	—	0	0	V
V_{DDE_A}	SR	C	Voltage on VDDE_A (I/O supply) pin with respect to ground (V_{SSE_A})	—	3.0	3.6	V
V_{DDE_B}	SR	C	Voltage on VDDE_B (I/O supply) pin with respect to ground (V_{SSE_B})	—	3.0	3.6	V
V_{DDE_C}	SR	C	Voltage on VDDE_C (I/O supply) pin with respect to ground (V_{SSE_C})	—	3.0	3.6	V
V_{DDE_E}	SR	C	Voltage on VDDE_E (I/O supply) pin with respect to ground (V_{SSE_E})	—	3.0	3.6	V
V_{DDMA}	SR	C	Voltage on VDDMA (stepper motor supply) pin with respect to ground (V_{SSMA})	—	3.0	3.6	V
V_{DDMB}	SR	C	Voltage on VDDMB (stepper motor supply) pin with respect to ground (V_{SSMB})	—	3.0	3.6	V
V_{DDMC}	SR	C	Voltage on VDDMC (stepper motor supply) pin with respect to ground (V_{SSMC})	—	3.0	3.6	V
V_{SSOSC}	SR	C	Voltage on VSSOSC (oscillator ground) pin with respect to V_{SS}	—	0	0	V

3.7.4 Recommended power-up and power-down order

Figure 10 shows the recommended order for powering up the power supplies on this device.

The 1.2 V regulator output starts after the device's internal POR (VDDREG HV) is deasserted at approximately 2.7 V on VDDREG.

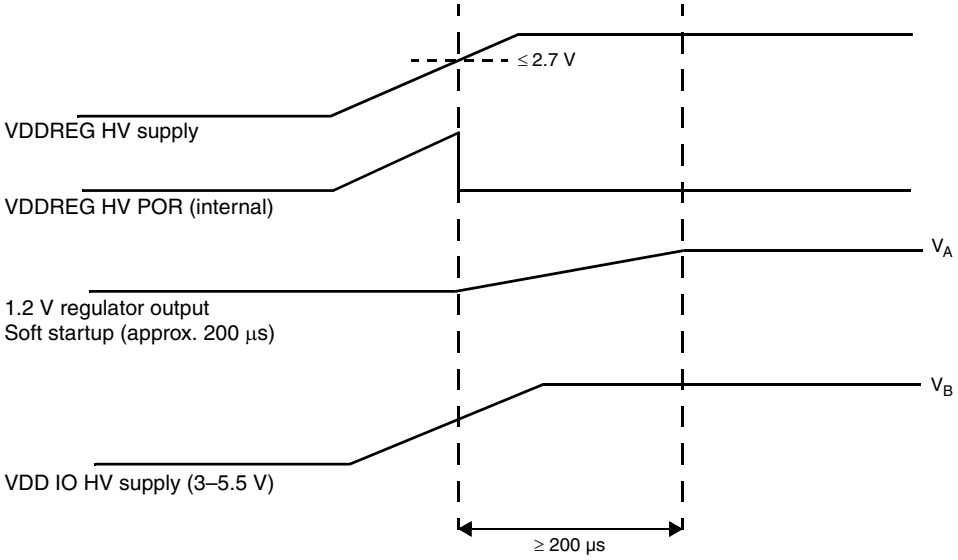


Figure 10. Recommended order for powering up the power supplies

CAUTION

The voltages V_A and V_B in Figure 10 must always obey the relation $V_B \geq V_A - 0.7$ V. Otherwise, currents from the 1.2 V supply to the 3.3 V supply may result.

Figure 11 shows the recommended order for powering down the power supplies on this device.

It is acceptable for the VDD IO HV supply to ramp down faster than the 1.2 V regulator output, even if the latter takes time to discharge the high 40 µF capacitance. (The capacitor will ultimately discharge.)

Table 33. MEDIUM configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
T_{tr}	CC	T	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	10	ns
		T		C_L = 50 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	20	
		T		C_L = 100 pF, V_{DD} = 5.0 V ±10%, PAD3V5V = 0	—	—	40	
		T		C_L = 25 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	12	
		T		C_L = 50 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	25	
		T		C_L = 100 pF, V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	40	
ΔI_{tr50}	CC	D	Current slew at C_L = 50 pF MEDIUM configuration	recommended configuration at V_{DD} = 5.0 V ±10%, PAD3V5V = 0 V_{DD} = 3.3 V ±10%, PAD3V5V = 1	—	—	7	mA/ns
		D		V_{DD} = 5.0 V ±10%, PAD3V5V = 1	—	—	16	

1 V_{DD} = 3.3 V ±10% / 5.0 V ±10%, T_A = –40 to 105 °C, unless otherwise specified

2 This is a transient configuration during power-up. All pads but $\overline{\text{RESET}}$ and NEXUS output (MDOx, EVTO, MCK) are configured in input or in high impedance state.

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

Table 34. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull, I_{OH} = –14 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		D		Push Pull, I_{OH} = –7 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C		Push Pull, I_{OH} = –11 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull, I_{OL} = 14 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		D		Push Pull, I_{OL} = 7 mA, V_{DD} = 5.0 V ±10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 11 mA, V_{DD} = 3.3 V ±10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 52. Pad AC specifications (5.0 V, PAD3V5V = 0)[1] (continued)

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	1	—	15	3	—	10	—	—	40	2.5	—	7	25
		1	—	15	5	—	20	—	—	20	2.5	—	7	50
		1	—	15	9	—	40	—	—	13	2.5	—	8	100
		1	—	15	12	—	70	—	—	7	2.5	—	8	200
3	Fast	1	—	6	1	—	4	—	—	100	18	—	55	25
		1	—	6	1.5	—	6	—	—	80	18	—	55	50
		1	—	6	3	—	12	—	—	40	18	—	55	100
		1	—	6	5	—	16	—	—	25	18	—	55	200
4	Pull Up/Down (5.5 V max)	—	—	—	—	—	5000	—	—	—	—	—	—	50
Parameter Classification		D			C			C			C			n/a

1 Propagation delay from $V_{DD}/2$ of internal signal to Pchannel/Nchannel on condition

2 Slope at rising/falling edge

Table 53. Pad AC specifications (3.3 V, PAD3V5V = 1)[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200

3.20.4 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) timing

Table 59. IRQ and NMI timing

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	t_{IPWL}	CC	T	IRQ/NMI Pulse Width Low	200	—	ns
2	t_{IPWH}	CC	T	IRQ/NMI Pulse Width High	200	—	ns
3	t_{ICYC}	CC	T	IRQ/NMI Edge to Edge Time[1]	400	—	ns

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

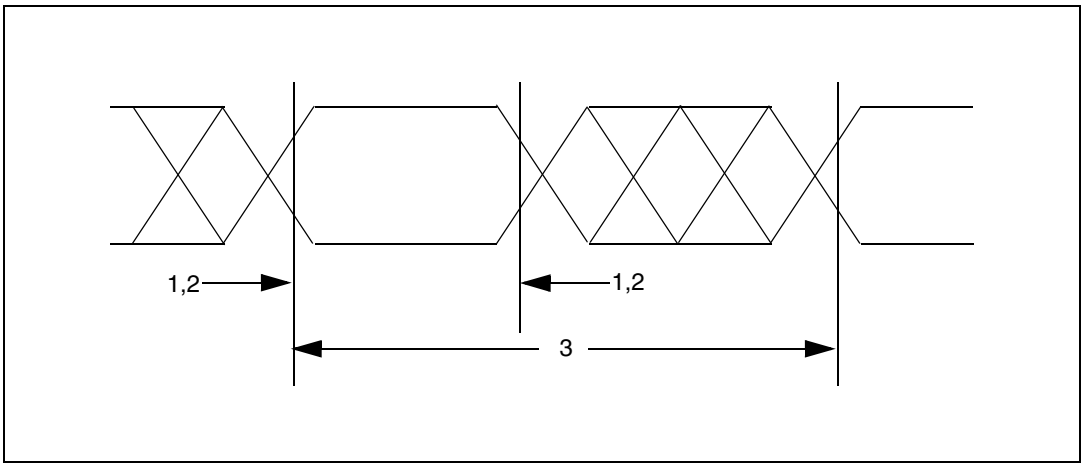


Figure 37. IRQ and NMI timing

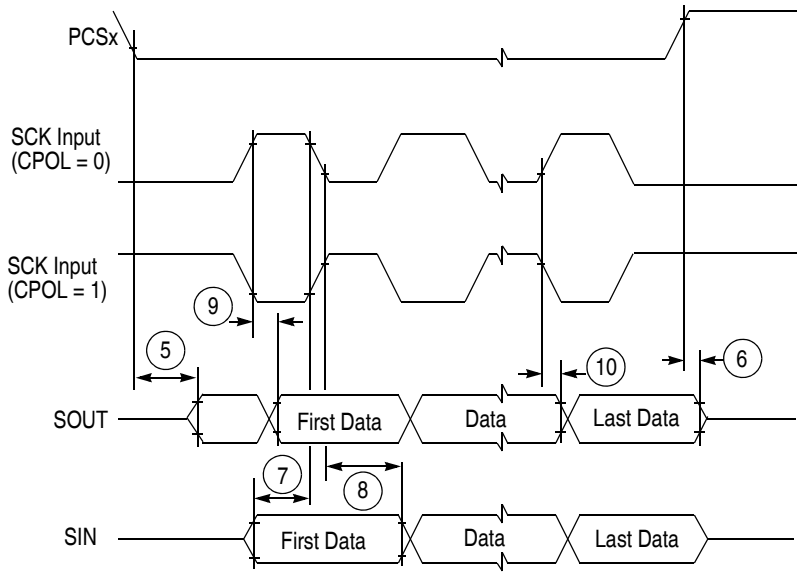
3.20.5 eMIOS timing

Table 60. eMIOS timing[1]

No.	Symbol		C	Parameter	Value		Unit
					Min[2]	Max	
1	t_{MIPW}	CC	D	eMIOS input pulse width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS output pulse width	1	—	t_{CYC}

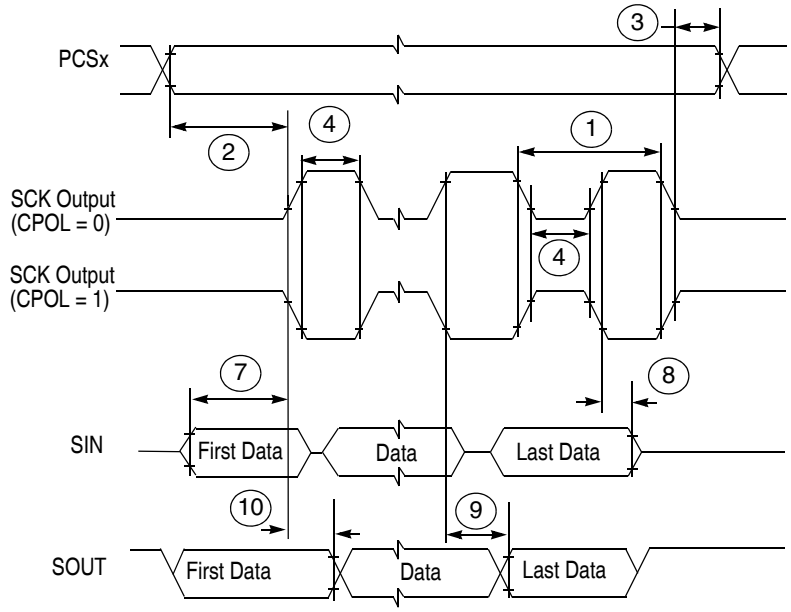
[1] eMIOS timing specified at f_{SYS} = 64 MHz, V_{DD12} = 1.14 V to 1.32 V, VDDE_x = 3.0 V to 5.5 V, T_A = –40 to 105 °C, and C_L = 50 pF with SRC = 0b00.

[2] There is no limitation on the peripheral for setting the minimum pulse width, the actual width is restricted by the pad delays. Refer to the pad specification section for the details.



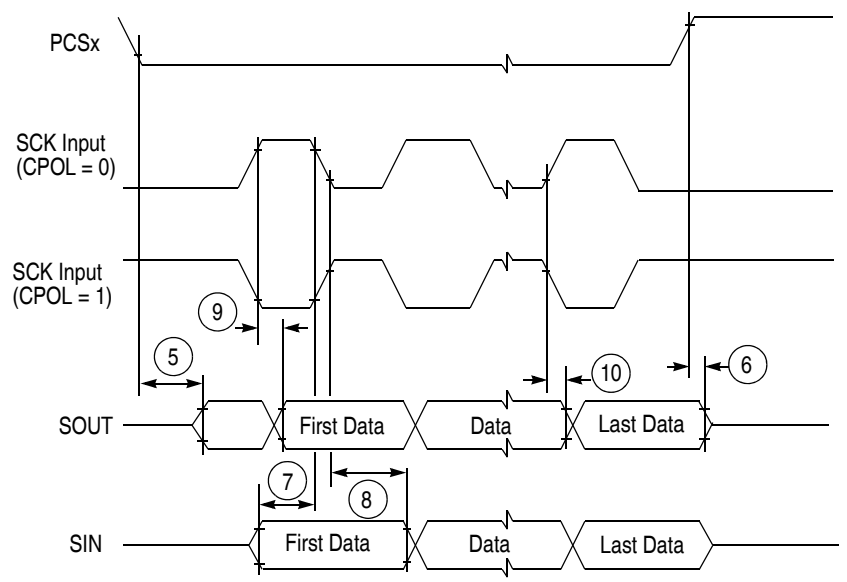
Note: Numbers in circles refer to values in Table 62.

Figure 41. DSPI classic SPI timing — slave, CPHA = 1



Note: Numbers in circles refer to values in Table 62.

Figure 42. DSPI modified transfer format timing — master, CPHA = 0



Note: Numbers in circles refer to values in Table 62.

Figure 45. DSPI modified transfer format timing — slave, CPHA = 1

3.20.8 I²C timing

Table 63. I²C Input Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	IP-Bus Cycle[1]
2	—	CC	D	Clock low time	8	—	IP-Bus Cycle[1]
4	—	CC	D	Data hold time	0.0	—	ns
6	—	CC	D	Clock high time	4	—	IP-Bus Cycle[1]
7	—	CC	D	Data setup time	0.0	—	ns
8	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]
9	—	CC	D	Stop condition setup time	2	—	IP-Bus Cycle[1]

[1] Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

Table 64. I²C Output Timing Specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1[1]	—	CC	D	Start condition hold time	6	—	IP-Bus Cycle[2]
2[1]	—	CC	D	Clock low time	10	—	IP-Bus Cycle[1]
3[3]	—	CC	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	CC	D	Data hold time	7	—	IP-Bus Cycle[1]
5[1]	—	CC	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	CC	D	Clock high time	10	—	IP-Bus Cycle[1]
7[1]	—	CC	D	Data setup time	2	—	IP-Bus Cycle[1]
8[1]	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[1]
9[1]	—	CC	D	Stop condition setup time	10	—	IP-Bus Cycle[1]

[1] Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

[2] Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

[3] Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

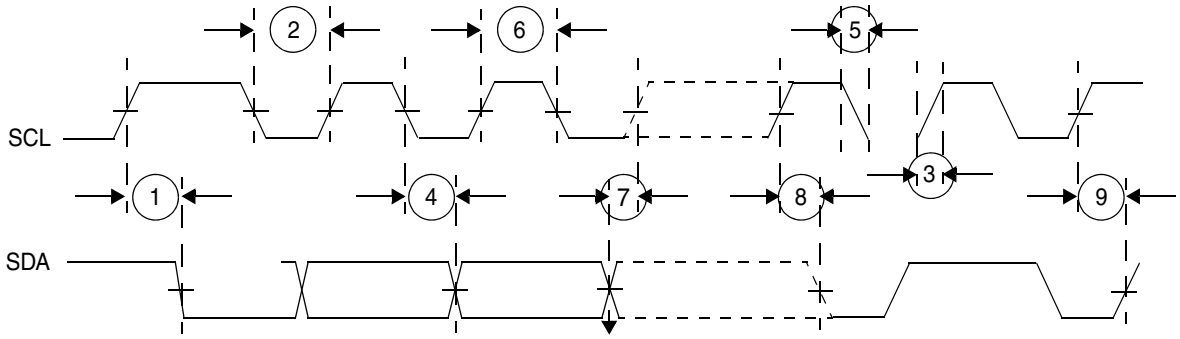


Figure 46. I²C input/output timing

3.20.9 QuadSPI timing

The following notes apply to Table 65:

- All data are based on a negative edge data launch from MPC5606S and a positive edge data capture as shown in the timing diagrams.
- Typical values are provided from center-split material at 25 °C and 3.3 V. Minimum and maximum values are from a temperature variation of –45 °C to 105 °C and the following supply conditions:
  - I/O voltage: 3.2 V, core supply: 1.2 V
  - I/O voltage: 3.6 V, core supply: 1.2 V
- All measurements are taken at 70% of VDDE levels for clock pin and 50% of VDDE level for data pins.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

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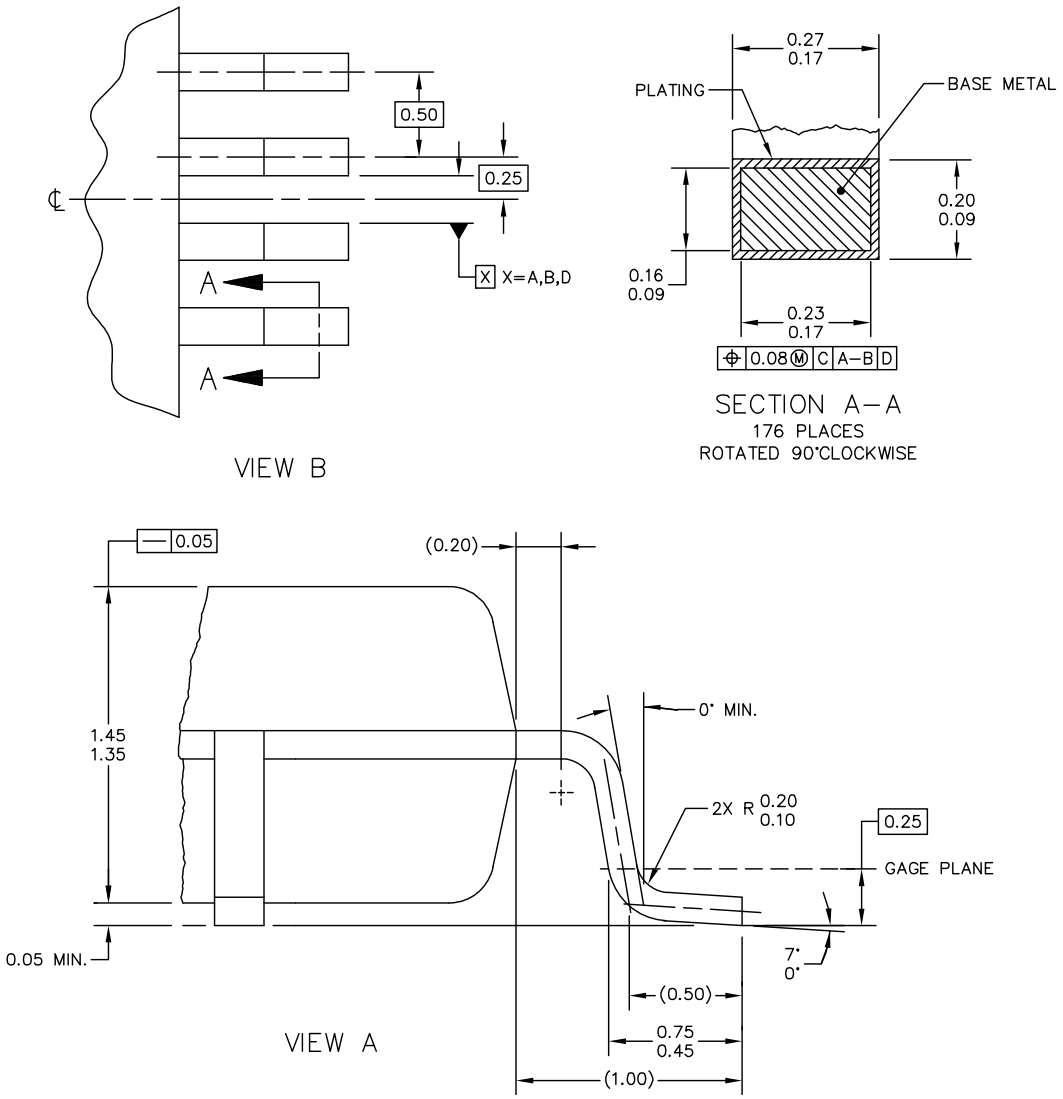
TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 52. LQFP144 mechanical drawing (Part 3 of 3)



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 176 LD TQFP, 24 X 24 PKG, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23479W	REV: B
	CASE NUMBER: 1101–01	02 JUN 2005
	STANDARD: JEDEC MS–026 BGA	

Figure 54. LQFP176 mechanical drawing (Part 2 of 3)

Table 66. Document revision history

Revision	Date	Substantive changes
2 (continued)	18 Aug 2009 (continued)	Table 37: – I_{RMSMED}: Replaced SLOW with MEDIUM in parameter column – I_{RMSFST}: Replaced SLOW with FAST in parameter column Section 3.8.4, “I/O pad current specification: Replaced ipp_hve with PAD3V5V Section 3.10, “RESET electrical characteristics: Replaced ipp_hve with PAD3V5V Updated Figure 15 Updated Figure 18 Updated Figure 20 Section 3.19, “Pad AC specifications: Replaced IPP_HVE with PAD3V5V Table 45: Added rows $I_{FIRCSTOP}$ and t_{FIRCSU} Table 46: – Added rows t_{SIRCSU} and $\Delta_{SIRCTRIM}$ – Updated conditions for $\Delta_{SIRCVAR}$ Added Table 42 “ADC input leakage current” Table 50: Updated TUEp and TUEx
		Table 7: Modified PC[0] to PC[9]: – I/O direction: was I, is I/O – pad type: was I, is S Table 50: Updated values for ‘Input current injection’ Section 3.20.3, “Interface to TFT LCD panels: Modified description of event No. 1 in sequence for active matrix interface timing Table 57: Removed value for Display pixel clock period Table 53: Removed duplicated row for part number MPC5604SEMLQ Section 2.4.2, “Voltage Supply Pins”: Added preferred power up sequence. Section 2.9, “Port pin summary”: Changed reset configuration on ADC pins. Section 3, “Electrical characteristics: Made updates to data. All data is still considered preliminary. Section 3.7.1, “Voltage regulator electrical characteristics”: Added lower power voltage regulator and ultra-low power voltage regulator characteristics.
3	—	Not released; no substantive changes between Rev. 2 and Rev. 3.
4	—	Not released; no substantive changes between Rev. 3 and Rev. 4.

Table 66. Document revision history

Revision	Date	Substantive changes
5 (continued)	1 Sep 2010 (continued)	Added a footnote to the “Pad type description” table. In the “Pad type description” table: • Revised the entry for SMD. • Revised the description for the J and M2 pad types. Revised the entry for VSSPLL in the “Absolute maximum ratings” and “Recommended operating conditions” table. Changed the max value for V_{DDPLL} (was 1.32 V, is 1.4 V) in several tables. Added the “Connecting power supply pins: What to do and what not to do” section. In the “Recommended operating conditions” table, changed the note to state “Maximum slew...” instead of “Minimum slew...”. In footnote 2 of the “Recommended operating conditions” table, changed “200 µF capacitance must be connected between V_{DDR} and V_{SS12}” to “10 µF capacitance must be connected between V_{DDR} and V_{SS12}.”. In the “Recommended operating conditions” section, added a caution on which voltages must be the same. In the “Recommended operating conditions (3.3 V)” table: • Revised the footnote affecting V_{DD12}/V_{SS12} supply capacitances. • Deleted footnote 9. • Deleted the entries for V_{DDPLL} and V_{DD12}. In the “Recommended operating conditions (5.0 V)” table: • Changed the footnote text “200 µF capacitance must be connected between V_{DDR} and V_{SS12}” to “10 µF capacitance must be connected between V_{DDR} and V_{SS12}” and revised the footnote affecting V_{DD12}/V_{SS12} supply capacitances. • Added a specification for TV_{DD}. • Deleted the entries for V_{DDPLL} and V_{DD12}. Revised the “EMC requirements on board” section. Added meaningful values to the “EMI testing specifications” table. In the “ESD absolute maximum ratings” table, added a specification for $V_{ESD(MM)}$. Deleted the empty “DC Electrical Characteristics” section. In the “I/O pad types” section, added an entry for SMD pads. Added SMC pad electrical characteristics. Revised the “Voltage regulator electrical characteristics” section. Revised the “Low-power voltage regulator electrical characteristics” table. Revised the “Ultra-low power voltage regulator electrical characteristics” table. Revised the “Low voltage monitor electrical characteristics” table. Added the “Recommended power-up and power-down order” section. Added the “Power-up inrush current profile” section. Added the “HPREG load regulation characteristics” section. Revised the “DC electrical characteristics” table. Replaced all values for “STANDBY mode current”. Revised the “I/O pad types” section. In the “I/O input DC electrical characteristics” table: • Changed the specifications for ILKG (was min = <1 µA, is min = –1 µA; was max = —, is max = 1 µA). • Added an entry for R_{ON}. Revised the “I/O output DC characteristics” section. Revised the “MEDIUM configuration output buffer electrical characteristics” table. Revised the “SMD pad electrical characteristics” table and changed its name (is “SMC pad...”). In the “SMC pad electrical characteristics” table, changed R_{DSOH} to R_{DSONH} and R_{DSOL} to R_{DSONL}. Moved the I_{MAX} specification from the “SMC pad electrical characteristics” table to the “Absolute maximum ratings” table.

Table 66. Document revision history

Revision	Date	Substantive changes
6	14 Jan 2011	Editorial changes and improvements. Swapped XTAL and EXTAL pins for the 208-pin BGA package and throughout. In the “Pinout and signal descriptions” section, changed WARNING labels to CAUTION labels. Updated the “Absolute maximum ratings” and “Recommended operating conditions” tables. Added footnote reference to V_{ss12} in “Recommended operating conditions (3.3 V)” table. Updated the “Connecting power supply pins” section. Removed footnote regarding characterization in the “Thermal characteristics” table. Updated the V_{DD12}/V_{DDPLL} operating voltages in the “Electromagnetic interference” table. Added typical values and updated the “Voltage regulator electrical characteristics,” “Low-power voltage regulator electrical characteristics,” and “Ultra-low-power voltage regulator electrical characteristics” tables. Updated classifications and values in the “Low voltage monitor electrical characteristics” table. Made major modifications and updates to the “DC electrical characteristics” table. Made major modifications and updates to the “I/O input DC electrical characteristics” table. Made major modifications and updates to the “I/O pull-up/pull-down DC electrical characteristics” table. Changed “SMC” pads to “SMD” pads throughout. Made updates to the “SMD pad electrical characteristics” table. Added run current during RESET to the “Reset electrical characteristics” table. Updated the FMPLL jitter (peak to peak) specification in the “FMPLL electrical characteristics” table. Updated f_{FIRC} and t_{FIRCSU} in the “Fast internal RC oscillator (16 MHz) electrical characteristics” table. Updated f_{SIRC} and t_{SIRCSU} in the “Slow internal RC oscillator (128 kHz) electrical characteristics” table. Removed “symmetric” pad type from the “Pad AC specifications (5.0 V, PAD3V5V = 0)” table. Removed “symmetric” pad type from the “Pad AC specifications (3.3 V, PAD3V5V = 1)” table. Updated V_{DD12} post-trimming minimum value in the “Low-power voltage regulator electrical characteristics” table. Updated V_{DD12} post-trimming minimum value in the “Ultra-low-power voltage regulator electrical characteristics” table. Updated $V_{LVDLVCORH}$ maximum value in the “Low voltage monitor electrical characteristics” table. Updated $V_{LVDLVCORL}$ minimum value in the “Low voltage monitor electrical characteristics” table. Updated value of V_{DD12}/V_{DDPLL} operating voltages in the “Input DC electrical characteristics” table. Corrected erroneous value of I_{LKG} (105°C case) in the “Input DC electrical characteristics” table.