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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	40kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2186bstz-160

TECHNICAL SUPPORT

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Fabricated in a high speed, double metal, low power, CMOS process, the ADSP-2186 operates with a 25 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2186's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2186 can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:
- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

Development System
The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2186. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-2186 assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The EZ-KIT Lite is a hardware/software kit offering a complete development environment for the ADSP-218x family: an ADSP-218x-based evaluation board with PC monitor software plus Assembler, Linker, Simulator and PROM Splitter software. The ADSP-218x EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demo Programs
- Evaluation Suite of Visual DSP

The ADSP-218x EZ-ICE Emulator aids in the hardware debugging of an ADSP-2186 system. The emulator consists of hardware, host computer resident software, and the target board connector. The ADSP-2186 integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2186 device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See Designing An EZ-ICE-Compatible Target System in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections), as well as the Target Board Connector for EZ-ICE Probe section of this data sheet, for the exact specifications of the EZ-ICE target board connector.

Additional Information
This data sheet provides a general overview of ADSP-2186 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-218x DSP Hardware Reference*. For more information about the development tools, refer to the *ADSP-2100 Family Development Tools Data Sheet*.

ARCHITECTURE OVERVIEW

The ADSP-2186 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2186 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

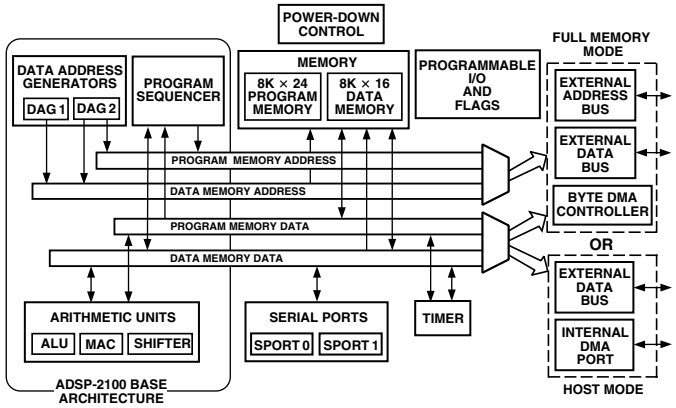


Figure 1. Block Diagram

Figure 1 is an overall block diagram of the ADSP-2186. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2186 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from data memory and program memory. Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2186 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2186 can fetch an operand from program memory and the next instruction in the same cycle.

When configured in host mode, the ADSP-2186 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2186 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2186 can respond to eleven interrupts. There are up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2186 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every *n* processor cycle, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2186 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2186 SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

PIN DESCRIPTIONS

The ADSP-2186 is available in a 100-lead LQFP package and a 144-Ball Mini-BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during RESET only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases

where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Common-Mode Pins

Pin Name(s)	# of Pins	Input/ Output	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$/	1	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O Pin
$\overline{\text{IRQL0}}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{\text{IRQL1}}$/	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{\text{IRQE}}$/	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
PF3	1	I/O	Programmable I/O Pin
Mode C/	1	I	Mode Select Input—Checked only During $\overline{\text{RESET}}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B/	1	I	Mode Select Input—Checked only During $\overline{\text{RESET}}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A/	1	I	Mode Select Input—Checked only During $\overline{\text{RESET}}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{\text{IRQ1:0}}$ FI, FO			Edge- or Level-Sensitive Interrupts, Flag In, Flag Out[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DD}	6	I	Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DD}	11	I	Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

NOTES
[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2186 processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

Full Memory Mode Pins (Mode C = 0)

Pin Name	# of Pins	Input/ Output	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte and I/O Spaces (8 MSBs Are Also Used as Byte Memory Addresses)

Host Mode Pins (Mode C = 1)

Pin Name	# of Pins	Input/ Output	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access
D23:8	16	I/O	Data I/O Pins for Program, Data Byte and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge

In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Terminating Unused Pin

The following table shows the recommendations for terminating unused pins.

Pin Terminations

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
IAD12:0	I/O (Z)	Hi-Z	$\overline{\text{IS}}$	Float
A0	O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{IWR}}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{IRD}}$	I	I	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)

Pin Terminations (Continued)

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/PF7	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/PF6	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/PF5	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/PF4	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	O		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	O		High or Low
DT1/FO	O	O		Float
EE	I	I		
$\overline{EBR}$	I	I		
$\overline{EBG}$	O	O		
$\overline{ERESET}$	I	I		
$\overline{EMS}$	O	O		
$\overline{EINT}$	I	I		
ECLK	I	I		
ELIN	I	I		
ELOUT	O	O		

NOTES
*Hi-Z = High Impedance.
1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options:
   Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive).
   Option 2: Program the unused pins as OUTPUTS, set them to 1, and let them float.
3. All bidirectional pins have three-stated outputs. When the pins are configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, RESET, and PF3:0 are not included in the table because these pins must be used.

Setting Memory Mode

Memory Mode selection for the ADSP-2186 is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are passive and active.

Passive configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 100 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active configuration involves the use of a three-stateable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{RESET}$ signal such that it only drives the PF2 pin when $\overline{RESET}$ is active (low). After $\overline{RESET}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output.

To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and not oscillate should the three-state driver's level hover around the logic switching point.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2186 provides four dedicated external interrupt input pins, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$ and $\overline{IRQE}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI and FO, for a total of six external interrupts. The ADSP-2186 also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and $\overline{RESET}$). The $\overline{IRQ2}$, $\overline{IRQ0}$ and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and IRQE is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (Lowest Priority)

BIASED ROUNDING

A mode is available on the ADSP-2186 to allow biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding up odd MR1 values.

For example:

Table VII. Biased Rounding Example

MR Value Before RND	Biased RND Result	Unbiased RND Result
00-0000-8000	00-0001-8000	00-0000-8000
00-0001-8000	00-0002-8000	00-0002-8000
00-0000-8001	00-0001-8001	00-0001-8001
00-0001-8001	00-0002-8001	00-0002-8001
00-0000-7FFF	00-0000-7FFF	00-0000-7FFF
00-0001-7FFF	00-0001-7FFF	00-0001-7FFF

This mode only has an effect when the MR0 register contains 0x8000; all other rounding operations work normally. This mode allows more efficient implementation of bit-specified algorithms that use biased rounding, for example the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

INSTRUCTION SET DESCRIPTION

The ADSP-2186 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2186's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

I/O Space Instructions

The instructions used to access the ADSP-2186's I/O memory space are as follows:

Syntax: IO(*addr*) = *dreg*
dreg = IO(*addr*);

where *addr* is an address value between 0 and 2047 and *dreg* is any of the 16 data registers.

Examples: IO(23) = AR0;
AR1 = IO(17);

Description: The I/O space read and write instructions move data between the data registers and the I/O memory space.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2186 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Emulation Reset and the Mode Pins

The Mode A, B, and C pins are located on the rising edge of the $\overline{\text{RESET}}$ signal. However, when the emulator reset ($\overline{\text{ERESET}}$) is asserted by the EZ-ICE, the DSP performs a chip reset, and the initial mode information is erased, and the logic values on the mode pins are latched. You must take into consideration the value of the mode pins before issuing a chip reset command from the EZ-ICE user interface. If you are using a passive method of maintaining mode information (as discussed in Setting Memory Modes) then it does not matter that the mode information is latched by an emulator reset. However, if you are using the $\overline{\text{RESET}}$ pin as a method of setting the value of the mode pins, then you have to take into consideration the effects of an emulator reset.

One method of ensuring that the values located on the mode pins is the one that is desired to construct a circuit like the one shown in Figure 9. This circuit will force the value located on the Mode C pin to zero; regardless if it latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

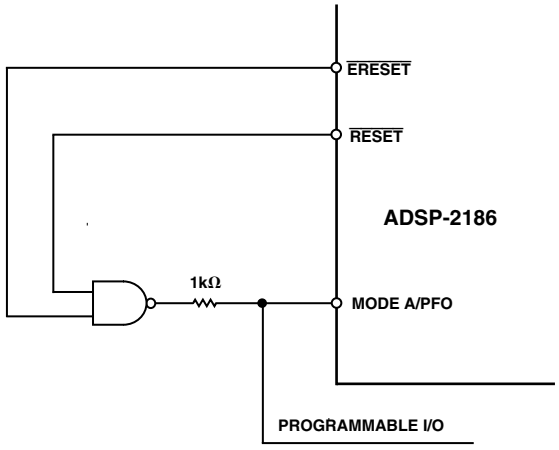


Figure 9. Boot Mode Circuit

See the *ADSP-2100 Family EZ-Tools* data sheet for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-2186 pins:

$\overline{\text{EBR}}$	$\overline{\text{EBG}}$	$\overline{\text{ERESET}}$
$\overline{\text{EMS}}$	$\overline{\text{EINT}}$	ECLK
ELIN	ELOUT	EE

These ADSP-2186 pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2186 and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE:

$\overline{BR}$	$\overline{BG}$
$\overline{RESET}$	GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2186 in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$ and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$ and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in Figure 10. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

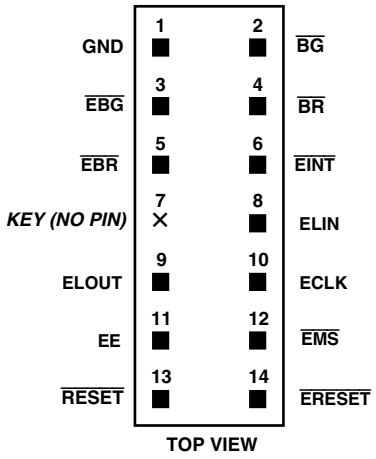


Figure 10. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15-inch clearance on all sides to accept the EZ-ICE probe plug. Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

Target Memory Interface

For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, and CM

Design a Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM) and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this DSP's data sheet. The performance of the EZ-ICE may approach published worst case specifications for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specifications for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristics and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2186 ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$ and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's DSP.

ADSP-2186–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	4.5	5.5	4.5	5.5	V
T_{AMB}	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min				
		I_{OH} = –100 µA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min				
		I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = V_{DD}max			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max				
		V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = V_{DD}max[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max				
		V_{IN} = 0 V[8], t_{CK} = 25 ns			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DD} = 5.0		14		mA
I_{DD}	Supply Current (Dynamic)[10, 11]	@ V_{DD} = 5.0				
		T_{AMB} = +25°C				
		t_{CK} = 34.7 ns		48		mA
		t_{CK} = 30 ns		55		mA
		t_{CK} = 25 ns		60		mA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 2.5 V,				
		f_{IN} = 1.0 MHz,				
		T_{AMB} = +25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12]	@ V_{IN} = 2.5 V,				
		f_{IN} = 1.0 MHz,				
		T_{AMB} = +25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2186 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$, CLKIN Inactive.

[9]Idle refers to ADSP-2186 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[11]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) LQFP . . . . . 280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2186 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-2186 timing parameters, for your convenience.

Memory Device Specification	ADSP-2186 Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2186 uses an input clock with a frequency equal to half the instruction rate; for example, a 20 MHz input clock (which is equivalent to 50 ns) yields a 25 ns processor cycle (equivalent to 40 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 7 ns = 0.5 (25 ns) – 7 ns = 5.5 ns

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN Period	50	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	0.5 t_{CK} – 7		ns
t_{CKH}	CLKOUT Width High	0.5 t_{CK} – 7		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low[1]	5 t_{CK}		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Setup after $\overline{\text{RESET}}$ High	5		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

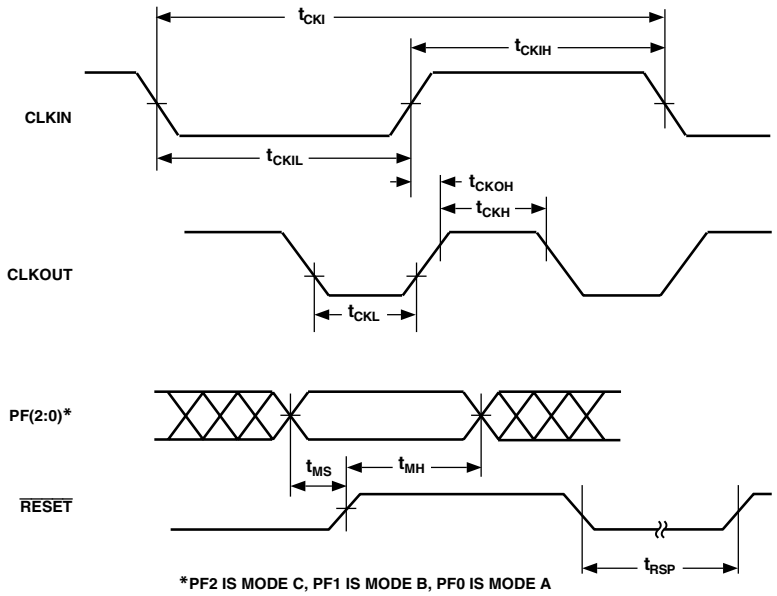


Figure 11. Clock Signals

TIMING PARAMETERS

Parameter		Min	Max	Unit
Interrupts and Flag				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	0.25 t_{CK} + 15		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	0.25 t_{CK}		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	0.25 t_{CK} – 7		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		0.5 t_{CK} + 5	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the *ADSP-218x DSP Hardware Reference*, for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, FL0, FL1, FL2, FO.

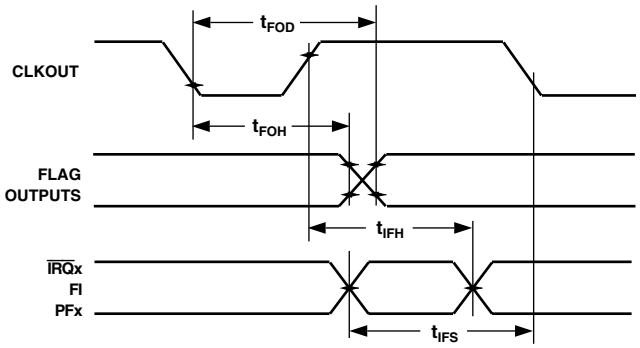


Figure 12. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	0.25 t_{CK} + 2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	0.25 t_{CK} + 17		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		0.25 t_{CK} + 10	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	0.25 t_{CK} – 7		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-218x DSP Hardware Reference*, for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

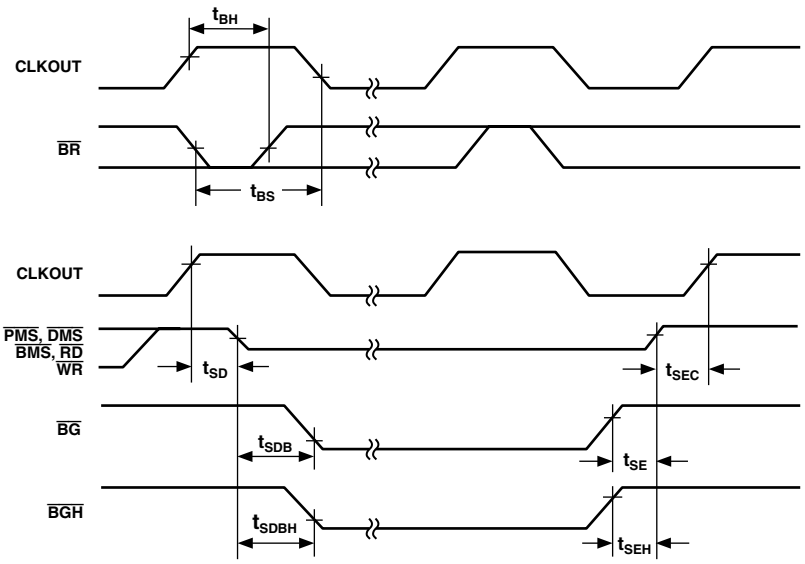


Figure 13. Bus Request–Bus Grant

TIMING PARAMETERS

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		0.5 t_{CK} – 9 + w	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		0.75 t_{CK} – 12.5 + w	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	1		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	0.5 t_{CK} – 5 + w		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	0.25 t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	0.25 t_{CK} – 6		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	0.25 t_{CK} – 3		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5 t_{CK} – 5		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

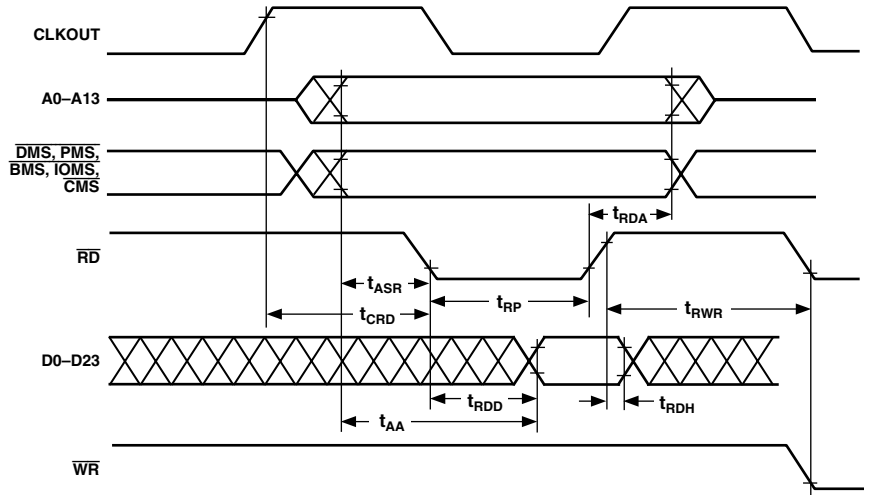


Figure 14. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	0.5 t_{CK} – 7+ w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	0.25 t_{CK} – 2		ns
t_{WP}	$\overline{WR}$ Pulsewidth	0.5 t_{CK} – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	0.25 t_{CK} – 6		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	0.25 t_{CK} – 7		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	0.25 t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	0.75 t_{CK} – 9 + w		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	0.25 t_{CK} – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5 t_{CK} – 5		ns

w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

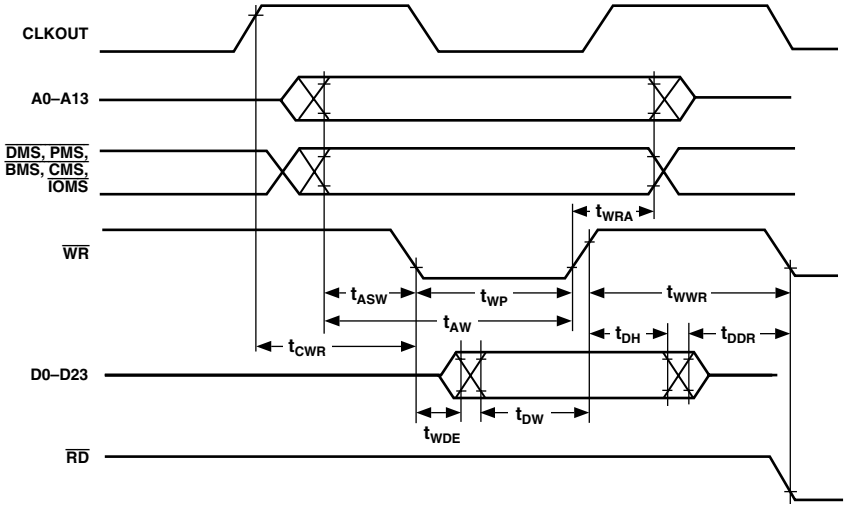


Figure 15. Memory Write

TIMING PARAMETERS

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	50		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	8		ns
t_{SCP}	$SCLK_{IN}$ Width	20		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	0.25 t_{CK}	0.25 t_{CK} + 10	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

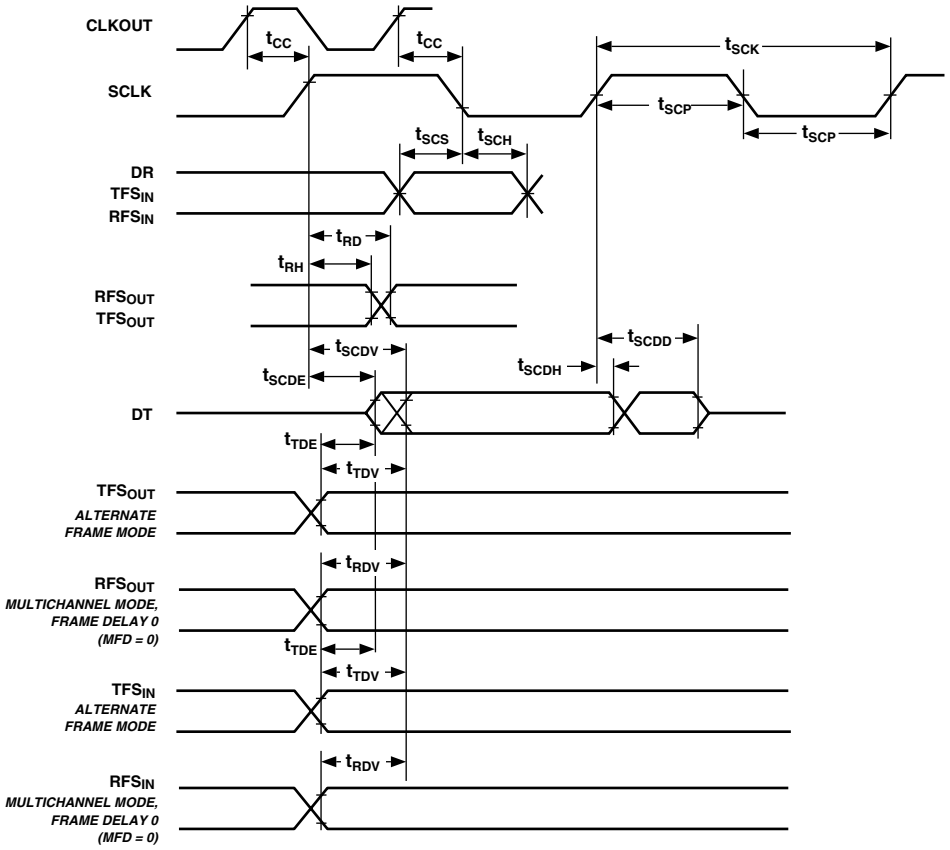


Figure 16. Serial Ports

TIMING PARAMETERS

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		15	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	0.5 t_{CK} – 10		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		15	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	2 t_{CK} – 5		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	t_{CK} – 5		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

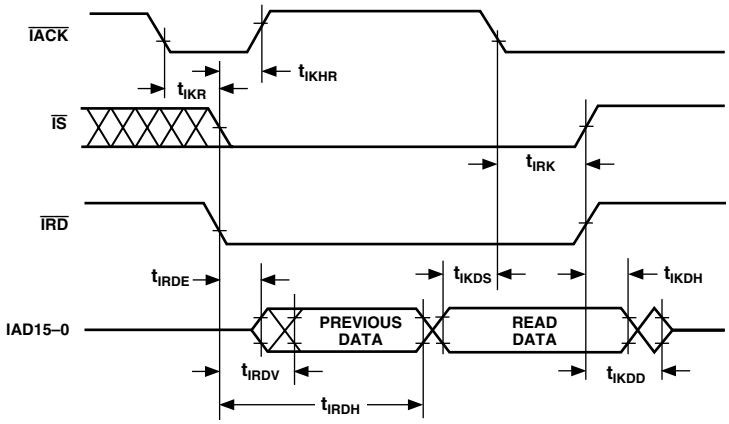


Figure 20. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP1}	Duration of Read (DM, PM1)[2]	15	$2\ t_{CK} - 5$	ns
t_{IRP2}	Duration of Read (PM2)[3]	15	$t_{CK} - 5$	ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		15	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[4]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[4]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		15	ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]DM Read or First Half of PM Read.
[3]Second Half of PM Read.
[4]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

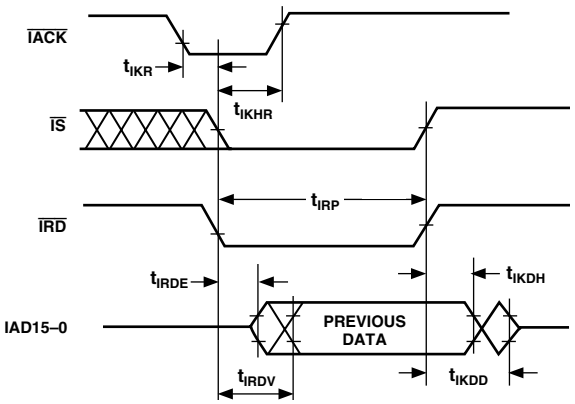
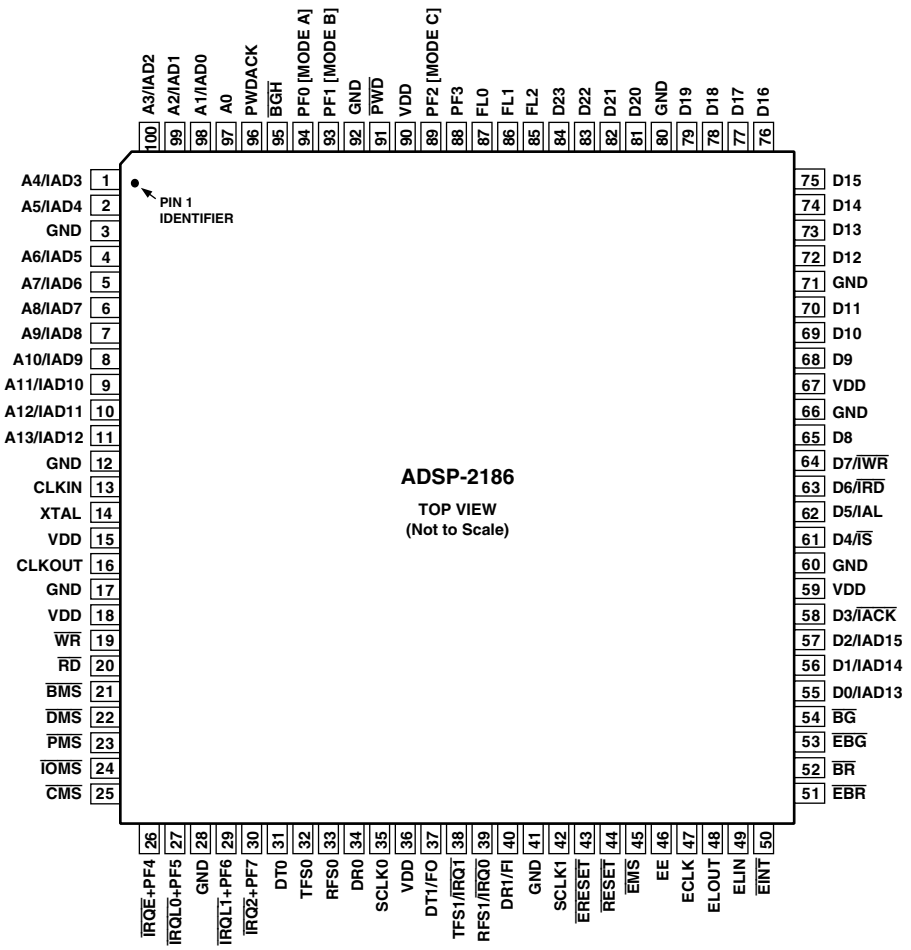


Figure 21. IDMA Read, Short Read Cycle

100-Lead LQFP Package Pinout



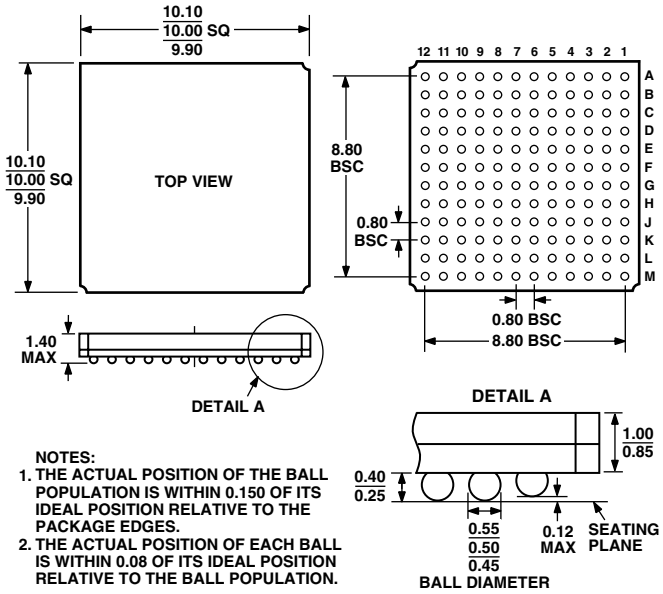
ADSP-2186 Mini-BGA (CA) Package Pinout
Bottom View

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	VDD	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	VDD	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	VDD	GND	GND	PF3	FL2	PF0 [MODE A]	FL0	A8/IAD7	VDD	VDD	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/ IAD10	A12/ IAD11	NC	A13/ IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	VDD	GND	GND	GND	CLKIN	H
VDD	VDD	D1/IAD14	$\overline{\text{BG}}$	RFS1/ $\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	VDD	VDD	NC	VDD	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/ $\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ + PF6	NC	$\overline{\text{IRQE}}$ + PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ + PF7	$\overline{\text{IRQL0}}$ + PF5	M

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

144-Ball Mini-BGA
(CA-144)



ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option*
ADSP-2186KST-115	0°C to 70°C	28.8	100-Lead LQFP	ST-100
ADSP-2186BST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100
ADSP-2186KST-133	0°C to 70°C	33.3	100-Lead LQFP	ST-100
ADSP-2186BST-133	–40°C to +85°C	33.3	100-Lead LQFP	ST-100
ADSP-2186KST-160	0°C to 70°C	40.0	100-Lead LQFP	ST-100
ADSP-2186BST-160	–40°C to +85°C	40.0	100-Lead LQFP	ST-100
ADSP-2186BCA-160	–40°C to +85°C	40.0	144-Ball Mini-BGA	CA-144

*ST = Plastic Thin Quad Flatpack (LQFP); CA = Mini-BGA.