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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	161-TBGA
Supplier Device Package	161-FBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2d35g0agb3000a

1. Product Lineup

Memory Size

Product Name		S6E2D35G0A S6E2D35J0A	S6E2D35GJA
On-chip Flash memory		384 Kbytes	
On-chip SRAM	SRAM	36 Kbytes	
	SRAM0	32 Kbytes	
	SRAM2	4 Kbytes	
VRAM for GDC		512 Kbytes	
VFLASH for GDC		-	2 Mbytes

Function

Product Name			S6E2D35G0A	S6E2D35J0A	S6E2D35GJA
Pin count			120/161	176	120
CPU			Cortex-M4F, MPU, NVIC 128ch.		
		Freq.	160 MHz		
Power supply voltage range			2.7 V to 3.6 V		
USB2.0 (Device/Host)			1ch.		
DMAC			8ch.		
DSTC			128ch.		
GDC unit	Graphics・Display controller		1 unit		
	High-Speed Quad SPI		1ch.		(VFLASH only)
	Hyper Bus Interface		1 unit		-
	SDRAM-IF		-	1ch.	-
External Bus Interface			Addr:25-bit (Max), Data: 8-/16-bit, CS:2 (Max) SRAM, NOR Flash, NAND Flash, SDRAM		
Multi-function Serial Interface (UART/CSIO/LIN/I^2C)			8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	6ch.	1 unit		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
I^2S			2 units		
QPRC			1ch.		
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes(Fixed, Programmable)		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			16 pins (Max)+ NMI × 1		
I/O ports			98 pins (Max)	154 pins (Max)	90 pins (Max)
12-bit A/D converter			24ch. (2 units)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR		High-speed	4 MHz		
		Low-speed	100 kHz		
Debug Function			SWJ-DP/ETM		
Unique ID			Yes		

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-in CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

Package \ Product Name	S6E2D35G0A	S6E2D35J0A	S6E2D35GJA
LQFP: LQM120 (0.5 mm pitch)	❍	-	❍
LQFP: LQP176 (0.5 mm pitch)	-	❍	-
FBGA: FDJ161 (0.5 mm pitch)	❍	-	-
Ex-LQFP(TEQFP): LEM120 (0.5 mm pitch)	❍		

❍: Supported

Note:

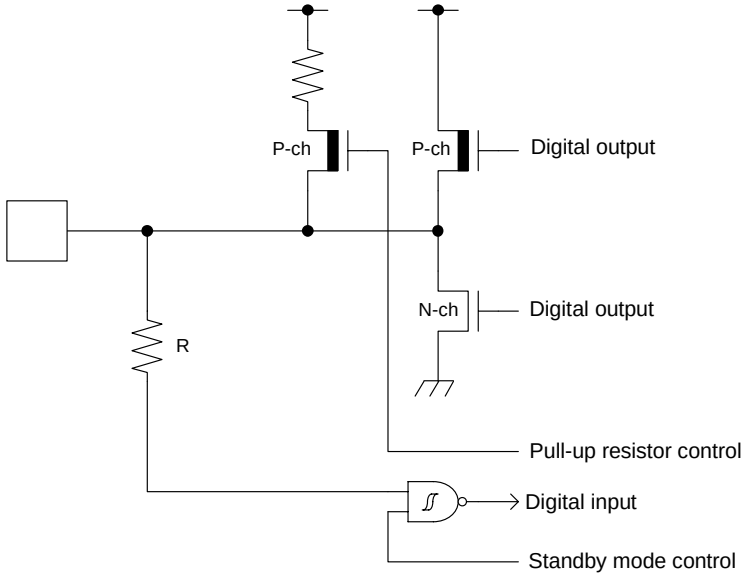
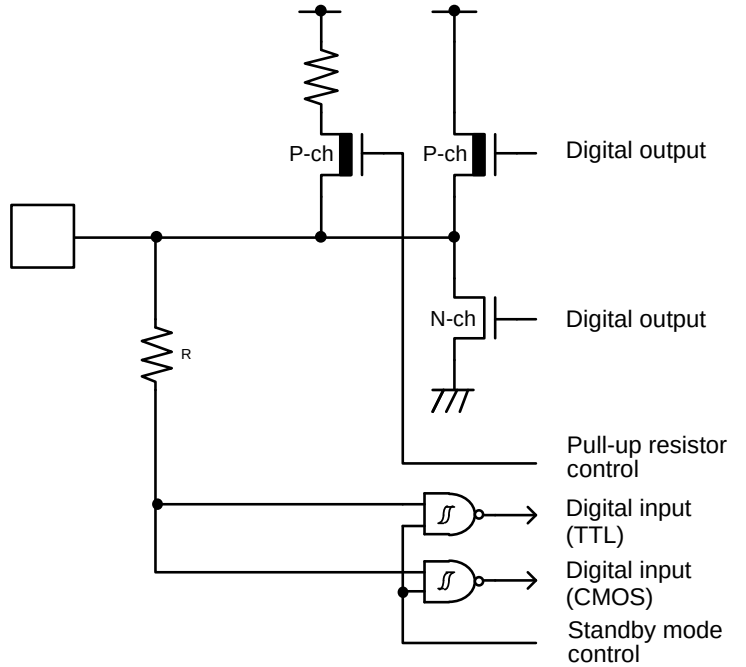
- *See 14. Package Dimensions for detailed information on each package.*

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
120	82	82	E12	P90 AN16 SIN0_1 INT08_1 PNL_PD23 PNL_TSIG11 MCLKOUT_0 MNALE_0 TRACECLK	F	O
121	83	83	E13	P91 AN17 SOT0_1 (SDA0_1) PNL_PD22 PNL_TSIG10 MAD23_0 MNCLE_0 TRACED0	F	N
122	84	84	D10	P92 AN18 SCK0_1 (SCL0_1) PNL_PD21 PNL_TSIG9 MAD22_0 MNWEX_0 TRACED1	F	N
123	85	85	D11	P93 AN19 SIN1_1 INT09_1 PNL_PD20 PNL_TSIG8 MAD21_0 MNREX_0 TRACED2	F	O
124	86	86	D12	P94 AN20 SOT1_1 (SDA1_1) PNL_PD19 PNL_TSIG7 MAD20_0 TRACED3	F	N

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
–	–	–	A1, A5, A10, A13, D5, D6, D7, D8, E5, E6, E7, E8, E9, F5, F6, F9, G4, G5, G9, H4, H5, H9, J4, J5, J6, J7, J8, J9, J10, K4, K6, K10, L6, M6, M7, M10, N1, N6, N8, N10, N13	VSS	–	–

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
GPIO	PB0	General-purpose I/O port B	47	–	–	–
	PB1		48	–	–	–
	PB2		49	–	–	–
	PB3		50	–	–	–
	PB4		56	–	–	–
	PB5		57	–	–	–
	PB6		58	–	–	–
	PB7		59	–	–	–
	PB8		72	–	–	–
	PB9		73	–	–	–
	PBA		74	–	–	–
	PBB		75	–	–	–
	PBC		76	–	–	–
	PBD		77	–	–	–
	PC0	General-purpose I/O port C	94	–	–	–
	PC1		95	–	–	–
	PC2		96	–	–	–
	PC3		97	–	–	–
	PC4		98	–	–	–
	PC5		99	–	–	–
	PC6		112	–	–	–
	PC7		113	–	–	–
	PC8		114	–	–	–
	PC9		115	–	–	–
	PCA		126	–	–	–
	PCB		127	–	–	–
	PCC		128	–	–	–
	PCD		129	–	–	–
	PD0	General-purpose I/O port D	134	–	–	–
	PD1		135	–	–	–
	PD2		136	–	–	–
	PD3		137	–	–	–
	PD4		138	–	–	–
	PD5		144	–	–	–
	PD6		145	–	–	–
	PD7		146	–	–	–
	PD8		147	–	–	–
	PD9		148	–	–	–
	PDA		166	–	–	–
	PDB		167	–	–	–
	PDC		168	–	–	–
	PDD		169	–	–	–

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
GDC SDRAM-IF (176 pin only)	GE_SDDQ24	SDRAM-IF data input / output pin	18	-	-	-
	GE_SDDQ25		17	-	-	-
	GE_SDDQ26		16	-	-	-
	GE_SDDQ27		15	-	-	-
	GE_SDDQ28		14	-	-	-
	GE_SDDQ29		13	-	-	-
	GE_SDDQ30		5	-	-	-
	GE_SDDQ31		4	-	-	-
	GE_SDDQM0	SDRAM-IF input / output mask pin	148	-	-	-
	GE_SDDQM1		147	-	-	-
	GE_SDDQM2		146	-	-	-
	GE_SDDQM3		145	-	-	-
Reset	INITX	External Reset Input pin. A reset is valid when INITX = L.	78	50	50	M8
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1 = L must be input.	84	56	56	M12
	MD0	Mode 0 pin. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	85	57	57	M11
Power	VCC	Power supply Pin	1	1	1	C1
			23	13	13	G1
			44	30	30	L1
			62	40	40	N4
			89	61	61	L13
			133	91	91	A12
			173	117	117	A4
GND	VSS	GND Pin	24	14	14	H1
			45	31	31	M1
			61	39	39	N3
			88	60	60	M13
			132	90	90	B13
			159	107	107	A7
			176	120	120	B1
Clock	X0	Main clock (oscillation) input pin	86	58	58	N11
	X0A	Sub clock (oscillation) input pin	79	51	51	N7
	X1	Main clock (oscillation) I/O pin	87	59	59	N12
	X1A	Sub clock (oscillation) I/O pin	80	52	52	N9
	CROUT_0	Built-in High-speed CR-osc clock output port	52	34	34	L4
	CROUT_1		64	42	42	N5
Analog Power	AVCC	A/D converter analog power supply pin	90	62	62	K13
	AVRL	A/D converter analog reference voltage input pin	92	64	64	J13
	AVRH	A/D converter analog reference voltage input pin	93	65	65	J12

Type	Circuit	Remarks
K		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA
L		・CMOS level output ・CMOS level hysteresis input ・TTL level hysteresis input :SDRAM-IF Data Input only ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	GPIO selected	Hi-Z / input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on Reset*1	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Sable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Internal input fixed at 0	Internal input fixed at 0	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Internal input fixed at 0	Internal input fixed at 0	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at 0 or input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected / GPIO selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, Sub crystal oscillator output pin is maintain previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, Oscillation is stopped at Stop mode and Deep standby Stop mode

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table 12-1 Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A= +85°C	T_A= +105°C
LQFP: LQM120 (0.5 mm pitch)	4 layers	38	1053	526
LQFP: LQM120 *1 (0.5 mm pitch)	4 layers	39	1026	513
LQFP: LQP176 (0.5 mm pitch)	4 layers	35	1143	571
FBGA: FDJ161 (0.5 mm pitch)	4 layers	35	1143	571
Ex-LQFP: LEM120 (0.5 mm pitch)	4 layers	18*2	2222	1111

*1: When S6E2D35GJA product.
*2: This is a case where the connection process was carried out back exposed die pad foundation. Please connect directly to GND back exposed die pad.

Notes:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7,*8 (PLL)	*5	160 MHz	185	285	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	179	276	mA	
					120 MHz	169	261	mA	
					100 MHz	161	250	mA	
					80 MHz	154	239	mA	
					60 MHz	146	227	mA	
					40 MHz	138	215	mA	
					20 MHz	130	204	mA	
					8 MHz	125	196	mA	
					4 MHz	124	195	mA	
			Normal operation *6,*7,*8 (PLL)	*5	160 MHz	45	122	mA	*3 When all peripheral clocks are OFF
					144 MHz	41	117	mA	
					120 MHz	36	111	mA	
					100 MHz	31	105	mA	
					80 MHz	26	99	mA	
					60 MHz	22	94	mA	
					40 MHz	17	89	mA	
					20 MHz	12	83	mA	
					8 MHz	10	80	mA	
					4 MHz	9	79	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*5: When not operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

Table 12-8 Typical and Maximum Current Consumption in Sleep Operation (other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *6 operation (built-in High-speed CR)	4 MHz	56	126	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					2	72	mA	*3 When all peripheral clocks are OFF
			Sleep *5,*6 operation (Sub oscillation)	32 kHz	0.52	69.65	mA	*3 When all peripheral clocks are ON
					0.51	69.65	mA	*3 When all peripheral clocks are OFF
			Sleep *6 operation (built-in Low-speed CR)	100 kHz	0.54	70.65	mA	*3 When all peripheral clocks are ON
					0.52	69.65	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

Table 12-9 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode (built-in High-speed CR)	4 MHz	1.14	2.8	mA	*3, *4 T_A=+25°C
					-	22.08	mA	*3, *4 T_A=+85°C
					-	31.3	mA	*3, *4 T_A=+105°C
			Timer mode *5 (Sub oscillation)	32 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
			Timer mode (built-in Low-speed CR)	100 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (Sub oscillation)	32 kHz	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

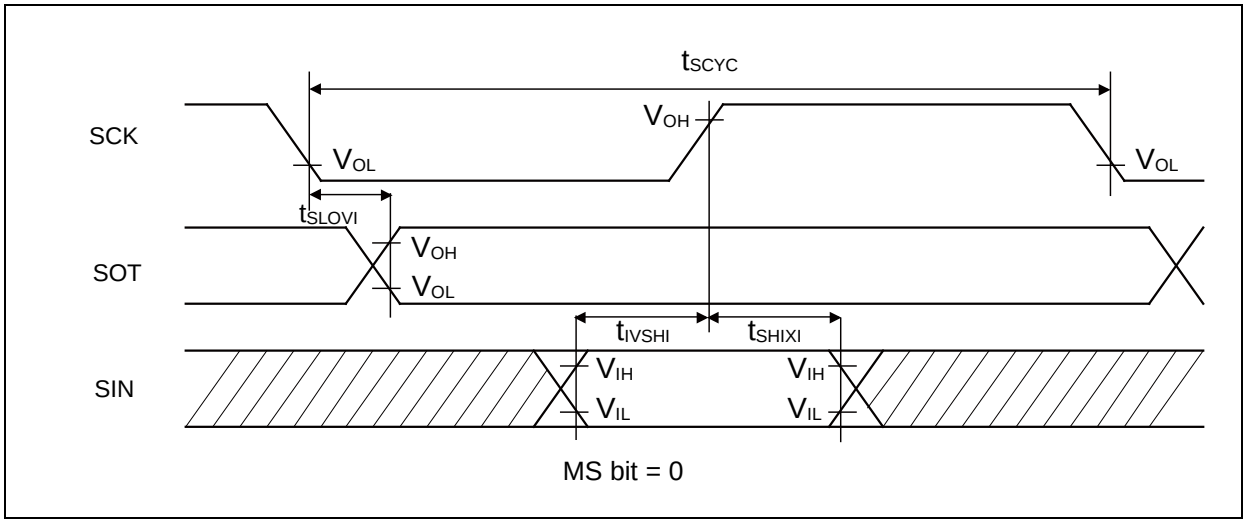
*4: When LVD is OFF

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

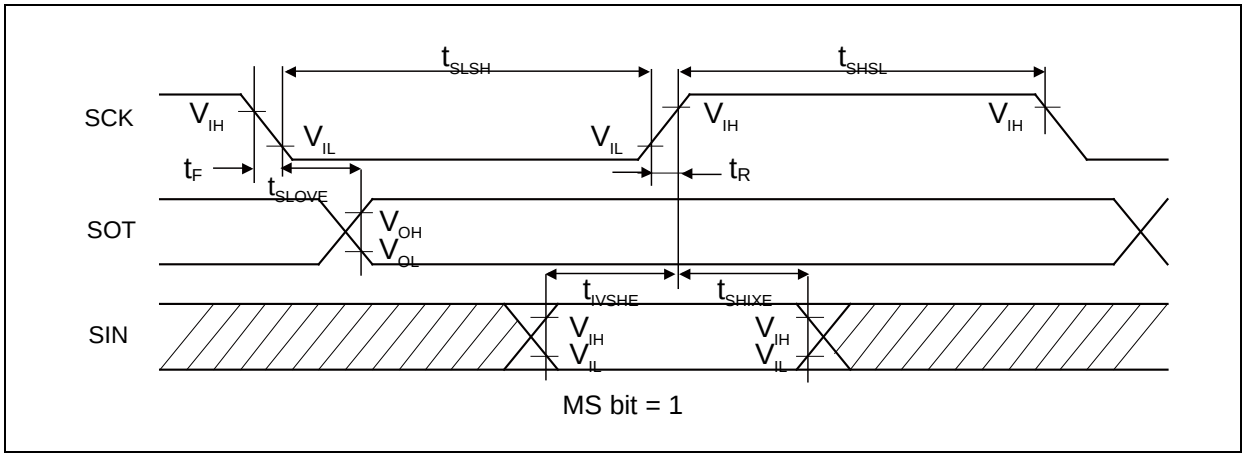
12.3.2 Pin Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	V_{CC}+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	2 mA type	I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		4 mA type	I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8 mA type	I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		11 mA type	I_{OH} = - 11 mA	V_{CC} - 0.5	-	V_{CC}	V	High-speed IO
		The pin doubled as USB I/O	I_{OH} = - 13.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
		The pin doubled as I^2C Fm+	I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
L level output voltage	V_{OL}	2 mA type	I_{OL} = 2 mA	V_{SS}	-	0.4	V	
		4 mA type	I_{OL} = 4 mA	V_{SS}	-	0.4	V	
		8 mA type	I_{OL} = 8 mA	V_{SS}	-	0.4	V	
		11 mA type	I_{OL} = 11 mA	V_{SS}	-	0.4	V	
		The pin doubled as USB I/O	I_{OL} = 10.5 mA	V_{SS}	-	0.4	V	
		The pin doubled as I^2C Fm+	I_{OL} = 3 mA	V_{SS}	-	0.4	V	At GPIO
			I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	-	30	80	200	kΩ	
			-	15	33	70		High-speed IO
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	



MS bit = 0



MS bit = 1

12.4.13 External Input Timing

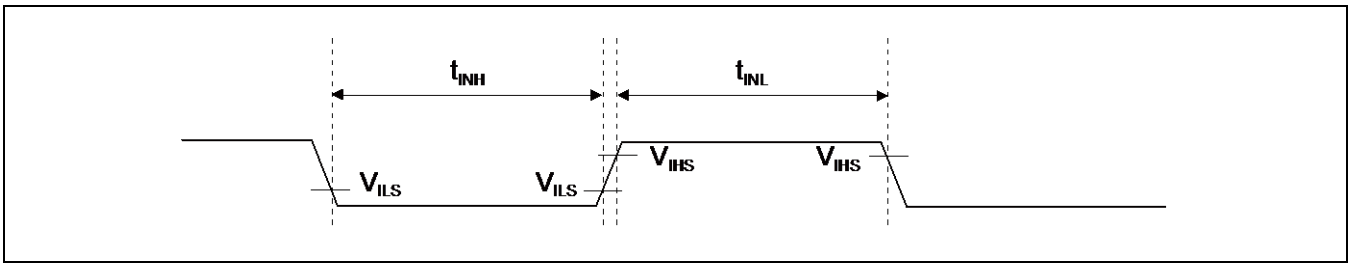
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCK0					Free-run timer input clock
		IC0x					Input capture
		DTTI0X	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx, NMIX	-	$2t_{CYCP}$ + 100(*1)	-	ns	External interrupt, NMI
				500(*2)	-	ns	
		WKUPx	-	500(*3)	-	ns	Deep standby wake up

(*1): t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which the Multi-function Timer and External interrupt are connected to, see 8. Block Diagram in this data sheet.

(*2): When in STOP mode, in timer mode.

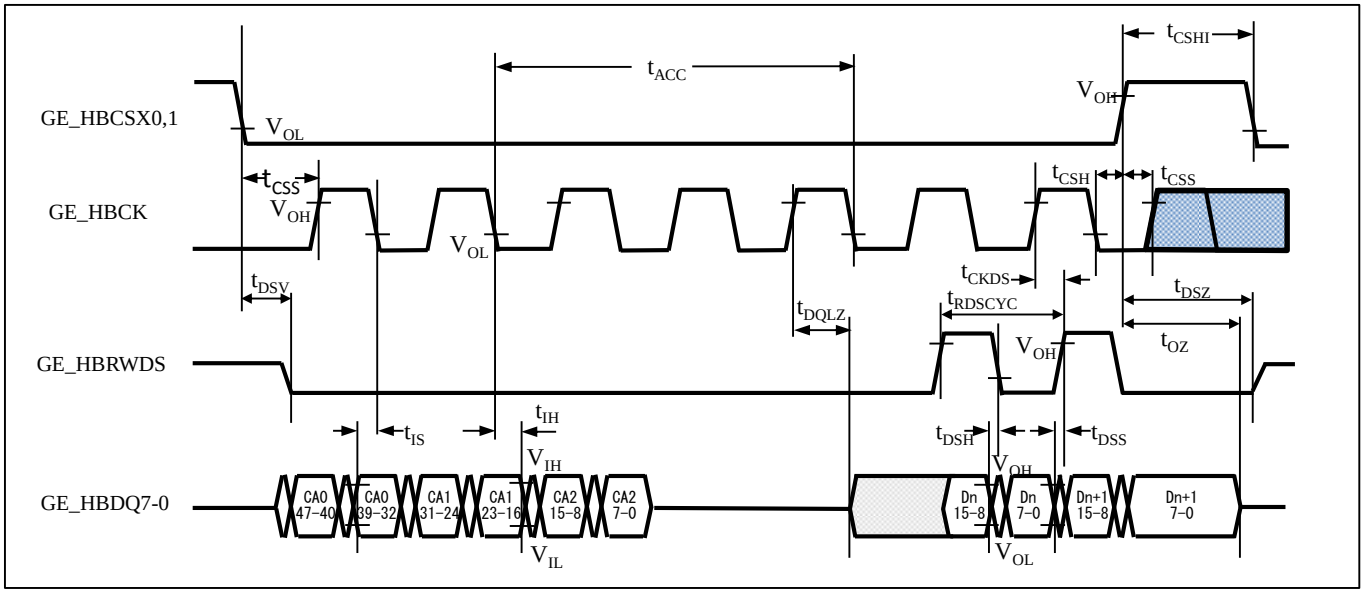
(*3): When in deep standby RTC mode, in deep standby Stop mode.



HyperFlash Read

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Hyper Bus clock cycle	t_{RDSCYC}	GE_HBCK	C_L=30pF	10	-	ns
Read initial Access Time	t_{ACC}	GE_HBCK		-	120	ns
CS↑ ↓→CK↑ Chip Select setup time	t_{CSS}	GE_HBCSX1 GE_HBCSX0		3	-	ns
CS↓ → RDS↓ Chip select active to RDS valid (Low)	t_{DSV}	GE_HBRWDS		-	8	ns
DQ → CK↑ ↓ Input setup time	t_{IS}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK↑ ↓→ DQ Input hold time	t_{IH}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK↓ → CS↑ Chip select hold time	t_{CSH}	GE_HBCSX1 GE_HBCSX0		0	-	ns
CS↑ → RDS(Hi-Z) Chip select Inactive to RDS High-Z	t_{DSZ}	GE_HBRWDS		-	7	ns
CK↑ ↓ → DQ (Low Z) Clock to DQs Low Z	t_{DQLZ}	GE_HBDQ7- GE_HBDQ0		0	-	ns
RDS↑ ↓→ DQ (valid) RDS transition to DQ valid	t_{DSS}	GE_HBDQ7- GE_HBDQ0		-0.8	+0.8	ns
RDS↑ ↓→ DQ (invalid) RDS transition to DQ invalid	t_{DSH}	GE_HBDQ7- GE_HBDQ0		-0.8	+0.8	ns
CS↑→ DQ (Hi-Z) Chip select Inactive to DQs High-Z	t_{OZ}	GE_HBDQ7- GE_HBDQ0		-	7	ns
CK↑ ↓→ RDS↑ ↓ CK transition to RDS transition	t_{CKDS}	GE_HBRWDS		1	7	ns
CS↑→ CS↓ Chip select HIGH between Operation	t_{CSHI}	GE_HBCSX1 GE_HBCSX0		8	-	ns



12.6 USB Characteristics

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-up resistance = 15kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 15kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

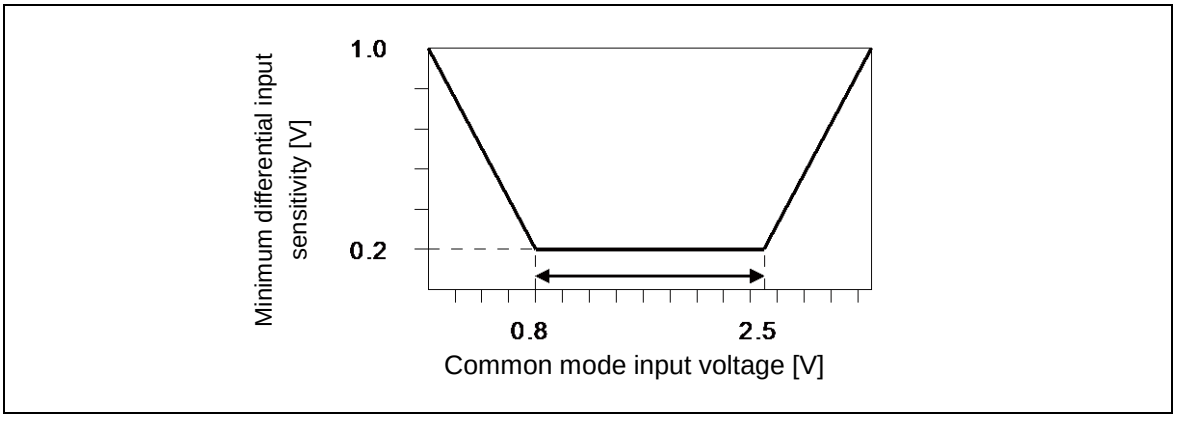
*1: The switching threshold voltage of Single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

There are some hysteresis to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.

Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

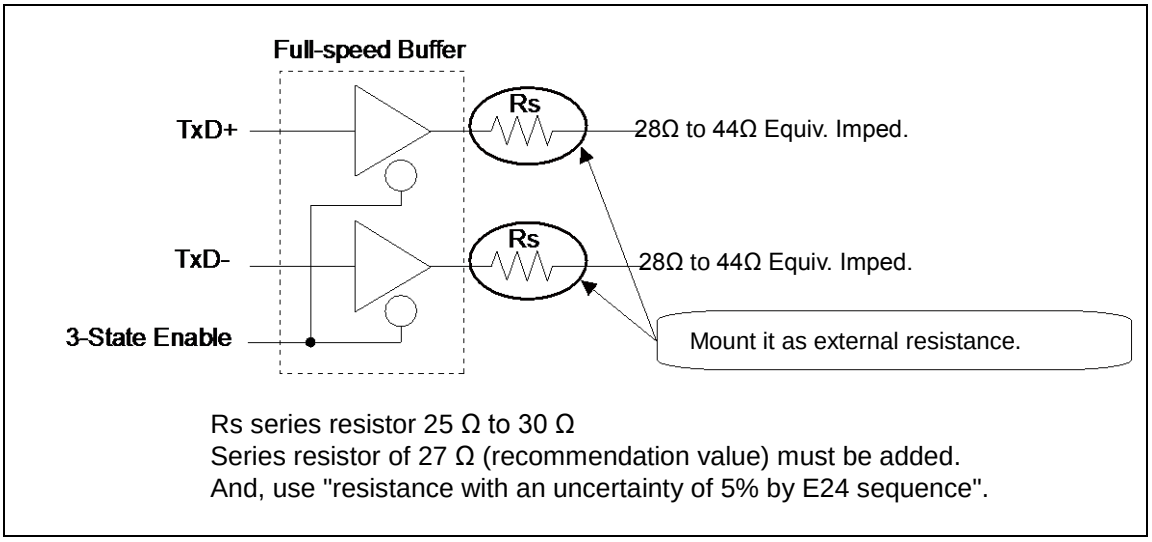
Above voltage range is the common mode input voltage range.



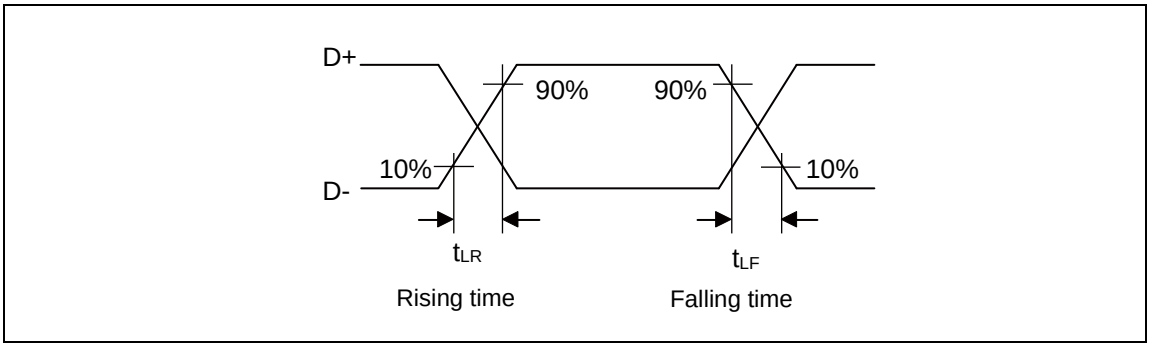
*3: The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the V_{SS} and 15 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.

*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15 % characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.



*7: They indicate rising time (t_{LR}) and Falling time (t_{LF}) of the Low-speed differential data signal.
They are defined by the time between 10 % and 90 % of the output signal voltage.



Note:

- *See Low-speed load (Compliance load) for conditions of external load.*

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode		336	667	µs	without RAM retention
Deep standby Stop mode		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)