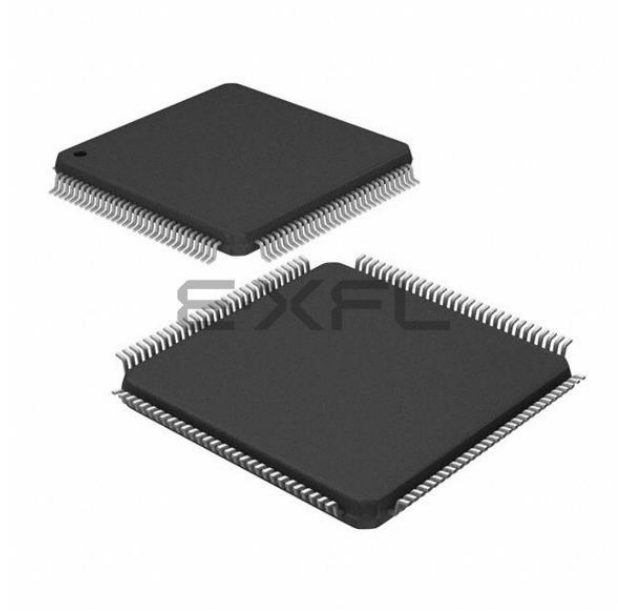

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2d35g0age20000

Table of Contents

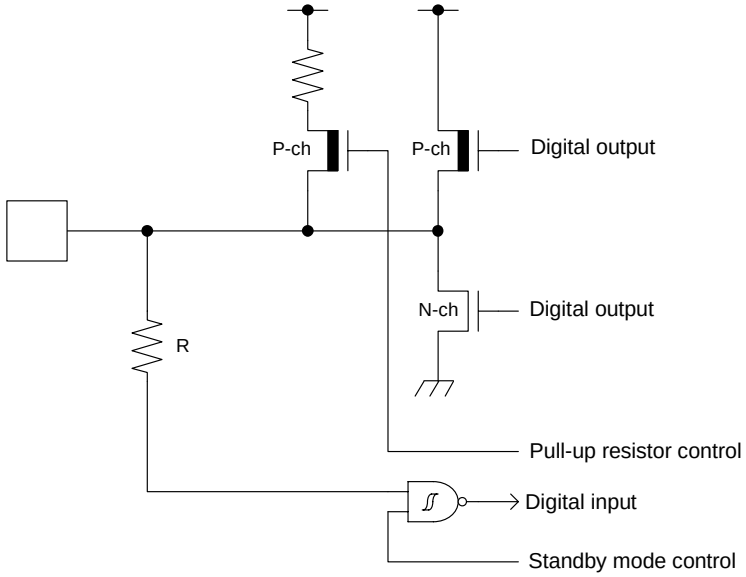
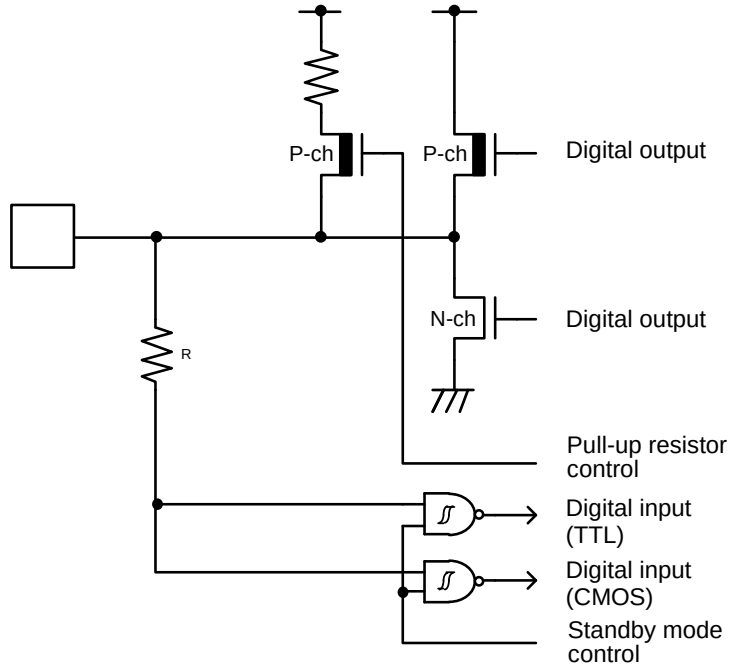
Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
141	94	94	C11	P02 TDI MAD24_0	E	H
142	95	95	B11	P03 TMS SWDIO	E	G
143	96	96	B10	P04 TDO SWO	E	G
144	–	–	–	PD5 GE_SDA0	K	I
145	–	–	–	PD6 GE_SDDQM3	K	I
146	–	–	–	PD7 GE_SDDQM2	K	I
147	–	–	–	PD8 GE_SDDQM1	K	I
148	–	–	–	PD9 GE_SDDQM0	K	I
149	97	97	C10	P05 INT10_1 PNL_PD15 MAD18_0	E	K
150	98	98	D9	P06 PNL_PD14 MAD17_0	E	I
151	99	99	C9	P07 SIN2_1 INT11_1 PNL_PD13 MAD16_0	E	K
152	100	100	B9	P08 SOT2_1 (SDA2_1) PNL_PD12 MAD15_0	E	I
153	101	101	A9	P09 SCK2_1 (SCL2_1) PNL_PD11 MAD14_0	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
154	102	102	C8	P0A SIN5_1 TIOA7_1 INT12_1 PNL_PD10 MAD13_0	E	K
155	103	103	B8	P0B SOT5_1 (SDA5_1) TIOB7_1 PNL_PD9 MAD12_0	E	I
156	104	104	A8	P0C SCK5_1 (SCL5_1) PNL_PD8 MAD11_0	E	I
157	105	105	C7	P0D PNL_PD7 MSDWEX_0	D	I
158	106	106	B7	P0E WKUP2 PNL_PD6 MCSX8_0	D	P
159	107	107	A7	VSS	—	—
160	108	108	C6	P68 SCK3_1 (SCL3_1) PNL_PD5 MSDCLK_0	D	I
161	109	109	B6	P67 SOT3_1 (SDA3_1) PNL_PD4 MSDCKE_0	D	I
162	110	110	A6	P66 SIN3_1 INT13_1 PNL_PD3	E	K
163	111	111	C5	P65 PNL_PD2	E	I
164	112	112	B5	P64 CTS4_0 PNL_PD1	E	I

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	81	53	53	M9
Analog GND	AVSS	A/D converter GND pin	91	63	63	K12
C Pin	C	Power supply stabilization capacity pin	60	38	38	N2

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

Type	Circuit	Remarks
K		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA
L		・CMOS level output ・CMOS level hysteresis input ・TTL level hysteresis input :SDRAM-IF Data Input only ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	GPIO selected	Hi-Z / input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	WKUP input enabled
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ Internal input fixed at 0 at reception	Hi-Z at trans-mission/ Internal input fixed at 0 at reception	Hi-Z / input enabled	Hi-Z / input enabled	Hi-Z / input enabled	Hi-Z / input enabled

*1: Oscillation is stopped at Sub timer mode, low-speed CR timer mode, RTC mode, Stop mode, Deep standby RTC mode, and Deep standby Stop mode.

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *5,*6 operation (PLL)	72 MHz	84	160	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
				60 MHz	80	155	mA	
				48 MHz	75	150	mA	
				36 MHz	71	145	mA	
				24 MHz	67	141	mA	
				12 MHz	63	137	mA	
				8 MHz	61	134	mA	
				4 MHz	60	133	mA	
				72 MHz	15	82	mA	*3 When all peripheral clocks are OFF
				60 MHz	13	80	mA	
				48 MHz	12	79	mA	
				36 MHz	10	77	mA	
				24 MHz	8	75	mA	
				12 MHz	7	74	mA	
				8 MHz	6	73	mA	
				4 MHz	5	72	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

Table 12-9 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode (built-in High-speed CR)	4 MHz	1.14	2.8	mA	*3, *4 T_A=+25°C
					-	22.08	mA	*3, *4 T_A=+85°C
					-	31.3	mA	*3, *4 T_A=+105°C
			Timer mode *5 (Sub oscillation)	32 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
			Timer mode (built-in Low-speed CR)	100 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (Sub oscillation)	32 kHz	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep Standby Stop mode (When RAM is OFF)	-	108	173	µA	*3, *4 T_A=+25°C
					-	1774	µA	*3, *4 T_A=+85°C
					-	2208	µA	*3, *4 T_A=+105°C
			Deep Standby Stop mode (When RAM is ON)	-	112	177	µA	*3, *4 T_A=+25°C
					-	1778	µA	*3, *4 T_A=+85°C
					-	2212	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep Standby RTC mode (When RAM is OFF)	32 kHz	109	174	µA	*3, *4 T_A=+25°C
					-	1771	µA	*3, *4 T_A=+85°C
					-	2205	µA	*3, *4 T_A=+105°C
			Deep Standby RTC mode (When RAM is ON)		113	178	µA	*3, *4 T_A=+25°C
					-	1775	µA	*3, *4 T_A=+85°C
					-	2209	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop *8	-	0.009	0.032	µA	*3, *4, *5 T_A=+25°C
					-	0.994	µA	*3, *4, *5 T_A=+85°C
					-	1.491	µA	*3, *4, *5 T_A=+105°C
			RTC *6, *8 operation		1.0	1.636	µA	*3, *4 T_A=+25°C
					-	2.828	µA	*3, *4 T_A=+85°C
					-	4.242	µA	*3, *4 T_A=+105°C
			RTC *7, *8 operation		0.7	1.153	µA	*3, *4 T_A=+25°C
					-	2.277	µA	*3, *4 T_A=+85°C
					-	3.416	µA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)
When the Standard setting (CCS/CCB=11001110)

*7: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)
When the low power setting (CCS/CCB=00000100)

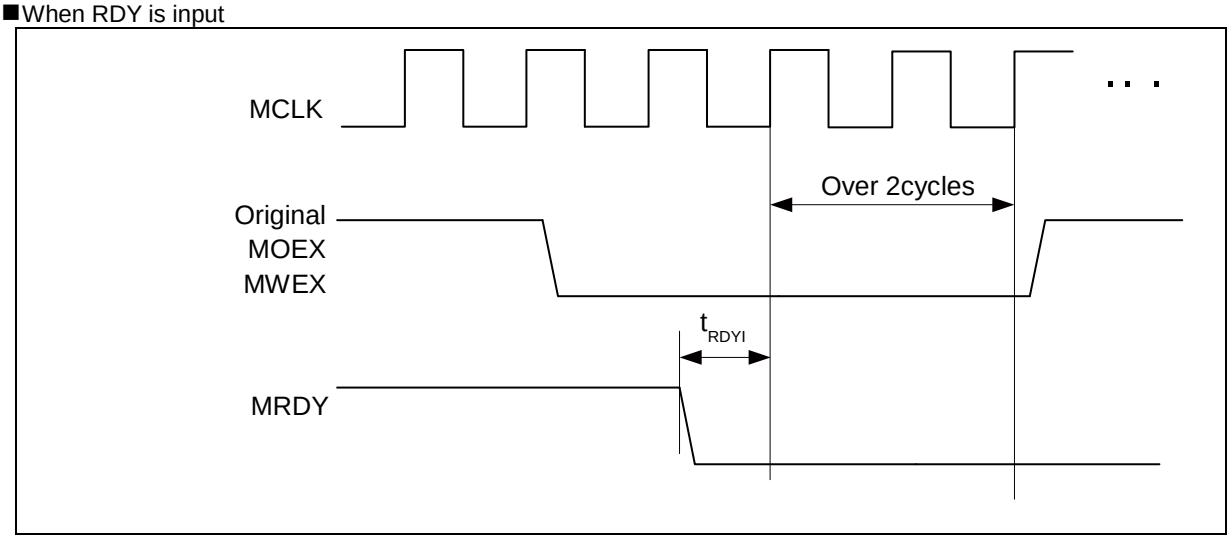
*8: In the case of setting RTC after VCC power on

External Ready Input Timing

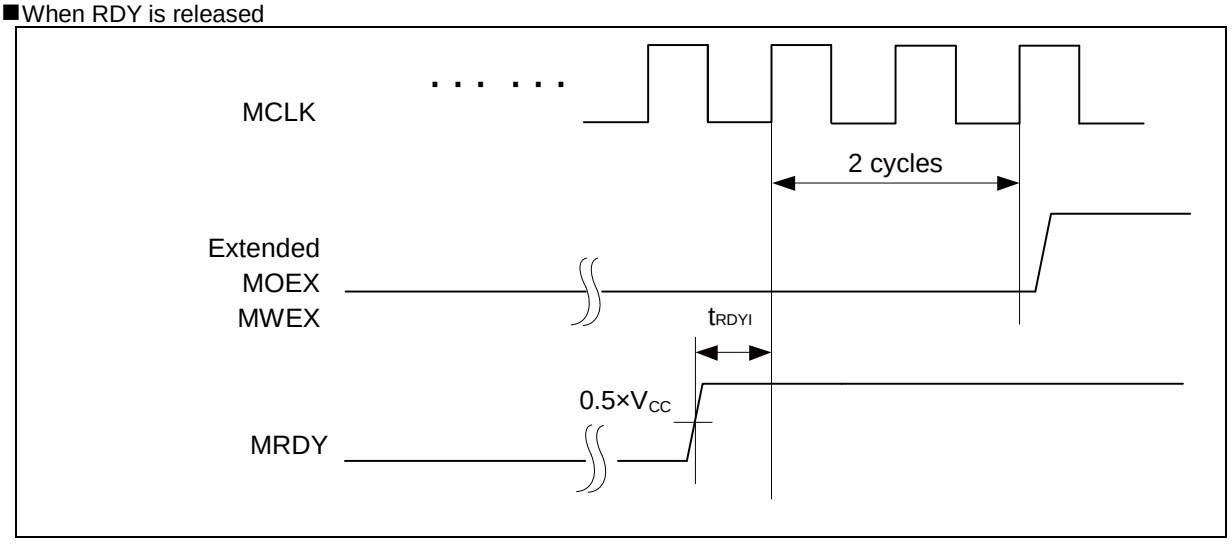
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input



■When RDY is released



Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

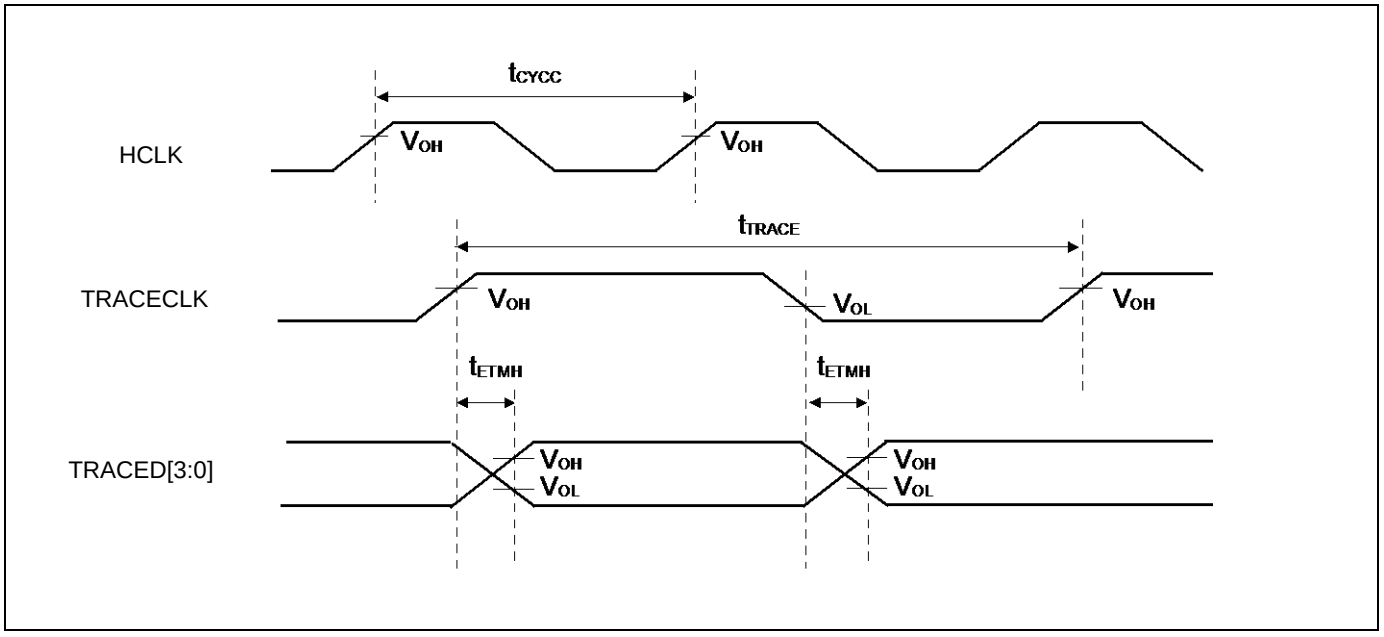
Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	-	2	15	ns	
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	-		32	MHz	
TRACECLK clock cycle	t_{TRACE}		-	31.25	-	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*



12.4.18 I²S Timing

Master Mode Timing

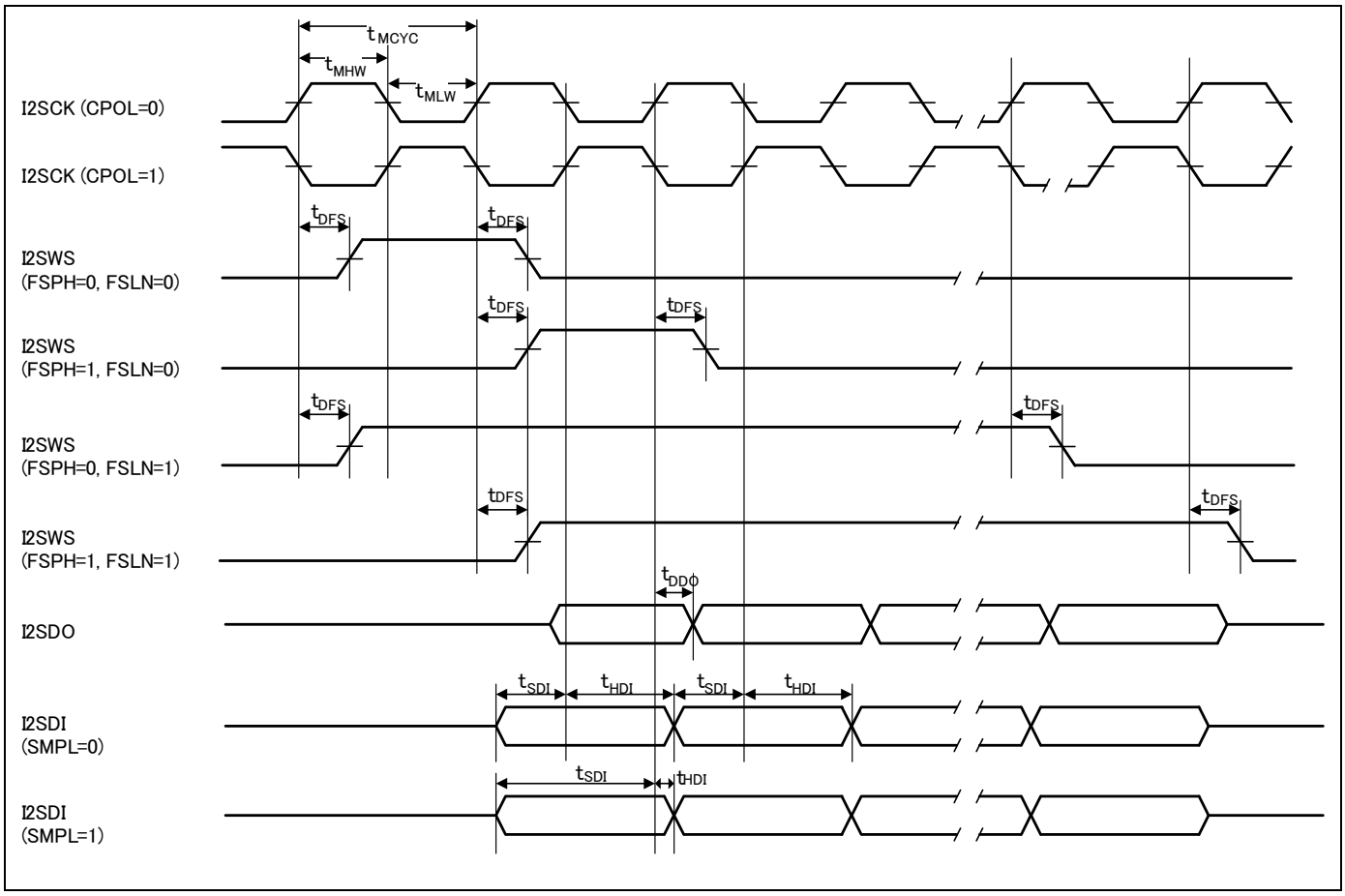
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rising time	t_{RI}	I2SDI	-	-	5	ns	
Input signal falling time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

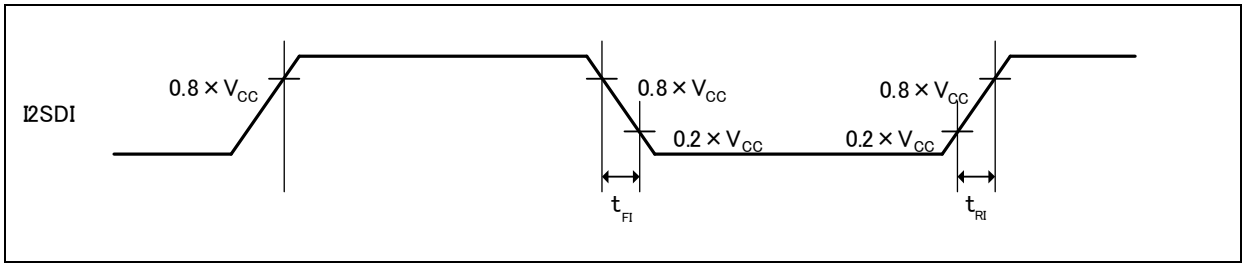
Notes:

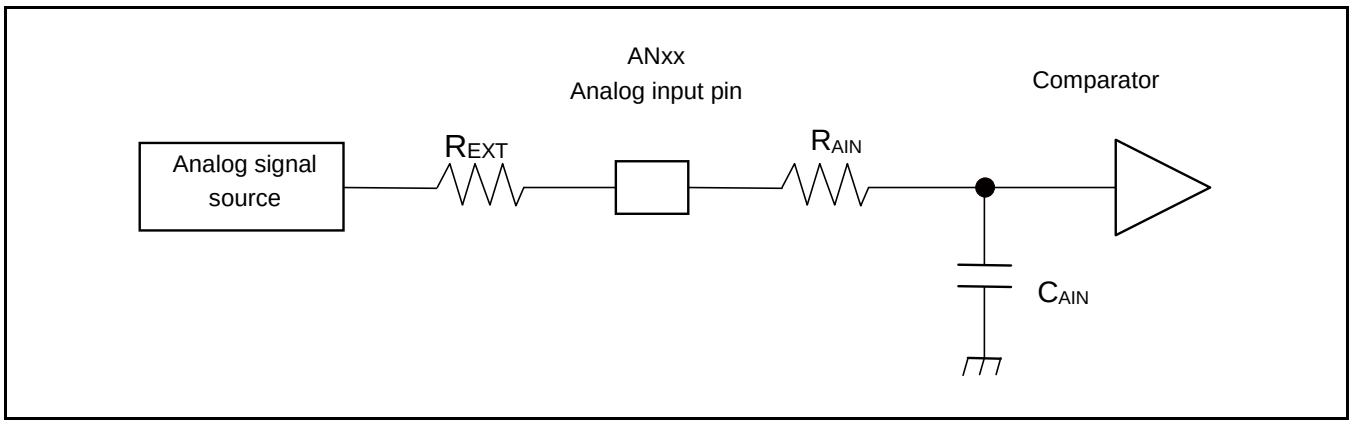
- *When the external load capacitance C_L = 20 pF*
- *When I2SWS=48 kHz, I2MCLK=256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details.



Note:

- *See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details of CPOL, FSPH, FSLIN, SMPL .*





(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.8 kΩ

C_{AIN}: Input capacity of A/D = 12.05 pF

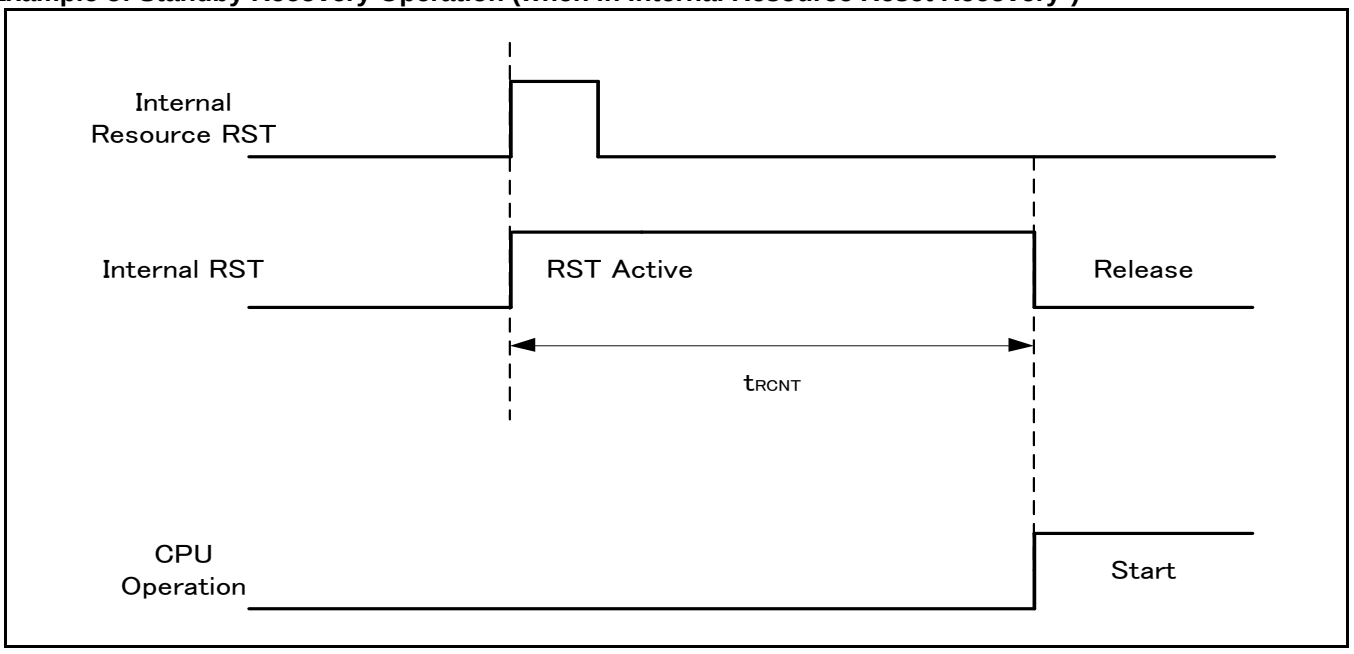
R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the Low-Power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: The return factor from each low power consumption modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856)*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-on Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*