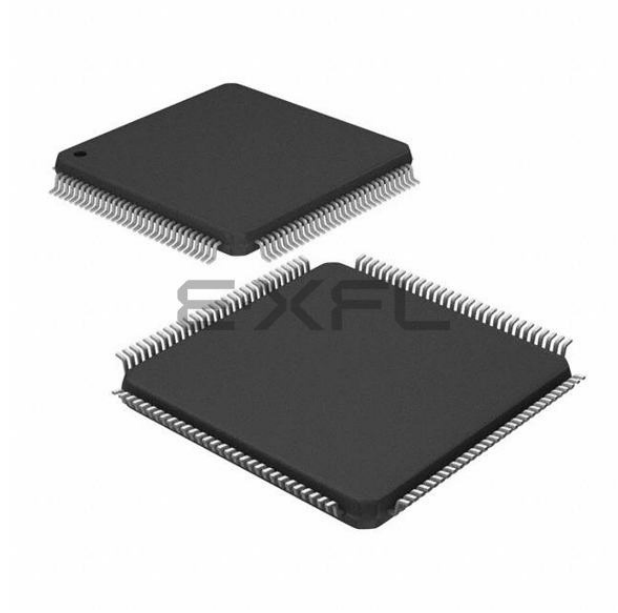

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What is "Embedded - Microcontrollers"?

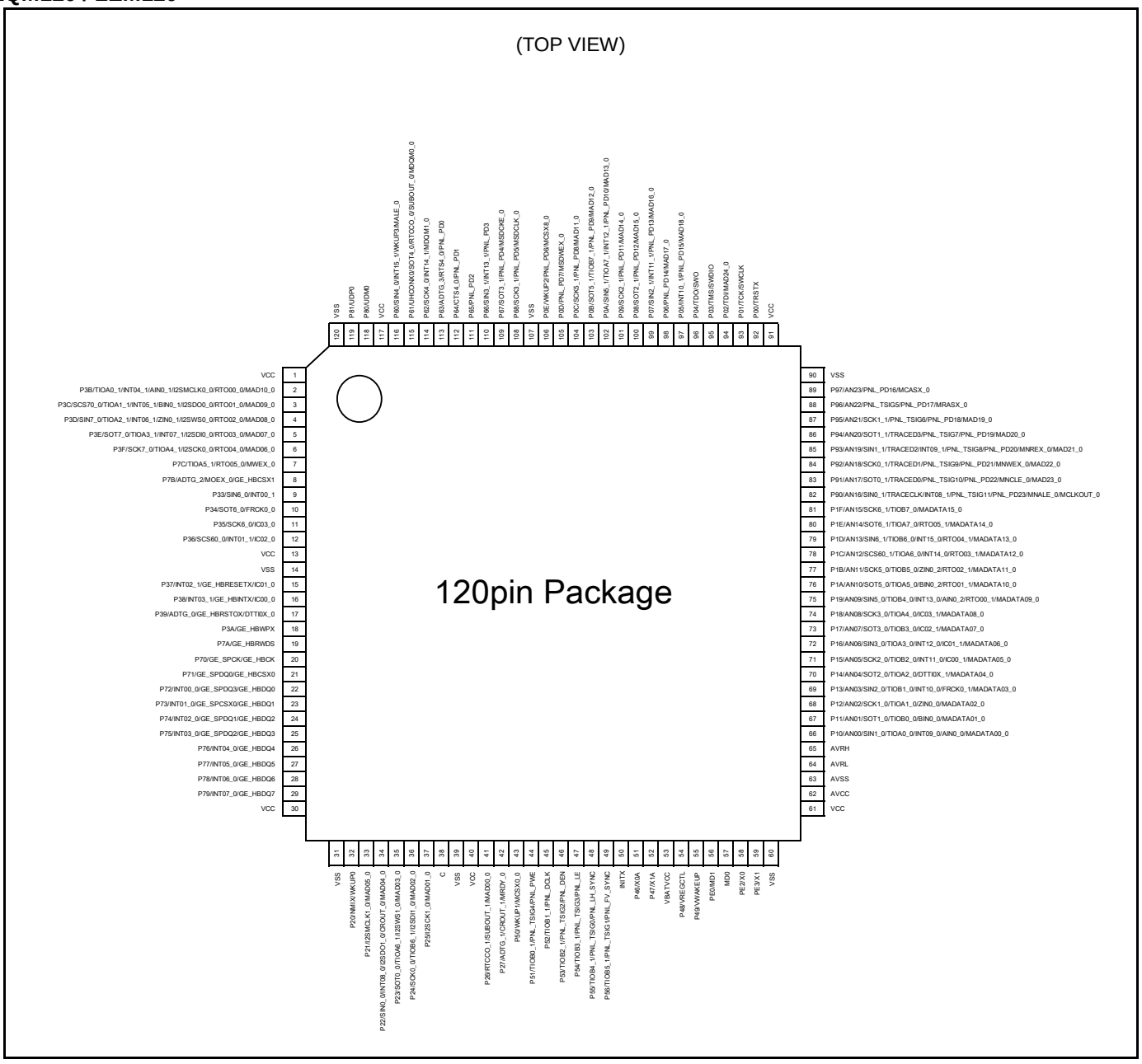
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2d35g0agv20000

3. Pin Assignment

LQM120 / LEM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
9	5	5	D2	P3E SOT7_0 (SDA7_0) TIOA3_1 INT07_1 I2SDI0_0 RTO03_0 (PPG02_0) MAD07_0	G	K
10	6	6	D1	P3F SCK7_0 (SCL7_0) TIOA4_1 I2SCK0_0 RTO04_0 (PPG04_0) MAD06_0	G	I
11	7	7	D4	P7C TIOA5_1 RTO05_0 (PPG04_0) MWEX_0	G	I
12	8	–	E4	P7B ADTG_2 GE_HBCSX1 MOEX_0	K	I
–	–	8	–	P7B ADTG_2 MOEX_0	K	I
13	–	–	–	PA8 GE_SDDQ29	L	I
14	–	–	–	PA9 GE_SDDQ28	L	I
15	–	–	–	PAA GE_SDDQ27	L	I
16	–	–	–	PAB GE_SDDQ26	L	I
17	–	–	–	PAC GE_SDDQ25	L	I
18	–	–	–	PAD GE_SDDQ24	L	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
113	–	–	–	PC7	K	I
				GE_SDBA0		
114	–	–	–	PC8	K	I
				GE_SDA11		
115	–	–	–	PC9	K	I
				GE_SDA10		
116	78	78	F12	P1C	F	M
				AN12		
				SCS60_1		
				TIOA6_0		
				INT14_0		
				RTO03_1 (PPG02_1)		
				MADATA12_0		
117	79	79	F13	P1D	F	M
				AN13		
				SIN6_1		
				TIOB6_0		
				INT15_0		
				RTO04_1 (PPG04_1)		
				MADATA13_0		
118	80	80	E10	P1E	F	L
				AN14		
				SOT6_1 (SDA6_1)		
				TIOA7_0		
				RTO05_1 (PPG04_1)		
				MADATA14_0		
119	81	81	E11	P1F	F	L
				AN15		
				SCK6_1 (SCL6_1)		
				TIOB7_0		
				MADATA15_0		

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
External Bus	MDQM0_0	External bus interface byte mask signal output pin	171	115	115	B3
	MDQM1_0		170	114	114	B4
	MALE_0	External bus interface Address Latch enable output signal for multiplex	172	116	116	B2
	MRDY_0	External bus interface external RDY input signal	64	42	42	N5
	MCLKOUT_0	External bus interface external clock output pin	120	82	82	E12
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	120	82	82	E12
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	121	83	83	E13
	MNREX_0	External bus interface read enable signal to control NAND Flash output pin	123	85	85	D11
	MNWEX_0	External bus interface write enable signal to control NAND Flash output pin	122	84	84	D10
	MOEX_0	External bus interface read enable signal for SRAM	12	8	8	E4
	MWEX_0	External bus interface write enable signal for SRAM	11	7	7	D4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	160	108	108	C6
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	161	109	109	B6
	MRASX_0	SDRAM interface SDRAM row active strobe pin	130	88	88	C12
	MCASX_0	SDRAM interface SDRAM column active strobe pin	131	89	89	C13
	MSDWEX_0	SDRAM interface SDRAM write enable pin	157	105	105	C7
External Interrupt	INT00_0	External interrupt request 00 input pin	36	22	-	H2
	INT00_1		19	9	9	E3
	INT01_0	External interrupt request 01 input pin	37	23	-	H3
	INT01_1		22	12	12	F4
	INT02_0	External interrupt request 02 input pin	38	24	-	J2
	INT02_1		25	15	15	F3
	INT03_0	External interrupt request 03 input pin	39	25	-	J3
	INT03_1		26	16	16	F2
	INT04_0	External interrupt request 04 input pin	40	26	-	K2
	INT04_1		6	2	2	C3
	INT05_0	External interrupt request 05 input pin	41	27	27	K3
	INT05_1		7	3	3	C2
	INT06_0	External interrupt request 06 input pin	42	28	28	L2
	INT06_1		8	4	4	D3
	INT07_0	External interrupt request 07 input pin	43	29	29	L3
	INT07_1		9	5	5	D2
	INT08_0	External interrupt request 08 input pin	52	34	34	L4
	INT08_1		120	82	82	E12
	INT09_0	External interrupt request 09 input pin	100	66	66	K11
	INT09_1		123	85	85	D11

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
I^2S 0	I2SMCLK0_0	I^2S ch.0 external clock pin	6	2	2	C3
	I2SDO0_0	I^2S ch.0 serial transition data output pin	7	3	3	C2
	I2SWS0_0	I^2S ch.0 frame synchronization signal pin	8	4	4	D3
	I2SDI0_0	I^2S ch.0 serial received data input pin	9	5	5	D2
	I2SCK0_0	I^2S ch.0 bit clock pin	10	6	6	D1
I^2S 1	I2SMCLK1_0	I^2S ch.1 external clock pin	51	33	33	M3
	I2SDO1_0	I^2S ch.1 serial transition data output pin	52	34	34	L4
	I2SWS1_0	I^2S ch.1 frame synchronization signal pin	53	35	35	M4
	I2SDI1_0	I^2S ch.1 serial received data input pin	54	36	36	K5
	I2SCK1_0	I^2S ch.1 bit clock pin	55	37	37	L5
GDC High-Speed Quad SPI	GE_SPCK	SPI clock output pin	34	20	-	J1
	GE_SPDQ0	SPI data input / output pin	35	21	-	K1
	GE_SPDQ1		38	24	-	J2
	GE_SPDQ2		39	25	-	J3
	GE_SPDQ3		36	22	-	H2
	GE_SPCSX0	SPI chip select output pin	37	23	-	H3
GDC HyperBus I/F	GE_HBCK	HBI clock output pin	34	20	-	J1
	GE_HBDQ0	HBI data input / output pin	36	22	-	H2
	GE_HBDQ1		37	23	-	H3
	GE_HBDQ2		38	24	-	J2
	GE_HBDQ3		39	25	-	J3
	GE_HBDQ4		40	26	-	K2
	GE_HBDQ5		41	27	-	K3
	GE_HBDQ6		42	28	-	L2
	GE_HBDQ7		43	29	-	L3
	GE_HBCSX0	HBI chip select output pin	35	21	-	K1
	GE_HBCSX1		12	8	-	E4
	GE_HBRWDS	HBI RWDS input / output pin	33	19	-	G2
	GE_HBRESETX	HBI hardware reset output pin	25	15	-	F3
	GE_HBINTX	HBI interrupt input pin	26	16	-	F2
	GE_HBRSTOX	HBI reset input pin	27	17	-	F1
	GE_HBWPX	HBI write protect output pin	28	18	-	G3

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

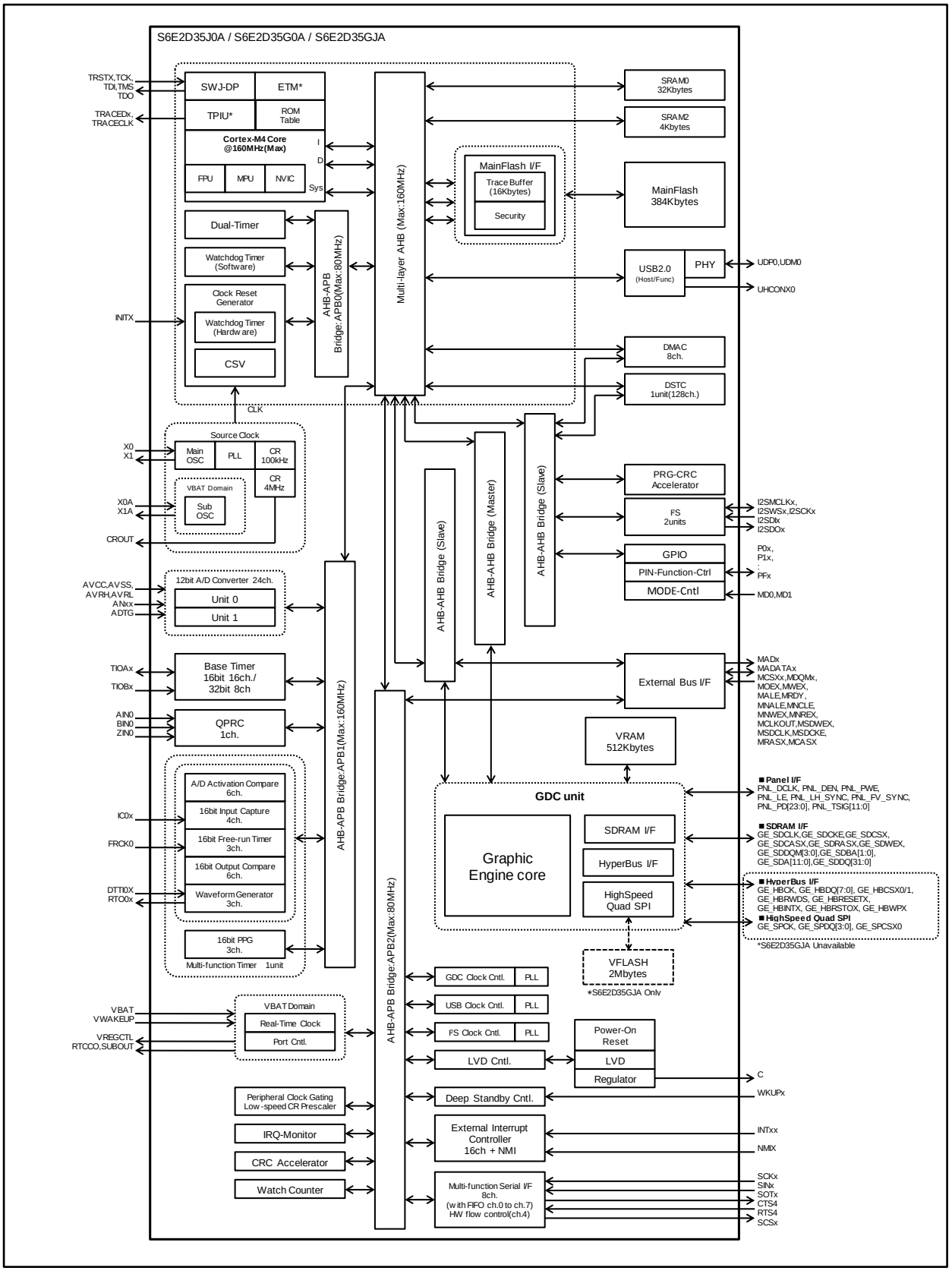
   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Block Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	160 MHz	182	279	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	176	270	mA	
					120 MHz	167	256	mA	
					100 MHz	159	244	mA	
					80 MHz	151	233	mA	
					60 MHz	143	221	mA	
					40 MHz	136	210	mA	
					20 MHz	128	199	mA	
					8 MHz	123	191	mA	
					4 MHz	122	190	mA	
			Normal operation , *6,*7 (PLL)	*5	160 MHz	43	117	mA	*3 When all peripheral clocks are OFF
					144 MHz	39	112	mA	
					120 MHz	34	106	mA	
					100 MHz	29	100	mA	
					80 MHz	24	95	mA	
					60 MHz	20	90	mA	
					40 MHz	15	84	mA	
					20 MHz	10	78	mA	
					8 MHz	7	74	mA	
					4 MHz	6	73	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to main flash memory and VFLASH memory

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation , *6,*7,*8 (PLL)	*5	72 MHz	168	251	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					60 MHz	161	242	mA	
					48 MHz	154	233	mA	
					36 MHz	147	224	mA	
					24 MHz	140	214	mA	
					12 MHz	133	205	mA	
					8 MHz	131	202	mA	
					4 MHz	128	199	mA	
				*5	72 MHz	41	114	mA	*3 When all peripheral clocks are OFF
					60 MHz	36	108	mA	
					48 MHz	32	104	mA	
					36 MHz	27	98	mA	
					24 MHz	23	94	mA	
					12 MHz	18	88	mA	
					8 MHz	17	87	mA	
					4 MHz	15	85	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

12.4.10 External Bus Timing

External Bus Clock Output Characteristics

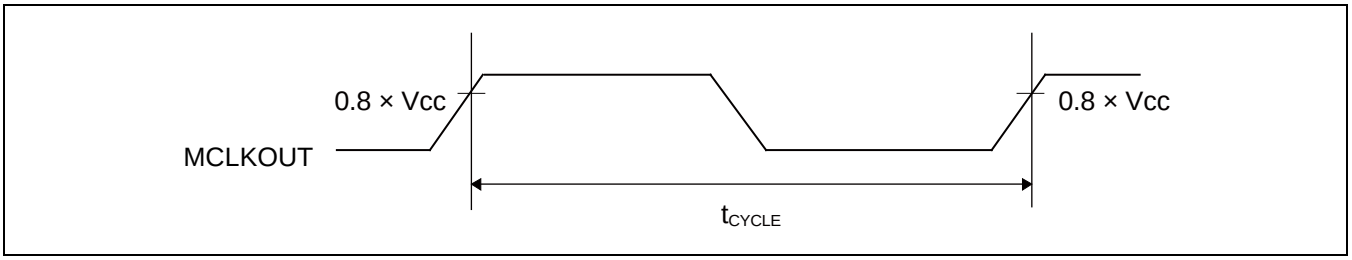
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCLE}	MCLKOUT*1		-	50*2	MHz	

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.

For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

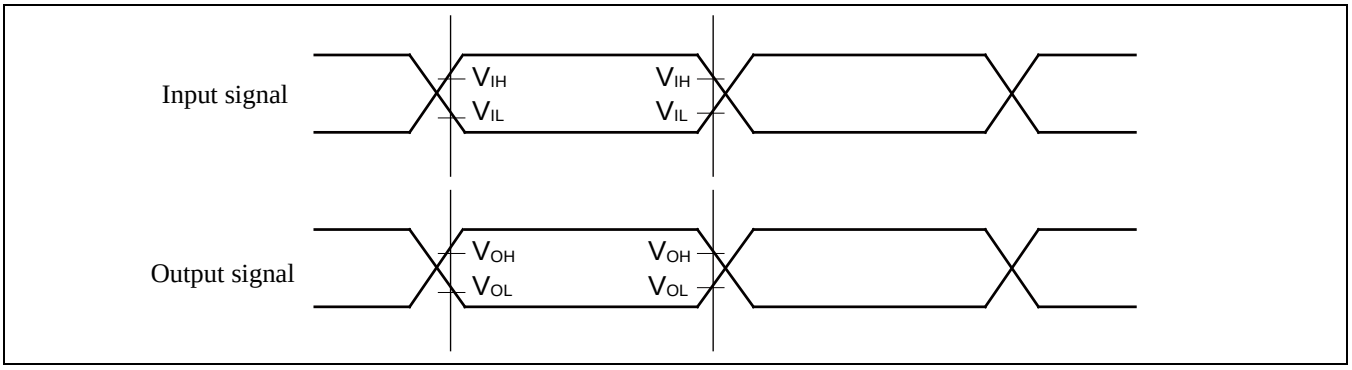
*2: Generate MCLKOUT at setting more than 4 divisions when the AHB bus clock exceeds 100 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



12.4.12 CSIO Timing

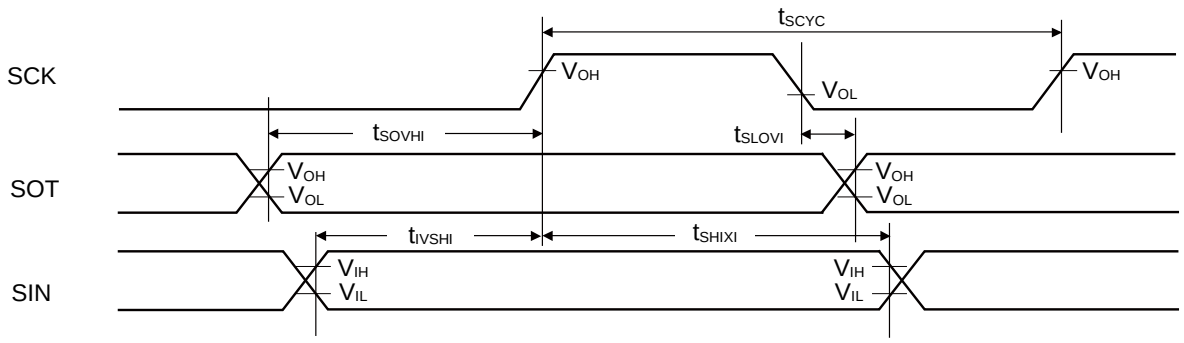
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

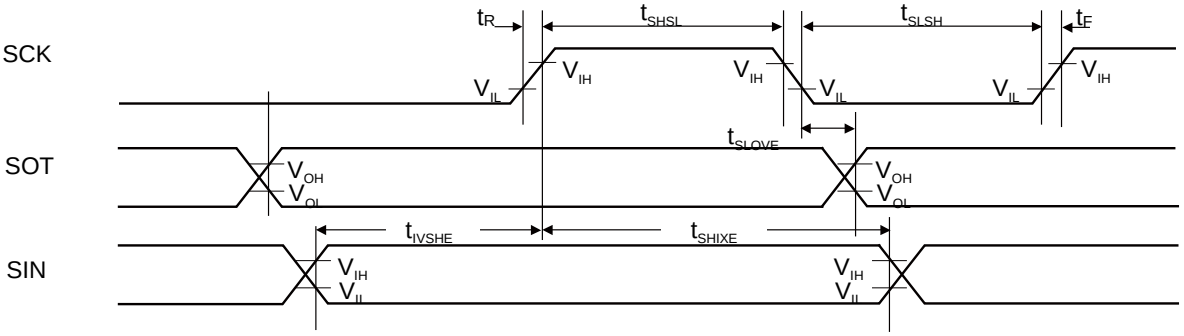
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-		-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

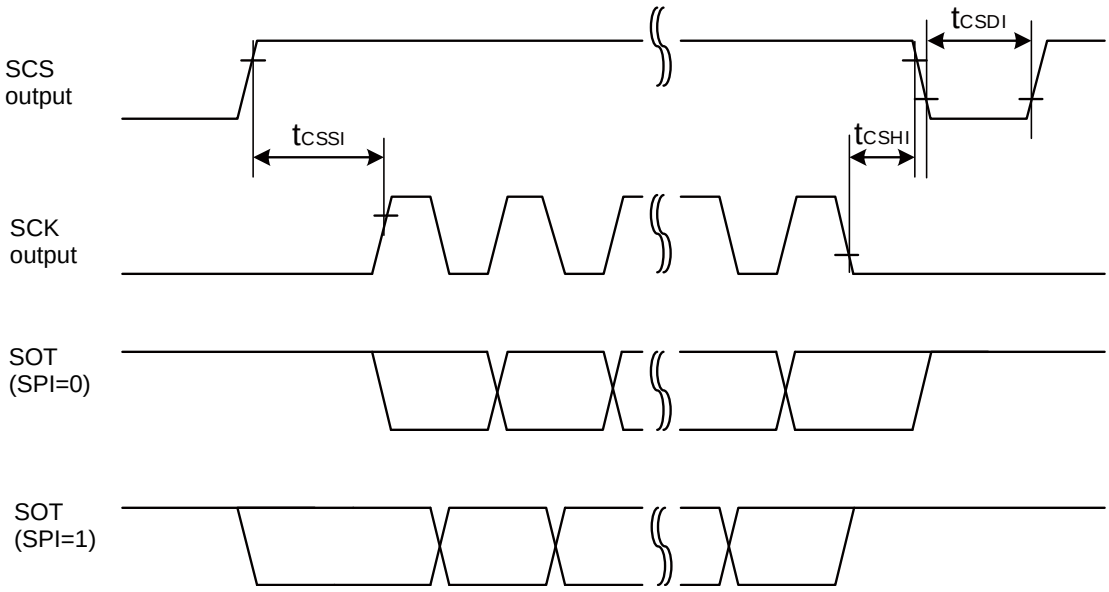
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

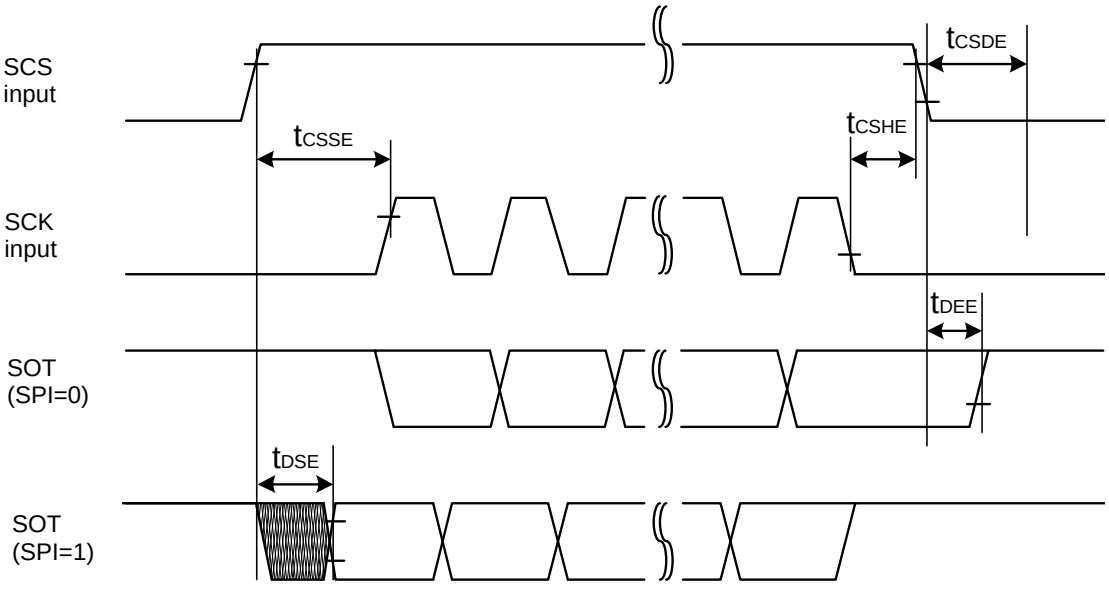
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

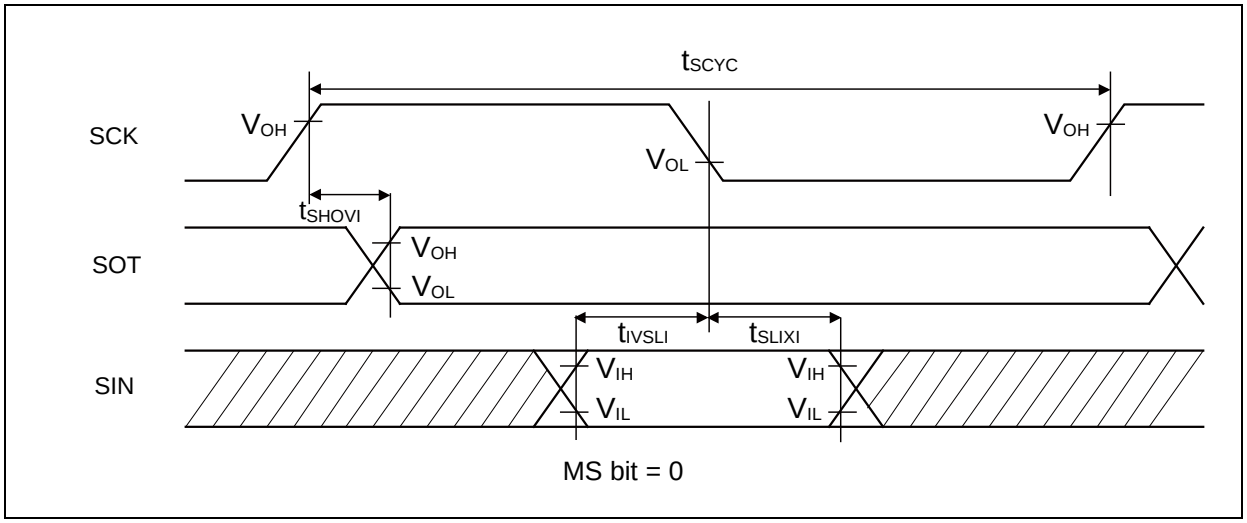
High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

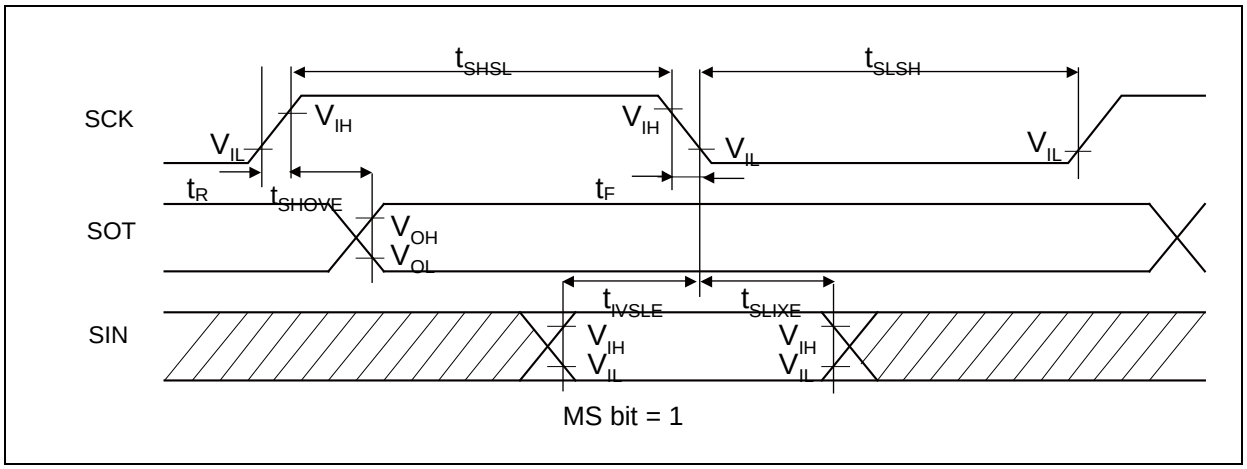
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



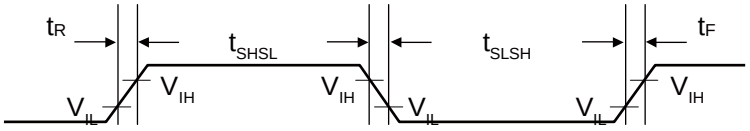
MS bit = 1

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	

SCK



12.4.15 I²C Timing

Standard Mode, Fast Mode

(V_{CC} = 2.7V to 3.6, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I²C bus device can be used on a Standard mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.

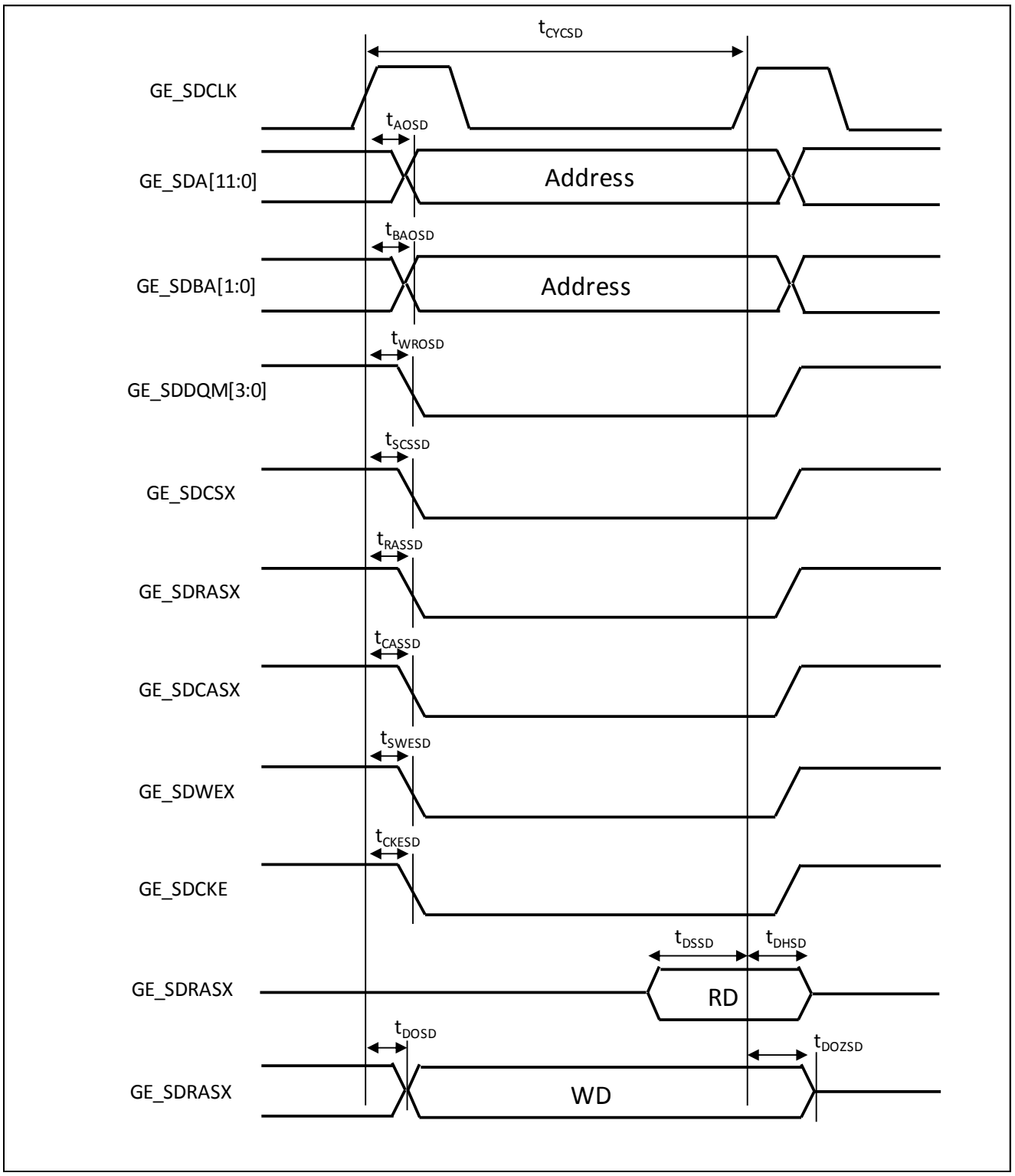
About the APB bus number that I²C is connected to, see 8. Block Diagram in this data sheet.

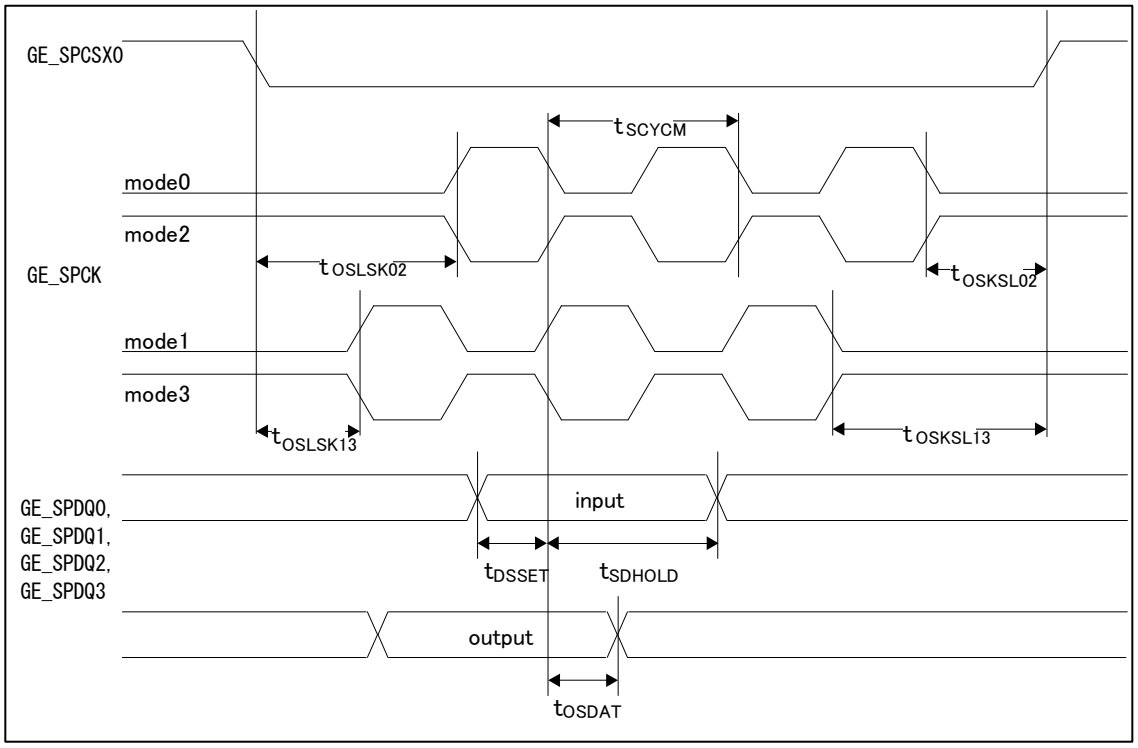
When the standard mode is used, please set to 2 MHz or more peripheral bus clock.

When fast mode is used, please set to 8MHz or more peripheral bus clock.

*5: The noise filter time can be changed by register settings.

Change the number of the noise filter steps according to APB bus clock frequency.


tCYCSD
GE_SDCLK
tAOSD
GE_SDA[11:0]
Address
tBAOSD
GE_SDBA[1:0]
Address
tWROSD
GE_SDDQM[3:0]
tSCSSD
GE_SDCSX
tRASSD
GE_SDRASX
tCASSD
GE_SDCASX
tSWESD
GE_SDWEX
tCKESD
GE_SDCKE
tDSSD
tDHSD
GE_SDRASX
RD
tDOSD
tDOZSD
GE_SDRASX
WD


GE_SPCSX0
tSCYCM
mode0
mode2
GE_SPCK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
GE_SPDQ0,
GE_SPDQ1,
GE_SPDQ2,
GE_SPDQ3
input
tDSSET
tSDHOLD
output
tOSDAT