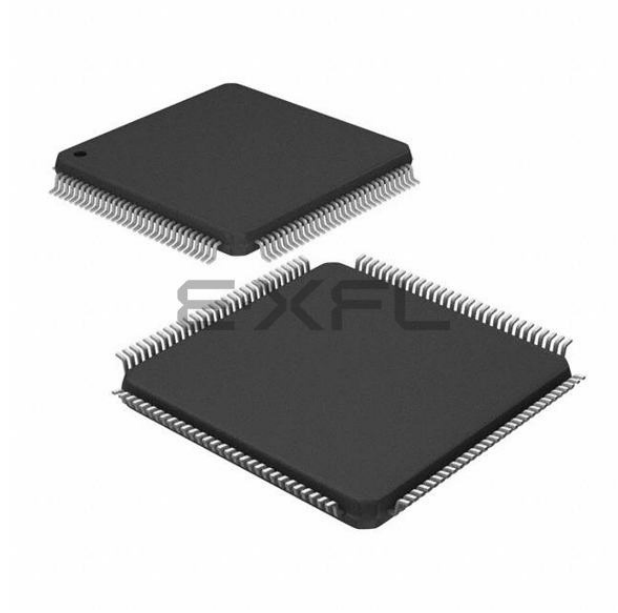

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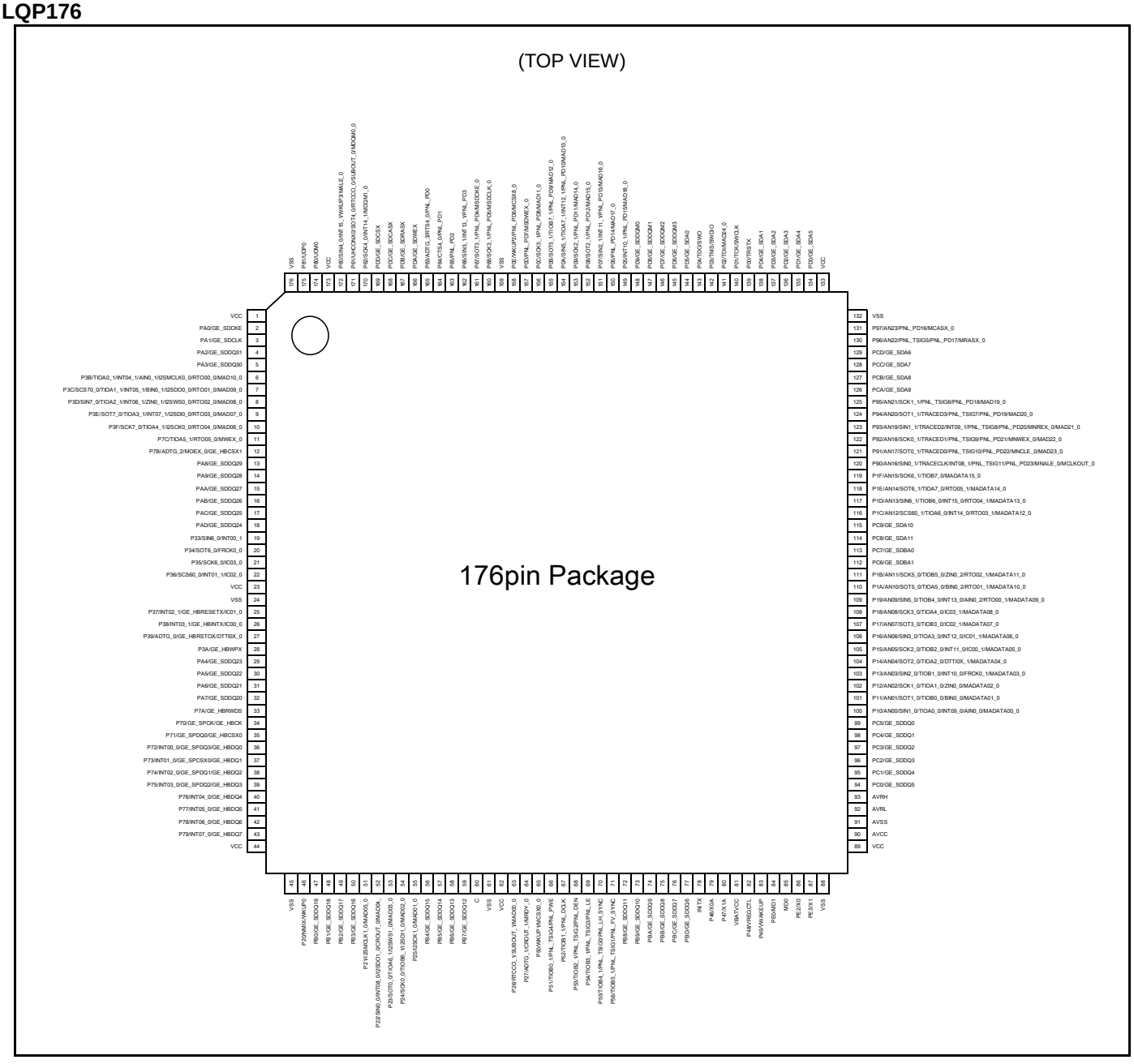
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2d35gjamv20000

LQP176



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161			
113	–	–	–	PC7	K	I
				GE_SDBA0		
114	–	–	–	PC8	K	I
				GE_SDA11		
115	–	–	–	PC9	K	I
				GE_SDA10		
116	78	78	F12	P1C	F	M
				AN12		
				SCS60_1		
				TIOA6_0		
				INT14_0		
				RTO03_1 (PPG02_1)		
				MADATA12_0		
117	79	79	F13	P1D	F	M
				AN13		
				SIN6_1		
				TIOB6_0		
				INT15_0		
				RTO04_1 (PPG04_1)		
				MADATA13_0		
118	80	80	E10	P1E	F	L
				AN14		
				SOT6_1 (SDA6_1)		
				TIOA7_0		
				RTO05_1 (PPG04_1)		
				MADATA14_0		
119	81	81	E11	P1F	F	L
				AN15		
				SCK6_1 (SCL6_1)		
				TIOB7_0		
				MADATA15_0		

Signal Description

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
ADC	ADTG_0	A/D converter external trigger input pin	27	17	17	F1
	ADTG_1		64	42	42	N5
	ADTG_2		12	8	8	E4
	ADTG_3		165	113	113	C4
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	100	66	66	K11
	AN01		101	67	67	J11
	AN02		102	68	68	H10
	AN03		103	69	69	H11
	AN04		104	70	70	H12
	AN05		105	71	71	H13
	AN06		106	72	72	G10
	AN07		107	73	73	G11
	AN08		108	74	74	G12
	AN09		109	75	75	G13
	AN10		110	76	76	F10
	AN11		111	77	77	F11
	AN12		116	78	78	F12
	AN13		117	79	79	F13
	AN14		118	80	80	E10
	AN15		119	81	81	E11
	AN16		120	82	82	E12
	AN17		121	83	83	E13
	AN18		122	84	84	D10
	AN19		123	85	85	D11
	AN20		124	86	86	D12
	AN21		125	87	87	D13
	AN22		130	88	88	C12
	AN23		131	89	89	C13
Base Timer 0	TIOA0_0	Base Timer ch.0 TIOA Pin	100	66	66	K11
	TIOA0_1		6	2	2	C3
	TIOB0_0	Base Timer ch.0 TIOB Pin	101	67	67	J11
	TIOB0_1		66	44	44	L7
Base Timer 1	TIOA1_0	Base Timer ch.1 TIOA Pin	102	68	68	H10
	TIOA1_1		7	3	3	C2
	TIOB1_0	Base Timer ch.1 TIOB Pin	103	69	69	H11
	TIOB1_1		67	45	45	K8

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D35GJA)	FBGA161
Multi-function Timer 0	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	10	6	6	D1
	RTO04_1 (PPG04_1)		117	79	79	F13
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	11	7	7	D4
	RTO05_1 (PPG04_1)		118	80	80	E10
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	100	66	66	K11
	AIN0_1		6	2	2	C3
	AIN0_2		109	75	75	G13
	BIN0_0	QPRC ch.0 BIN input pin	101	67	67	J11
	BIN0_1		7	3	3	C2
	BIN0_2		110	76	76	F10
	ZIN0_0	QPRC ch.0 ZIN input pin	102	68	68	H10
	ZIN0_1		8	4	4	D3
	ZIN0_2		111	77	77	F11
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	171	115	115	B3
	RTCCO_1		63	41	41	M5
	SUBOUT_0	Sub clock output pin	171	115	115	B3
	SUBOUT_1		63	41	41	M5
USB0	UDM0	USB ch.0 device/host D – pin	174	118	118	A3
	UDP0	USB ch.0 device/host D + pin	175	119	119	A2
	UHCONX0	USB ch.0 external pull-up control pin	171	115	115	B3
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	46	32	32	M2
	WKUP1	Deep standby mode return signal input pin 1	65	43	43	K7
	WKUP2	Deep standby mode return signal input pin 2	158	106	106	B7
	WKUP3	Deep standby mode return signal input pin 3	172	116	116	B2
VBAT	VREGCTL	On-board regulator control pin	82	54	54	L11
	VWAKEUP	The return signal input pin from a hibernation state	83	55	55	L12

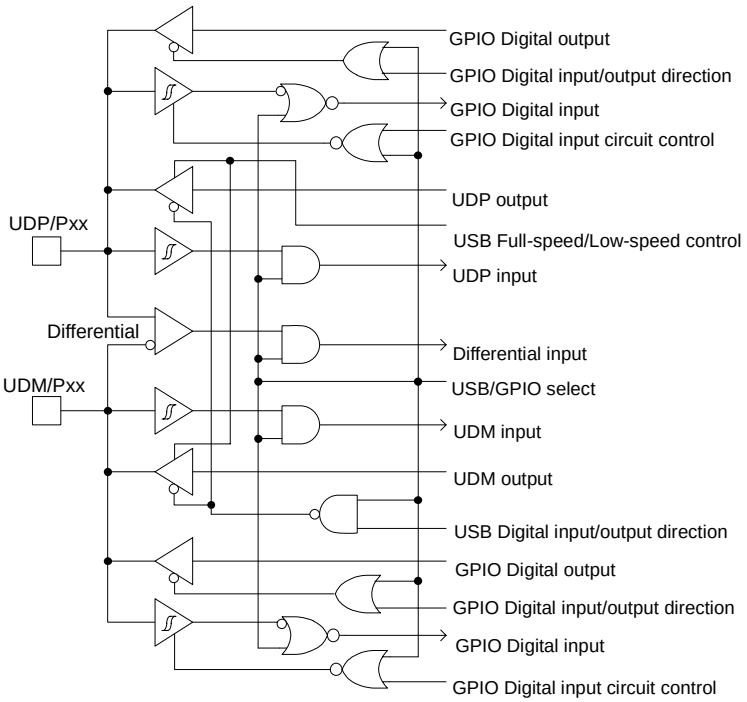
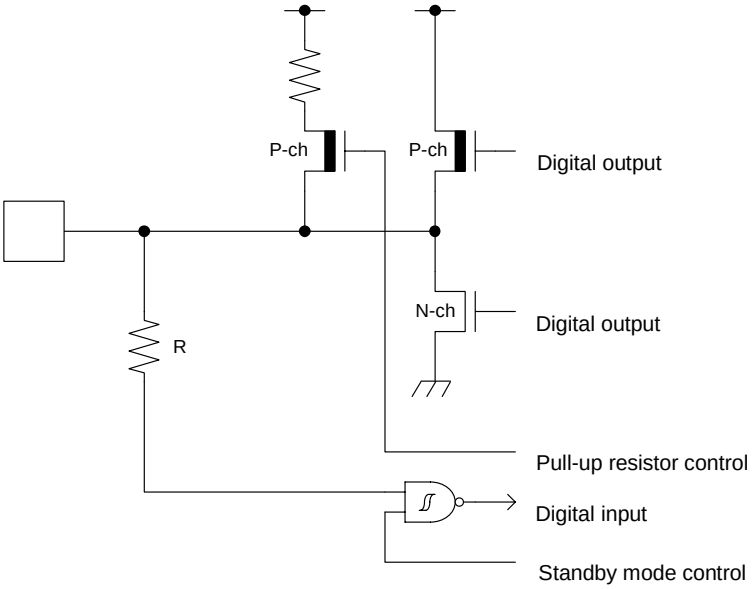
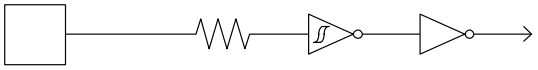
Type	Circuit	Remarks
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control ・I_{OH} = -20.5 mA, I_{OL} = 18.5 mA
I		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・Available to control of PZR registers.
J		・CMOS level hysteresis input

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7,*8 (PLL)	*5	160 MHz	185	285	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	179	276	mA	
					120 MHz	169	261	mA	
					100 MHz	161	250	mA	
					80 MHz	154	239	mA	
					60 MHz	146	227	mA	
					40 MHz	138	215	mA	
					20 MHz	130	204	mA	
					8 MHz	125	196	mA	
					4 MHz	124	195	mA	
			Normal operation *6,*7,*8 (PLL)	*5	160 MHz	45	122	mA	*3 When all peripheral clocks are OFF
					144 MHz	41	117	mA	
					120 MHz	36	111	mA	
					100 MHz	31	105	mA	
					80 MHz	26	99	mA	
					60 MHz	22	94	mA	
					40 MHz	17	89	mA	
					20 MHz	12	83	mA	
					8 MHz	10	80	mA	
					4 MHz	9	79	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*5: When not operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

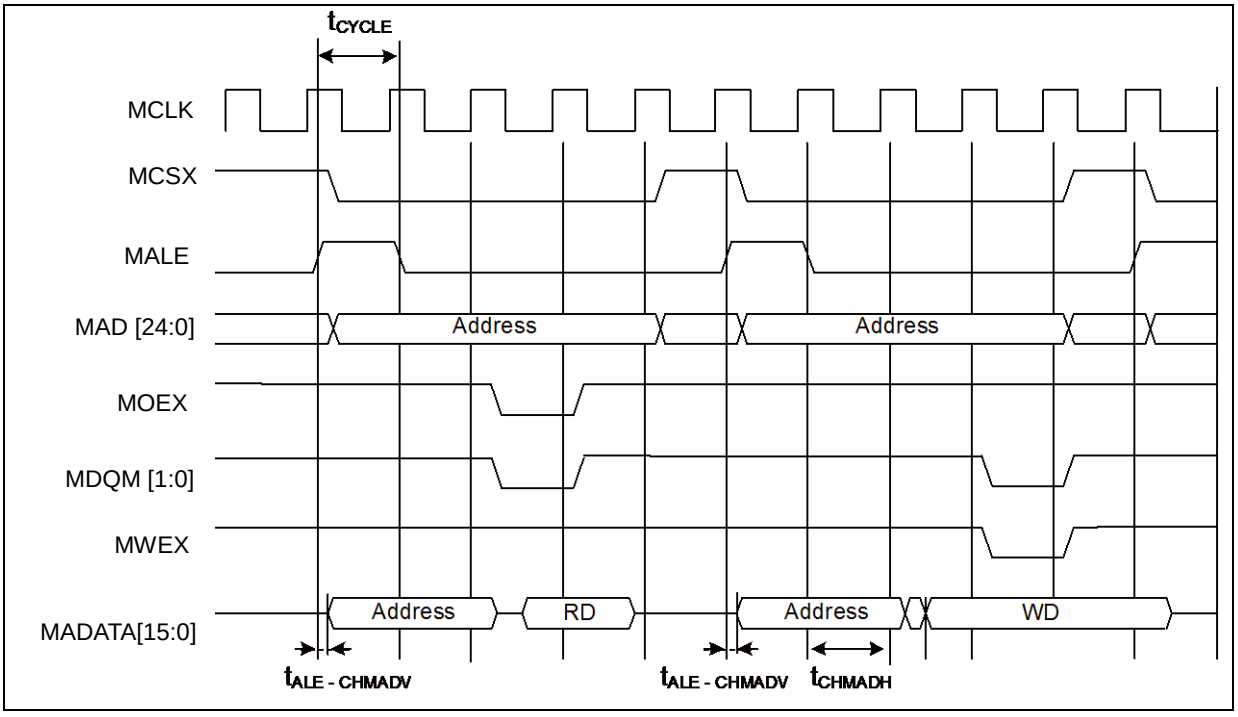
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24:0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*



SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCSD}	MSDCLK	-	-	50	MHz	
Address delay time	t_{AOSD}	MSDCLK, MAD[15:0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t_{DOSD}	MSDCLK, MADATA[15:0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[15:0]	-	2	19.5	ns	
MDQM[1:0] delay time	t_{WROSD}	MSDCLK, MDQM[1:0]	-	1	12	ns	
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	-	2	12	ns	
Data setup time	t_{DSSD}	MSDCLK, MADATA[15:0]	-	19	-	ns	
Data hold time	t_{DHSD}	MSDCLK, MADATA[15:0]	-	0	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF*

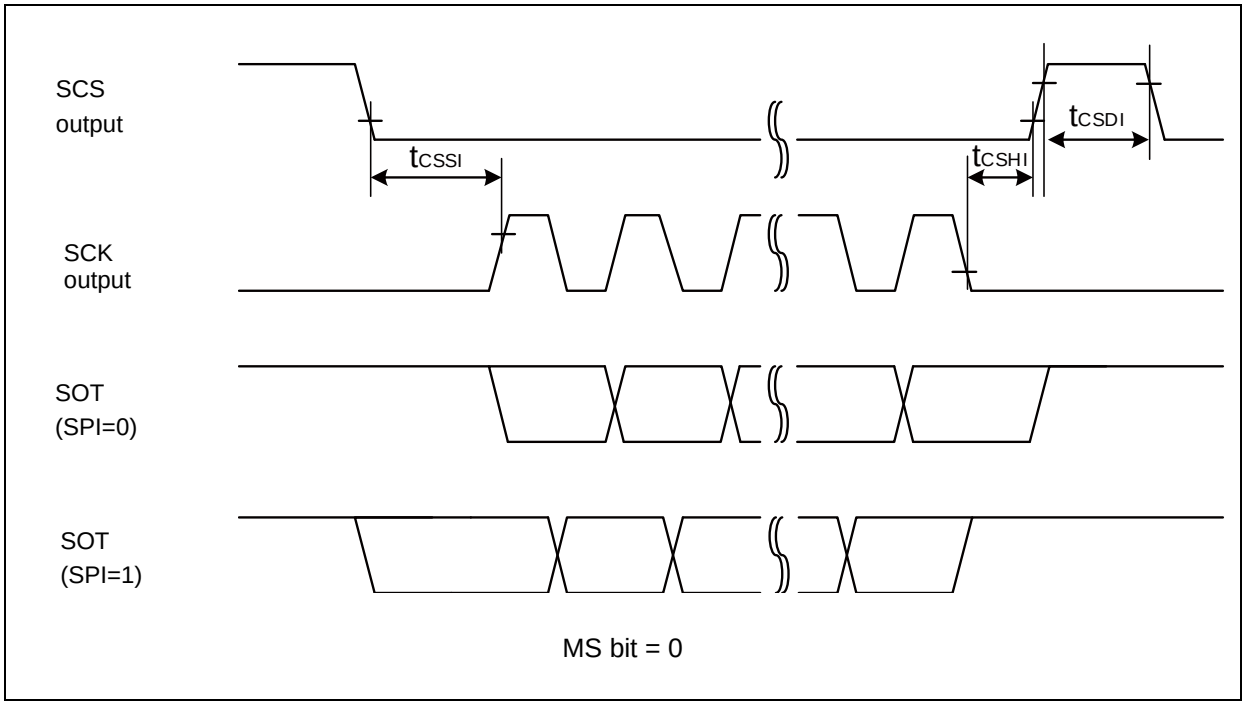
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

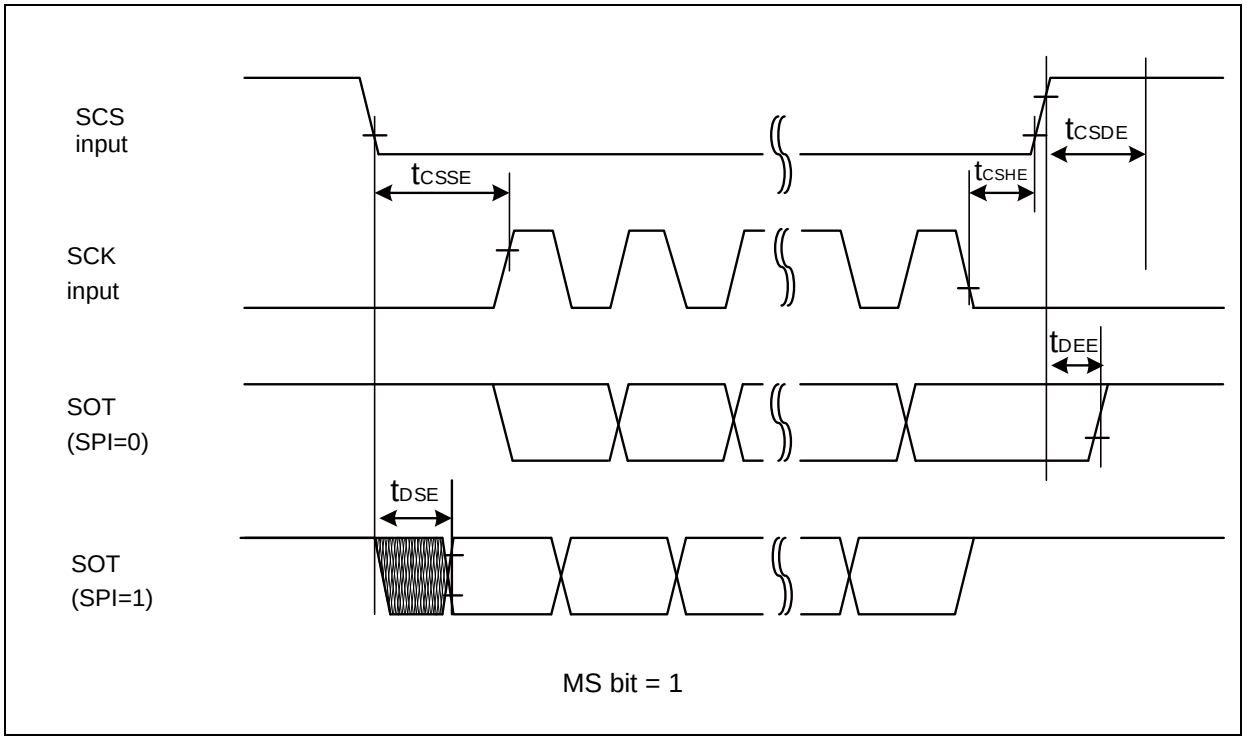
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

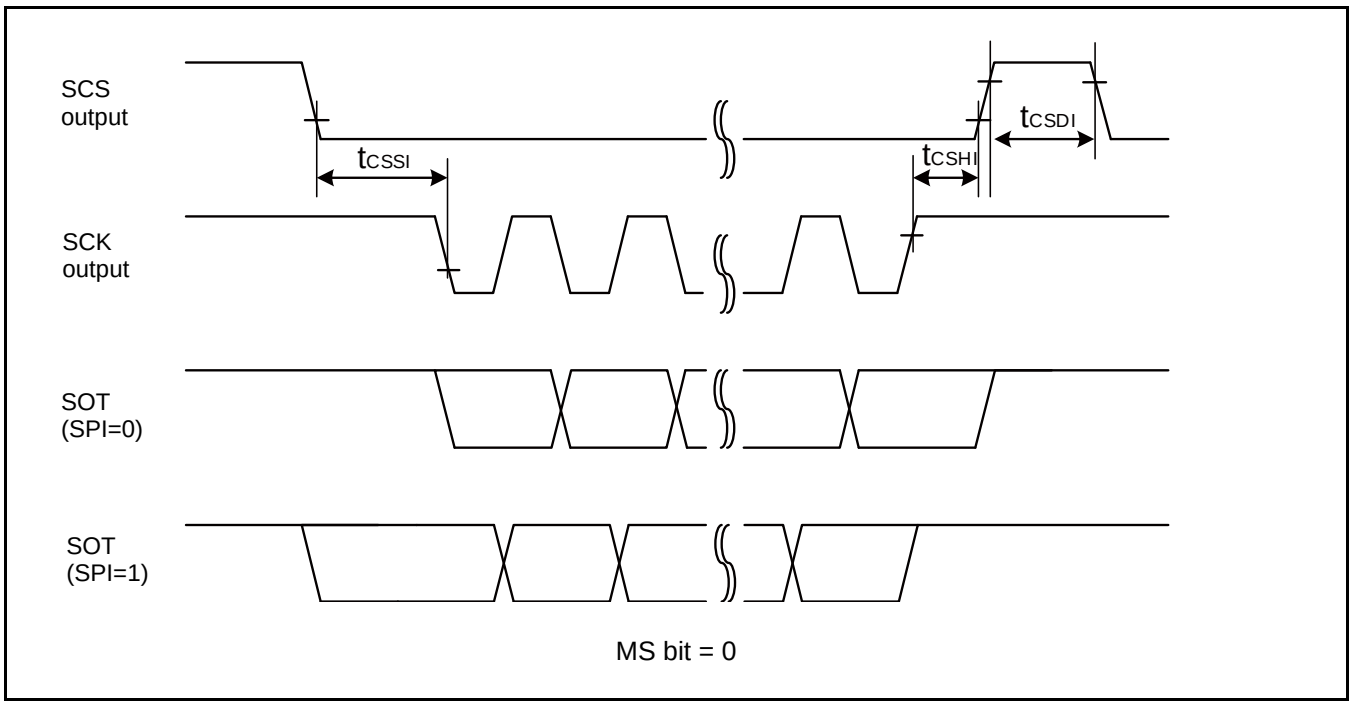
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



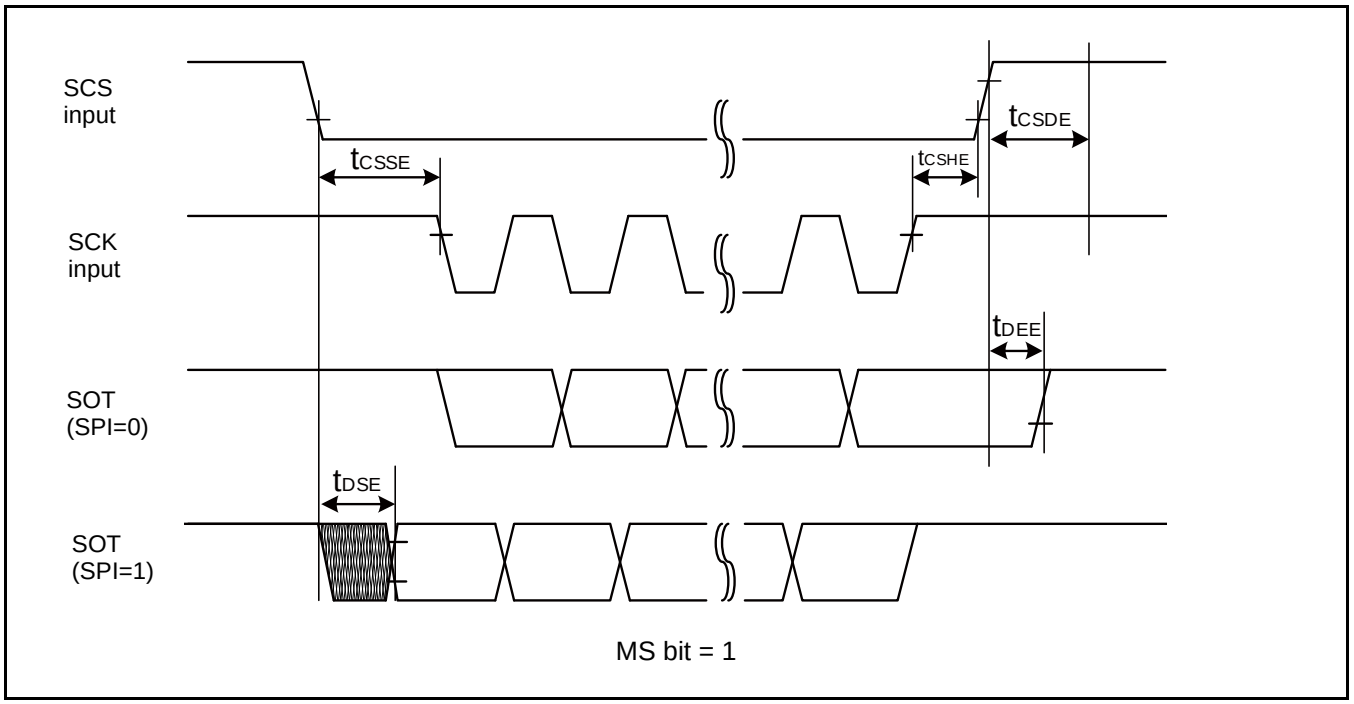
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

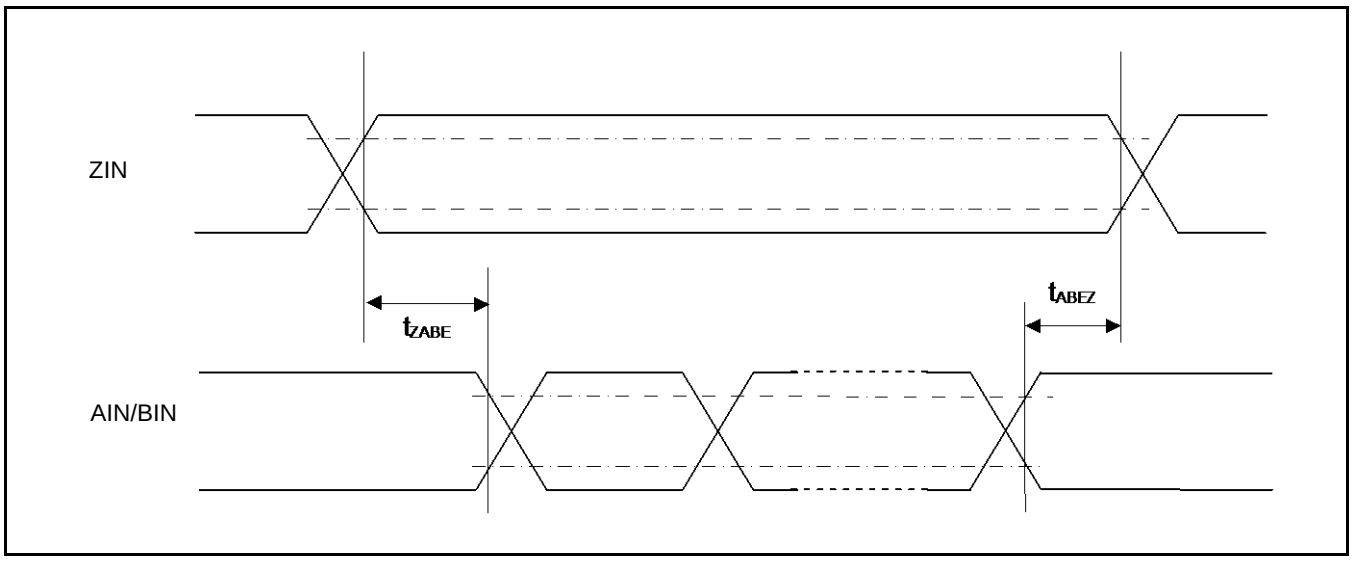
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


ZIN
AIN/BIN
tZABE
tABEZ

12.4.15 I²C Timing

Standard Mode, Fast Mode

(V_{CC} = 2.7V to 3.6, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I²C bus device can be used on a Standard mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.

About the APB bus number that I²C is connected to, see 8. Block Diagram in this data sheet.

When the standard mode is used, please set to 2 MHz or more peripheral bus clock.

When fast mode is used, please set to 8MHz or more peripheral bus clock.

*5: The noise filter time can be changed by register settings.

Change the number of the noise filter steps according to APB bus clock frequency.

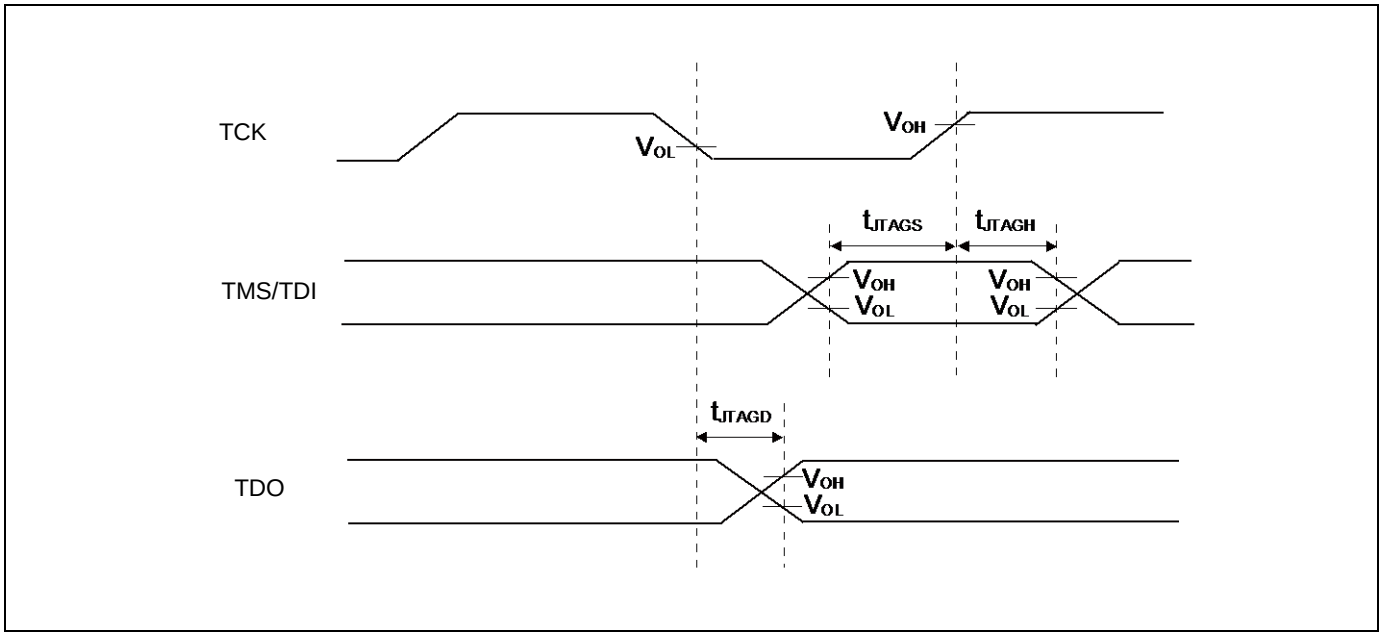
12.4.17 JTAG Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	-	15	-	ns	
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	-	15	-	ns	
TDO delay time	t_{JTAGD}	TCK, TDO	-	-	45	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*



12.4.18 I²S Timing

Master Mode Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rising time	t_{RI}	I2SDI	-	-	5	ns	
Input signal falling time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS=48 kHz, I2MCLK=256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details.

12.4.19 GDC:Panel Output Timing

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	$t_{CYCPNGE}$	PNL_DCLK	-	-	40	MHz
PNL_DCLK↓→PNL_PD[23:0] Output delay time	$t_{PDOPDGE}$	PNL_PD[23:0]	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_LH_SYNC Output delay time	$t_{HDOPDGE}$	PNL_LH_SYNC	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_FV_SYNC Output delay time	$t_{VDOPDGE}$	PNL_FV_SYNC	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_LE Output delay time	$t_{LDOPDGE}$	PNL_LE	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_DEN Output delay time	$t_{DDOPDGE}$	PNL_DEN	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_PWE Output delay time	$t_{PDOPDGE}$	PNL_PWE		-4.5	4.5	ns

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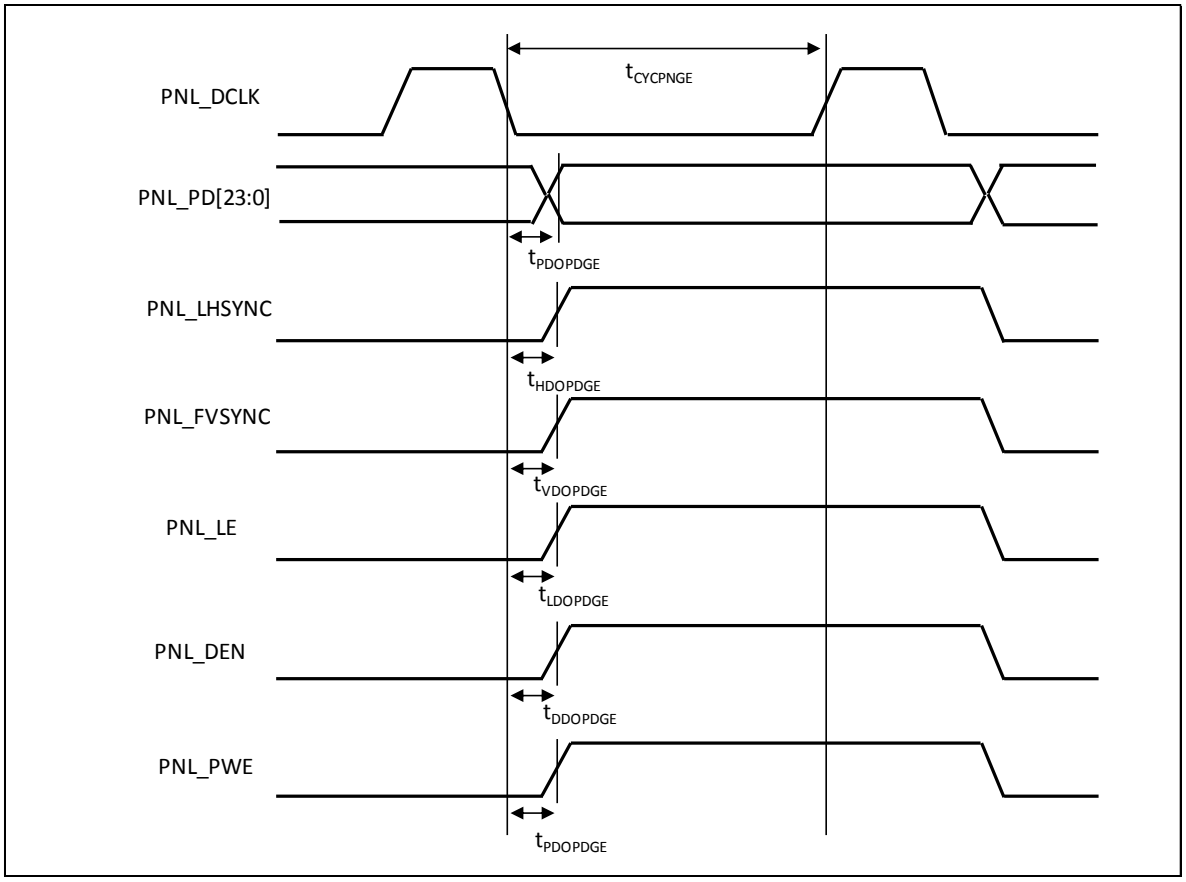


12.6 USB Characteristics

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-up resistance = 15kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 15kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

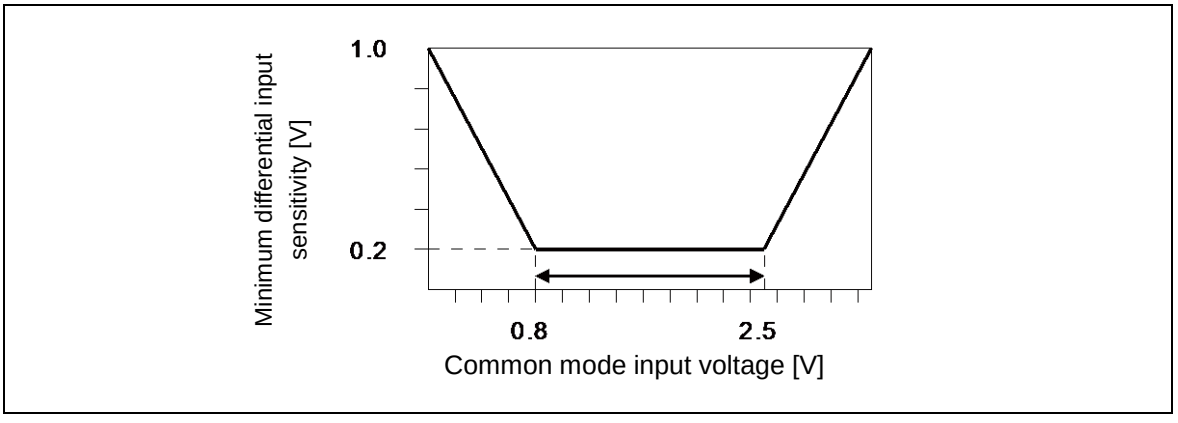
*1: The switching threshold voltage of Single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

There are some hysteresis to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.

Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.



*3: The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the V_{SS} and 15 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	6.6	31	s	Includes write time prior to internal erase

Write Cycles and Data Hold Time

Erase/Write Cycles (cycle)	Data Hold Time (year)
1,000	20*
10,000	10*
100,000	5*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.9 VFLASH Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4 KB)	-	50	450	ms	
Block Erase Time (64 KB)	-	500	2000	ms	
Page Program Time	-	0.7	3	ms	
Chip erase time	-	11.2	64	s	

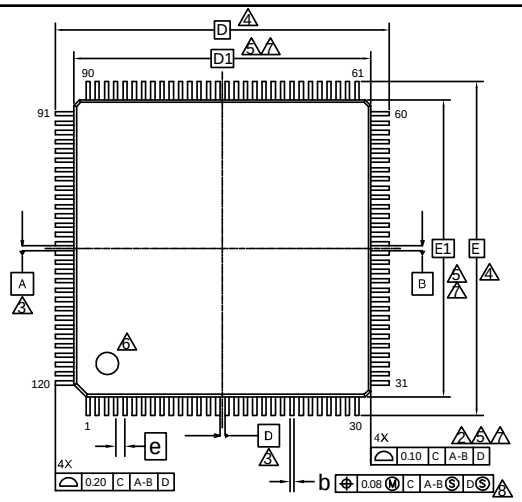
Erase Endurance

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Erase per sector	100k	-	-	cycle	

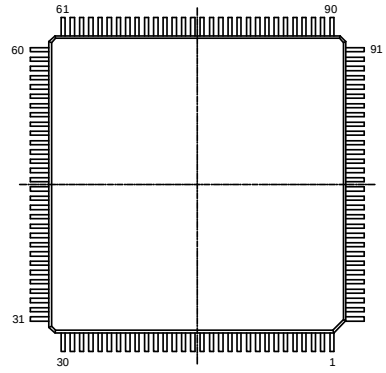
*: Data retention of 20 years is based on 1k erase cycle or less.

14. Package Dimensions

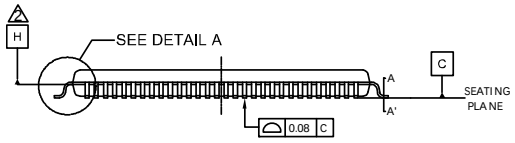
Package Type	Package Code
LQFP 120	LQM 120



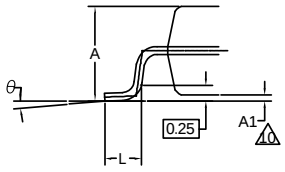
TOP VIEW



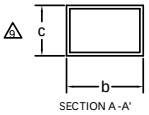
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**