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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0408psc1866

GENERAL DESCRIPTION (Continued)

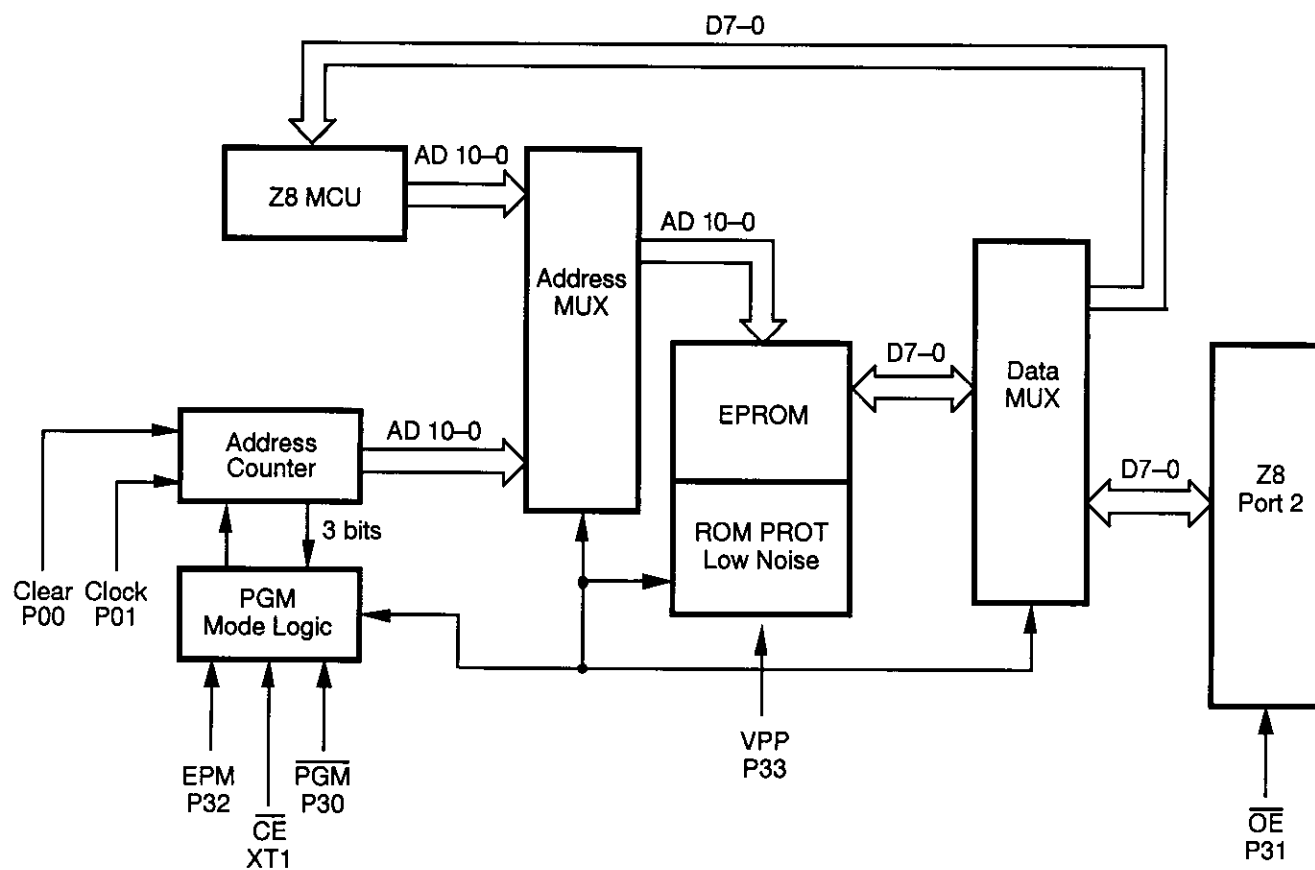


Figure 2. EPROM Programming Mode Block Diagram

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

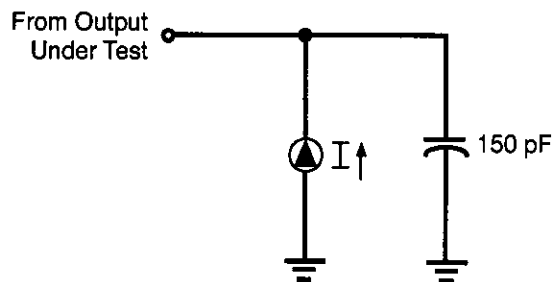


Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V _{CC} [4]	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz	7
I _{CC2}	Standby Current	4.5V		10.0	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7,8
		5.5V		10.0	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7,8
I _{ALL}	Auto Latch Low Current	4.5V		32.0	16	μA	0V < V _{IN} < V _{CC}	
		5.5V		32.0	16	μA	0V < V _{IN} < V _{CC}	
I _{ALH}	Auto Latch High Current	4.5V		-16.0	-8.0	μA	0V < V _{IN} < V _{CC}	
		5.5V		-16.0	-8.0	μA	0V < V _{IN} < V _{CC}	

Notes:

- Port 2 and Port 0 only
- V_{SS} = 0V = GND
- The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
- V_{CC} = 4.5 to 5.5V, typical values measured at V_{CC} = 5.0V.
The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V_{CC} = 5.0V.
- Standard Mode (not Low EMI Mode)
- Z86E08 only
- All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
- If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I _{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
I _{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

Standard Temperature

15		$T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$							
No	Symbol	Parameter	V_{CC}	8 MHz		12 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

Extended Temperature

T _A = -40 °C to +105 °C									
				8 MHz		12 MHz			
No	Symbol	Parameter	V _{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1
11	Tpor	Power-On Reset Time	4.5V	12	100	12	100	ms	1
			5.5V	12	100	12	100	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

No	Symbol	Parameter	V _{CC}	T _A = −40 °C to +105 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V	25		25		ns	1
			5.5V	25		25		ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V	100		100		ns	1
			5.5V	100		100		ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

\overline{CE} Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

\overline{OE} Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear Clear (active High). This pin resets the internal address counter at the High Level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one with one clock cycle.

PGM Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V_{PP}, \overline{CE} , EPM, \overline{OE} pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

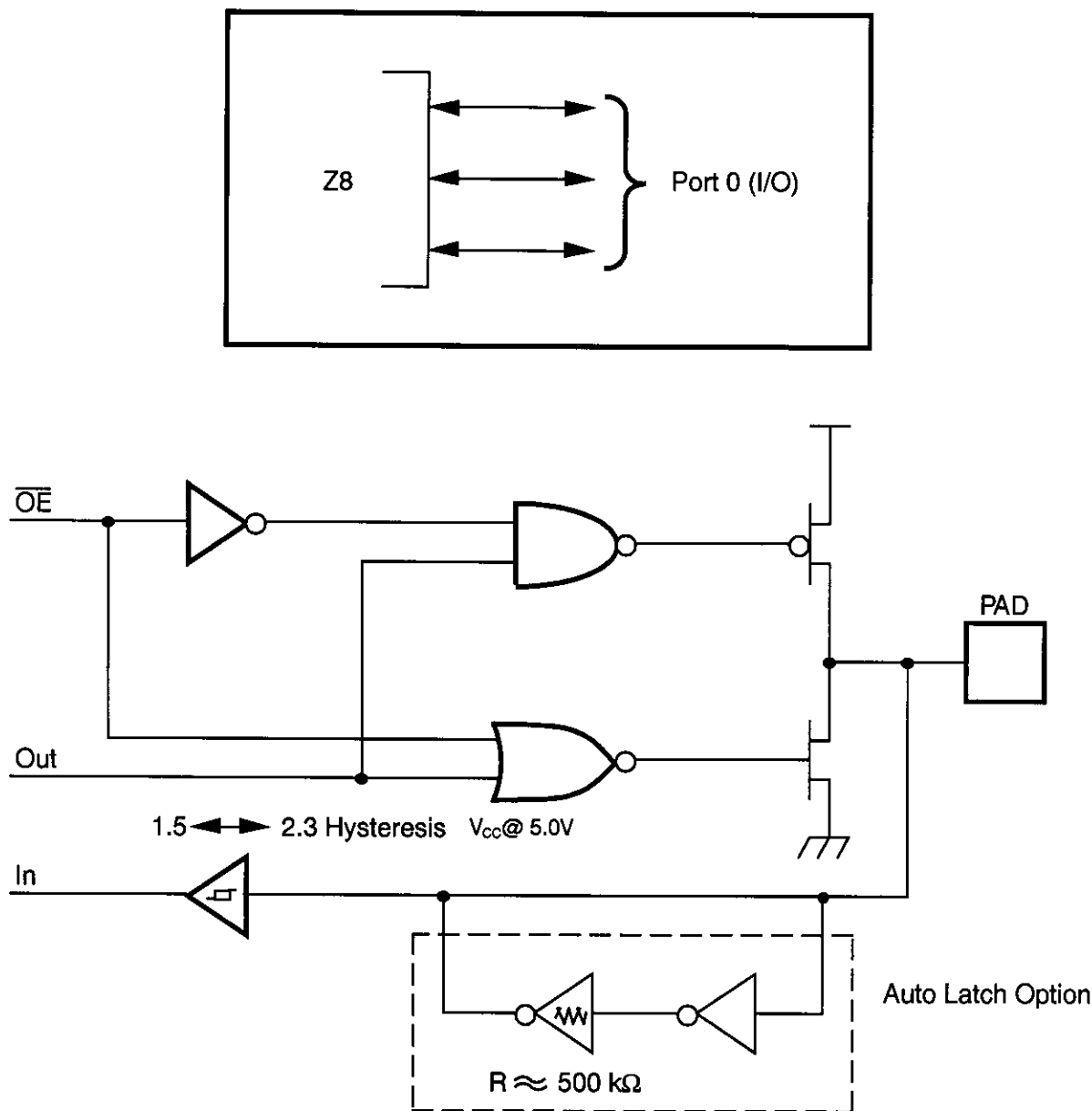


Figure 7. Port 0 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

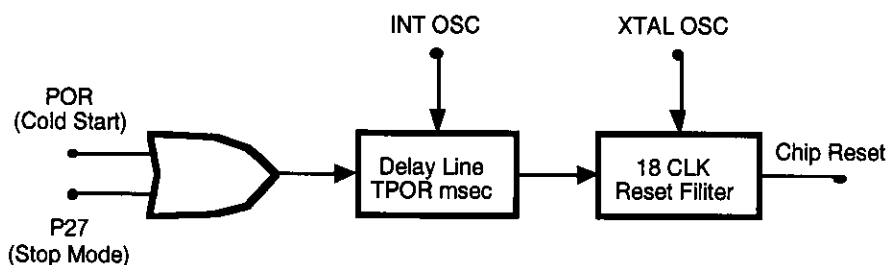


Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

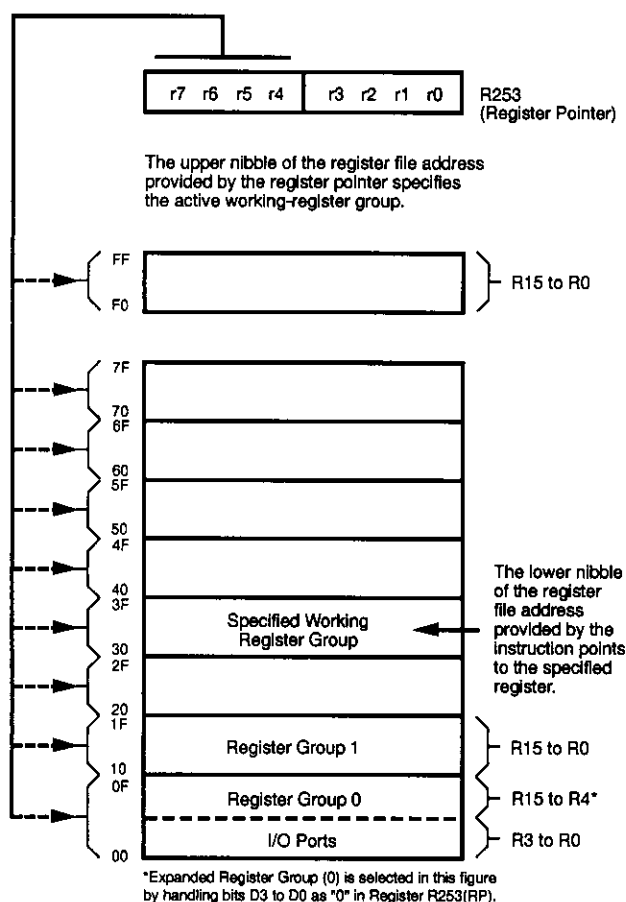


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
 $V_{CC} = 5.0V @ 25^{\circ}C$

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 μ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
 $V_{CC} = 3.3V @ 25^{\circ}C$

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 μ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

FUNCTIONAL DESCRIPTION (Continued)

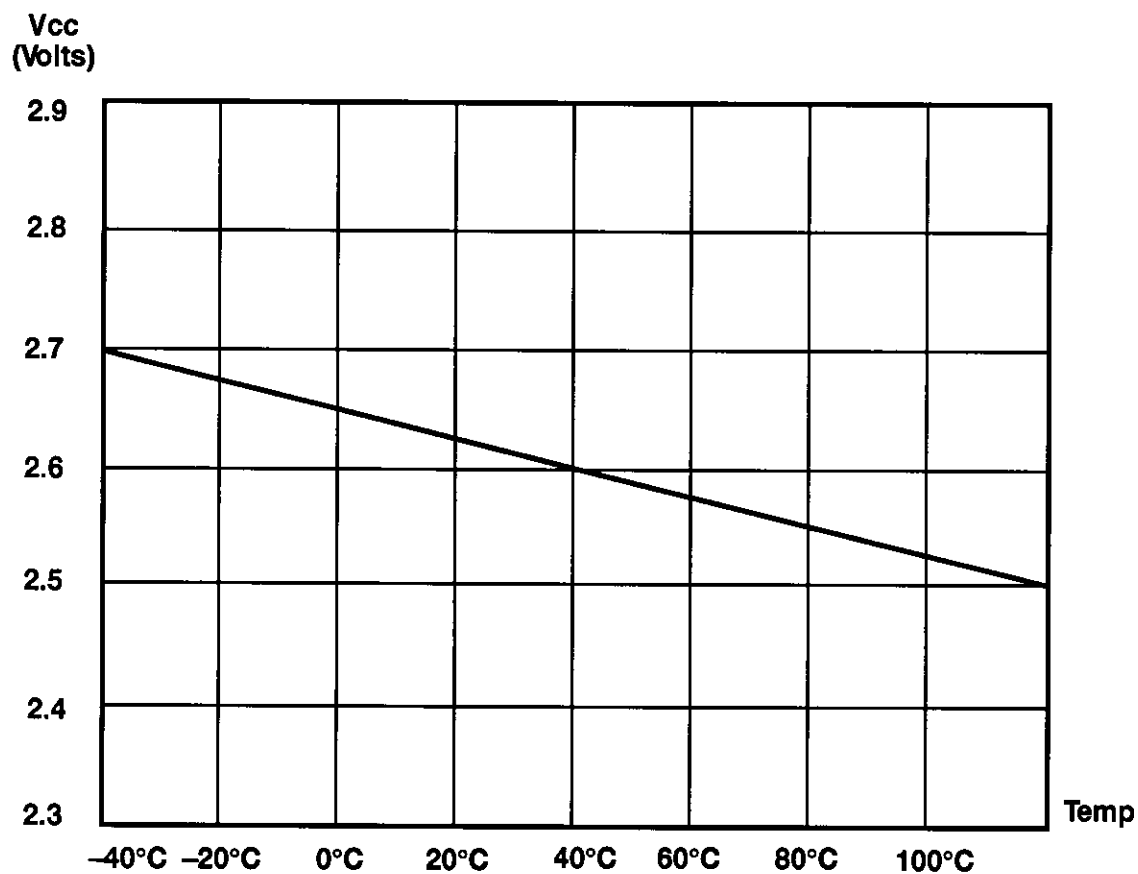
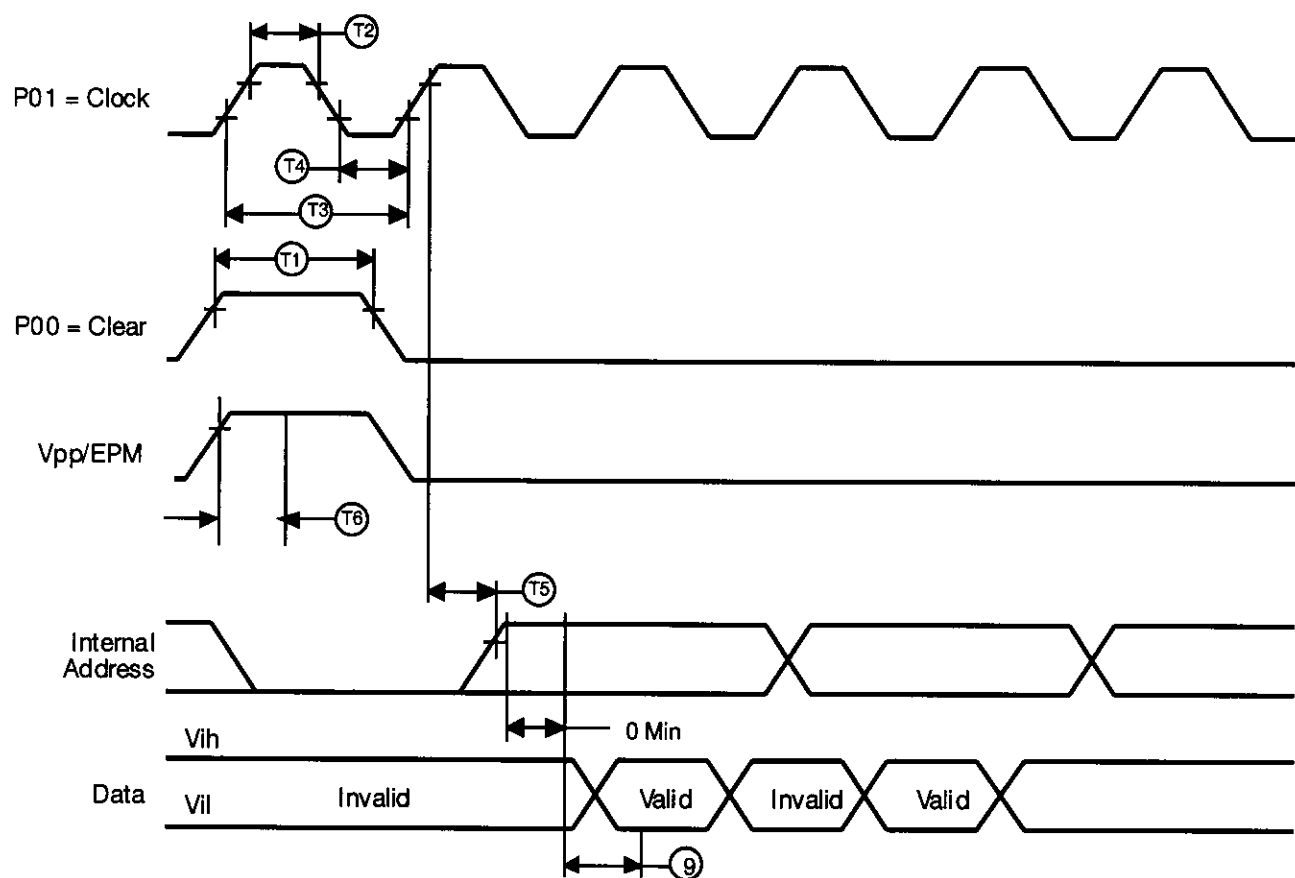


Figure 17. Typical Auto Reset Voltage
(V_{LV}) vs. Temperature



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 μ s Min

Figure 18. Z86E04/E08 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

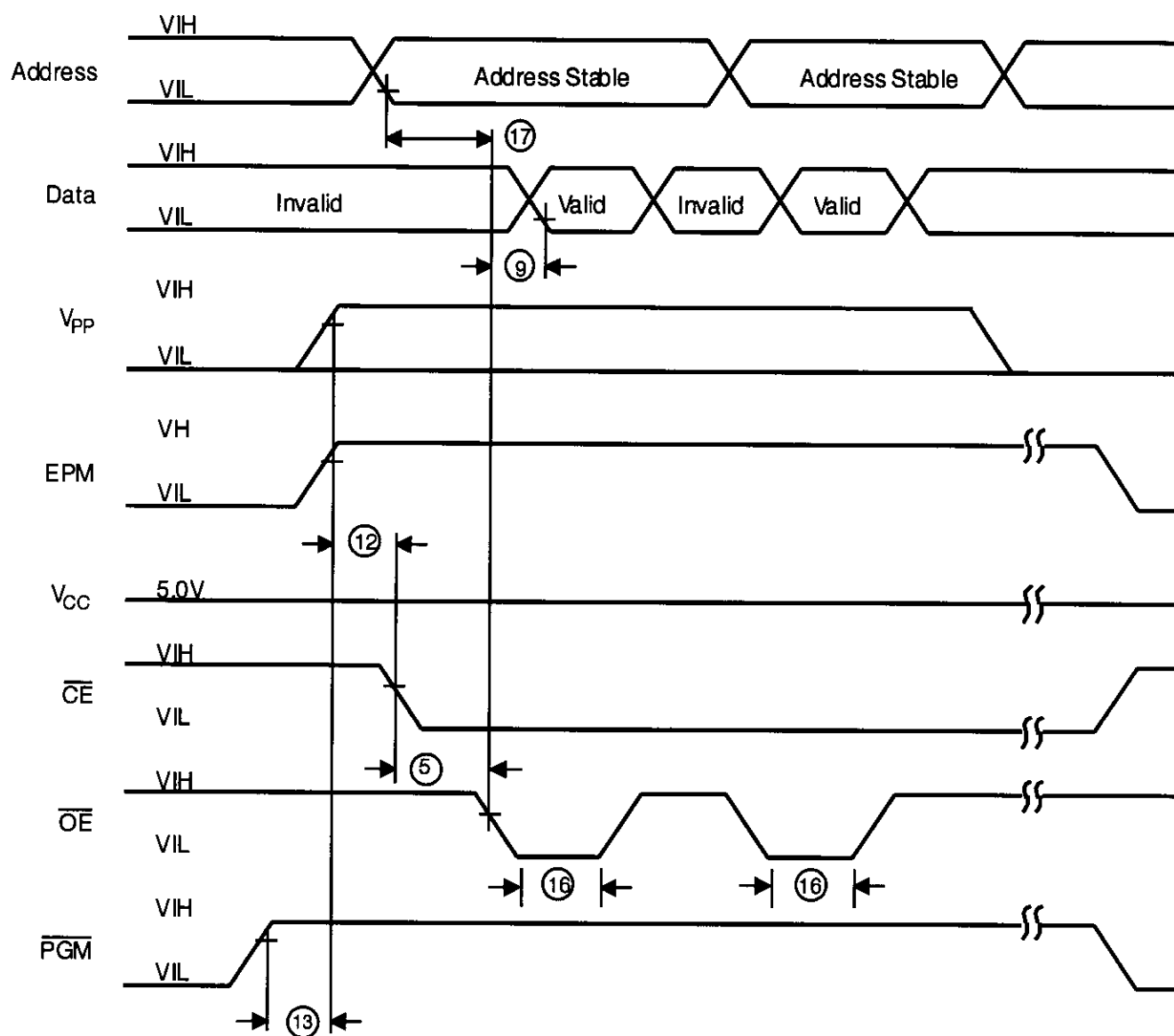


Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)

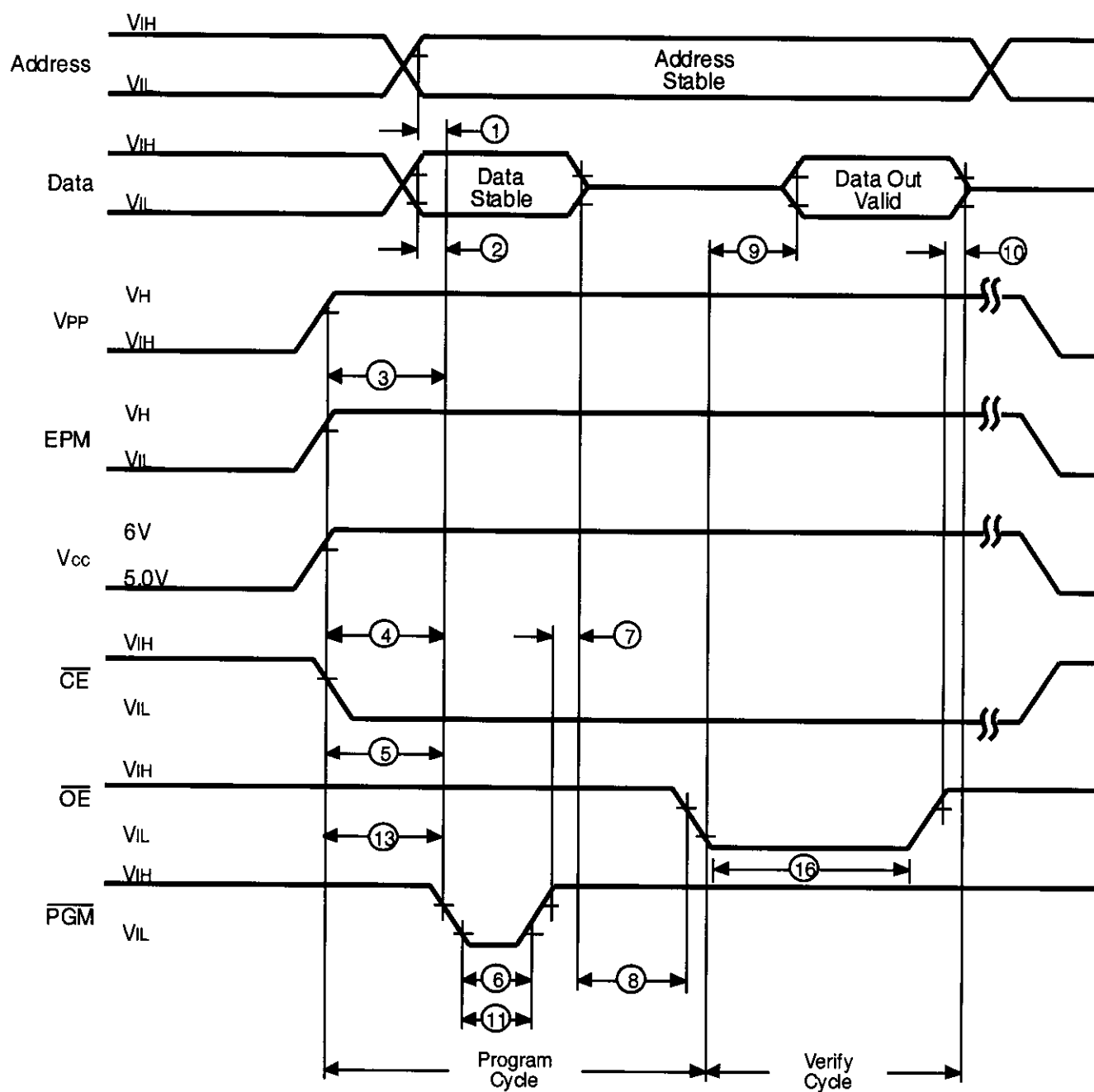
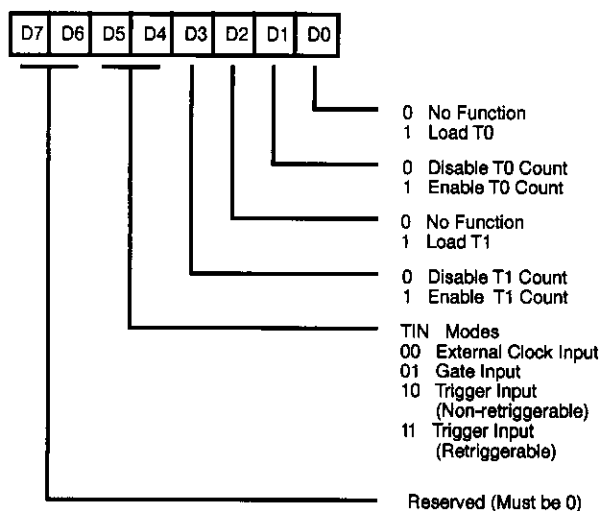


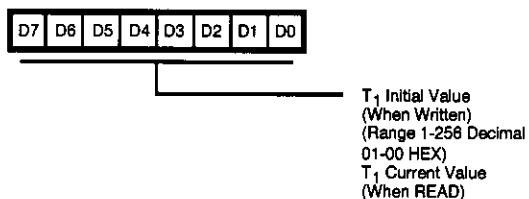
Figure 20. Z86E04/E08 Programming Waveform
(Program and Verify)

Z8 CONTROL REGISTERS

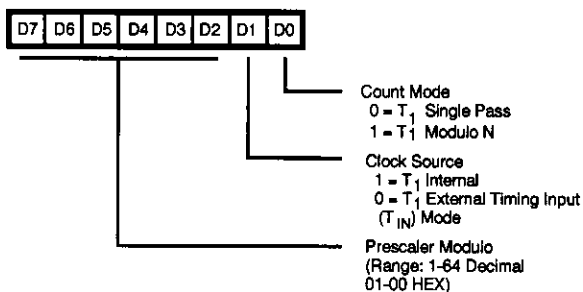
R241 TMR

Figure 24. Timer Mode Register (F1_H: Read/Write)

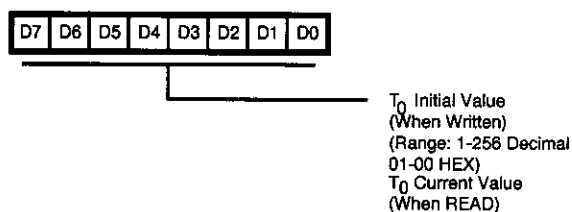
R242 T1

Figure 25. Counter Timer 1 Register (F2_H: Read/Write)

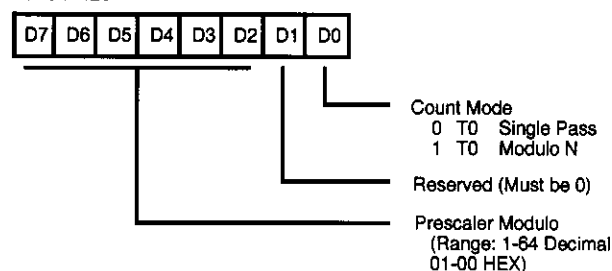
R243 PRE1

Figure 26. Prescaler 1 Register (F3_H: Write Only)

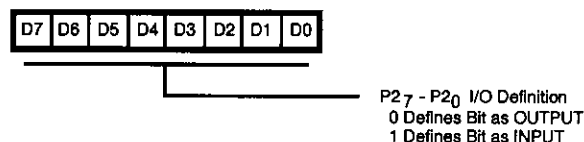
R244 T0

Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

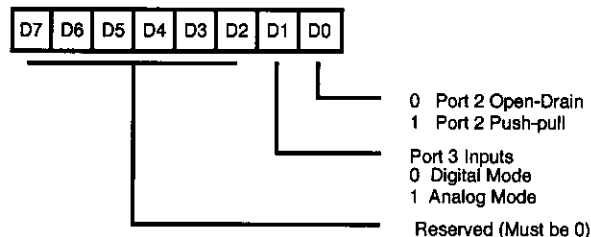
R245 PRE0

Figure 28. Prescaler 0 Register (F5_H: Write Only)

R246 P2M

Figure 29. Port 2 Mode Register (F6_H: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7_H: Write Only)

Z8 CONTROL REGISTERS (Continued)

R248 P01M

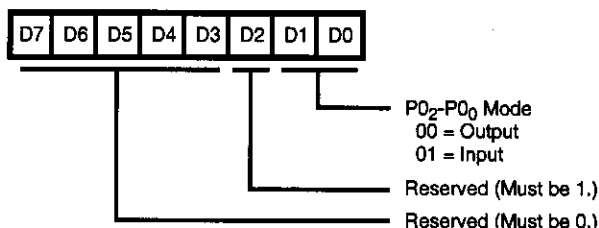


Figure 31. Port 0 and 1 Mode Register
(F8_H: Write Only)

R249 IPR

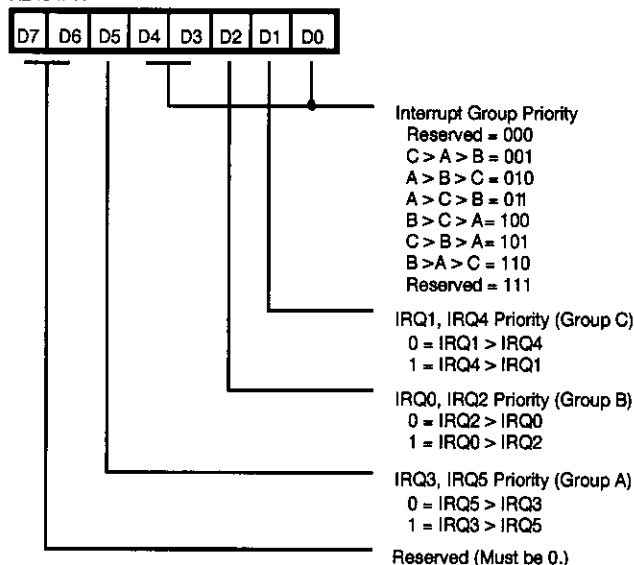


Figure 32. Interrupt Priority Register
(F9_H: Write Only)

R250 IRQ

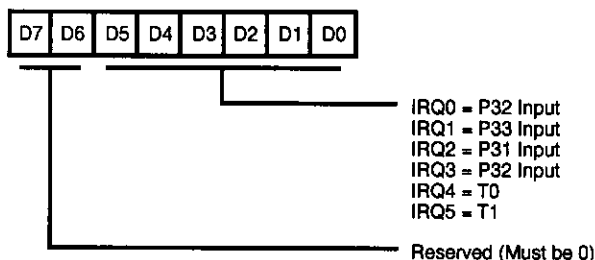


Figure 33. Interrupt Request Register
(FA_H: Read/Write)

R251 IMR

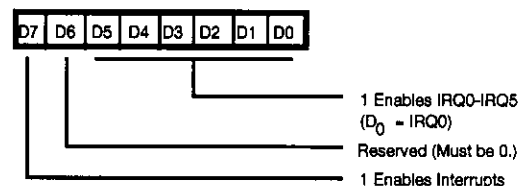


Figure 34. Interrupt Mask Register
(FB_H: Read/Write)

R252 Flags

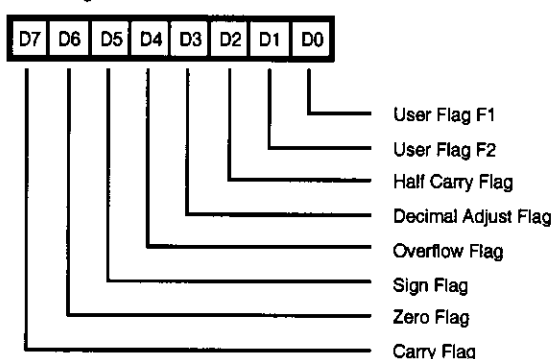


Figure 35. Flag Register
(FC_H: Read/Write)

R253 RP

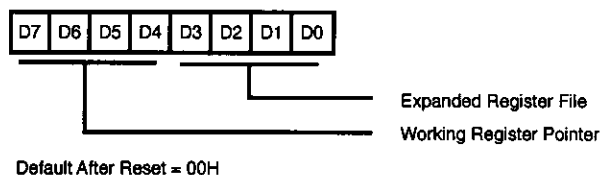


Figure 36. Register Pointer
(FD_H: Read/Write)

R255 SPL

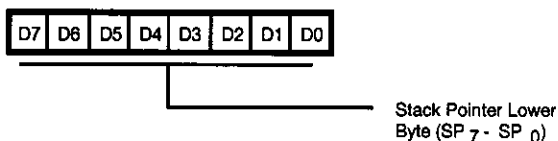
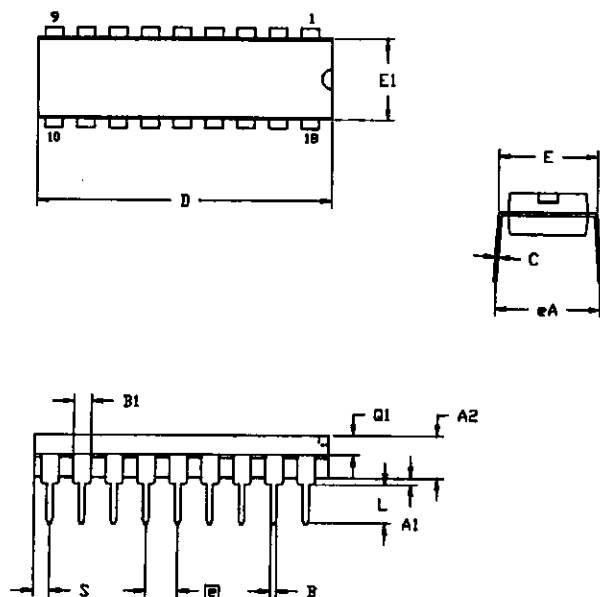


Figure 37. Stack Pointer
(FF_H: Read/Write)

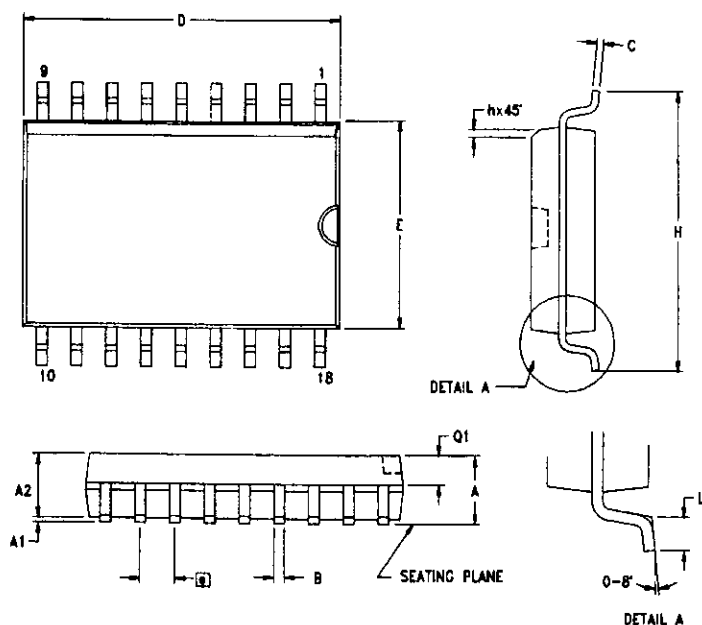
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be

found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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