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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z86e0412hec1903">https://www.e-xfl.com/product-detail/zilog/z86e0412hec1903</a>

## FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1 $\mu$ s @ 12 MHz)
- RAM Bytes (125)

## GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8<sup>®</sup> MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

**Note:** All Signals with an overline, " $\overline{\phantom{x}}$ ", are active Low, for example:  $\overline{B/W}$  (WORD is active Low);  $\overline{B}/W$  (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

**ABSOLUTE MAXIMUM RATINGS**

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power

dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	-40	+105	C	
Storage Temperature	-65	+150	C	
Voltage on any Pin with Respect to $V_{SS}$	-0.7	+12	V	1
Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$	-0.3	+7	V	
Voltage on Pins 7, 8, 9, 10 with Respect to $V_{SS}$	-0.6	$V_{DD}+1$	V	2
Total Power Dissipation		1.65	W	
Maximum Allowable Current out of $V_{SS}$		300	mA	
Maximum Allowable Current into $V_{DD}$		220	mA	
Maximum Allowable Current into an Input Pin	-600	+600	$\mu\text{A}$	3
Maximum Allowable Current into an Open-Drain Pin	-600	+600	$\mu\text{A}$	4
Maximum Allowable Output Current Sunked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Total Maximum Output Current Sunked by a Port		60	mA	
Total Maximum Output Current Sourced by a Port		45	mA	

**Notes:**

1. This applies to all pins except where otherwise noted. Maximum current into pin must be  $\pm 600 \mu\text{A}$ .
2. There is no input protection diode from pin to  $V_{DD}$  (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

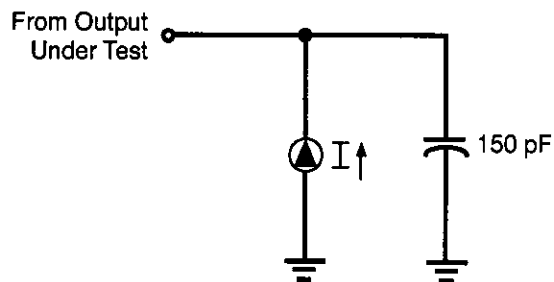


Figure 5. Test Load Diagram

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

**DC ELECTRICAL CHARACTERISTICS**

Standard Temperature

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V <sub>INMAX</sub>	Max Input Voltage	4.5V		12		V	I <sub>in</sub> < 250 μA	1
		5.5V		12		V	I <sub>in</sub> < 250 μA	1
V <sub>CH</sub>	Clock Input High Voltage	4.5V	0.8 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	4.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.7	V	Driven by External Clock Generator	
		5.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.7	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	4.5V	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V		
		5.5V	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V		
V <sub>IL</sub>	Input Low Voltage	4.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.5	V		
		5.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.5	V		
V <sub>OH</sub>	Output High Voltage	4.5V	V <sub>CC</sub> -0.4		4.8	V	I <sub>OH</sub> = -2.0 mA	5
		5.5V	V <sub>CC</sub> -0.4		4.8	V	I <sub>OH</sub> = -2.0 mA	5
		4.5V	V <sub>CC</sub> -0.4		4.8	V	Low Noise @ I <sub>OH</sub> = -0.5 mA	
		5.5V	V <sub>CC</sub> -0.4		4.8	V	Low Noise @ I <sub>OH</sub> = -0.5 mA	
V <sub>OL1</sub>	Output Low Voltage	4.5V		0.8	0.1	V	I <sub>OL</sub> = +4.0 mA	5
		5.5V		0.4	0.1	V	I <sub>OL</sub> = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I <sub>OL</sub> = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I <sub>OL</sub> = 1.0 mA	
V <sub>OL2</sub>	Output Low Voltage	4.5V		0.8	0.8	V	I <sub>OL</sub> = +12 mA,	5
		5.5V		0.8	0.8	V	I <sub>OL</sub> = +12 mA,	5
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V <sub>LV</sub>	V <sub>CC</sub> Low Voltage Auto Reset		2.2	3.0	2.8	V	@ 6 MHz Max. Int. CLK Freq.	
I <sub>IL</sub>	Input Leakage (Input Bias Current of Comparator)	4.5V	-1.0	1.0		μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V	-1.0	1.0		μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>OL</sub>	Output Leakage	4.5V	-1.0	1.0		μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V	-1.0	1.0		μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
V <sub>ICR</sub>	Comparator Input Common Mode Voltage Range		0	V <sub>CC</sub> -1.0		V		

**DC ELECTRICAL CHARACTERISTICS**

## Extended Temperature

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V <sub>INMAX</sub>	Max Input Voltage	4.5V		12.0		V	I <sub>IN</sub> < 250 μA	1
		5.5V		12.0		V	I <sub>IN</sub> < 250 μA	1
V <sub>CH</sub>	Clock Input High Voltage	4.5V	0.8 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	4.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.7	V	Driven by External Clock Generator	
		5.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.7	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	4.5V	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V		
		5.5V	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.8	V		
V <sub>IL</sub>	Input Low Voltage	4.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.5	V		
		5.5V	V <sub>SS</sub> -0.3	0.2 V <sub>CC</sub>	1.5	V		
V <sub>OH</sub>	Output High Voltage	4.5V	V <sub>CC</sub> -0.4		4.8	V	I <sub>OH</sub> = -2.0 mA	5
		5.5V	V <sub>CC</sub> -0.4		4.8	V	I <sub>OH</sub> = -2.0 mA	5
		4.5V	V <sub>CC</sub> -0.4			V	Low Noise @ I <sub>OH</sub> = -0.5 mA	
		5.5V	V <sub>CC</sub> -0.4			V	Low Noise @ I <sub>OH</sub> = -0.5 mA	
V <sub>OL1</sub>	Output Low Voltage	4.5V		0.4	0.1	V	I <sub>OL</sub> = +4.0 mA	5
		5.5V		0.4	0.1	V	I <sub>OL</sub> = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I <sub>OL</sub> = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I <sub>OL</sub> = 1.0 mA	
V <sub>OL2</sub>	Output Low Voltage	4.5V		1.0	0.3	V	I <sub>OL</sub> = +12 mA,	5
		5.5V		1.0	0.3	V	I <sub>OL</sub> = +12 mA,	5
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V <sub>LV</sub>	V <sub>CC</sub> Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I <sub>IL</sub>	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V		-1.0	1.0	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>OL</sub>	Output Leakage	4.5V		-1.0	1.0	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V		-1.0	1.0	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
V <sub>ICR</sub>	Comparator Input Common Mode Voltage Range		0	V <sub>CC</sub> -1.5		V		

## DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I <sub>CC</sub>	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I <sub>CC1</sub>	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 12 MHz	5,7
I <sub>CC</sub>	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

**AC ELECTRICAL CHARACTERISTICS**

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

Standard Temperature

15		$T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$							
No	Symbol	Parameter	$V_{CC}$	8 MHz		12 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

**Notes:**

1. Timing Reference uses 0.7  $V_{CC}$  for a logic 1 and 0.2  $V_{CC}$  for a logic 0.
2. Interrupt request through Port 3 (P33–P31).



**AC ELECTRICAL CHARACTERISTICS**

Low Noise Mode, Standard Temperature

No	Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0 °C to +70 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

**Notes:**

1. Timing Reference uses 0.7 V<sub>CC</sub> for a logic 1 and 0.2 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

## FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

**Note:** \*Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

**Program Memory.** The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

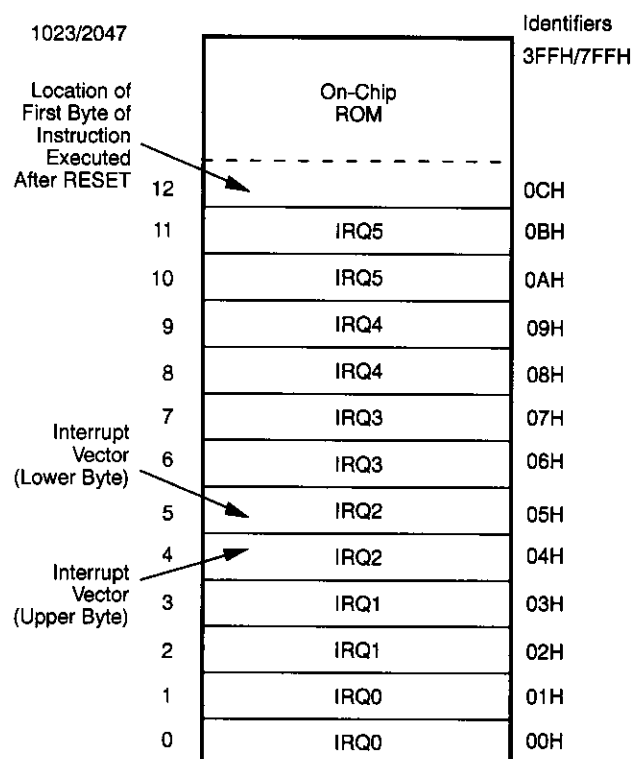


Figure 11. Program Memory Map

**Register File.** The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

Location	Identifiers
255 (FFH)	Stack Pointer (Bits 7-0) SPL
254 (FE)	General-Purpose Register GPR
253 (FD)	Register Pointer RP
252 (FC)	Program Control Flags FLAGS
251 (FB)	Interrupt Mask Register IMR
250 (FA)	Interrupt Request Register IRQ
249 (F9)	Interrupt Priority Register IPR
248 (F8)	Ports 0-1 Mode P01M
247 (F7)	Port 3 Mode P3M
246 (F6)	Port 2 Mode P2M
245 (F5)	T0 Prescaler PRE0
244 (F4)	Timer/Counter 0 T0
243 (F3)	T1 Prescaler PRE1
242 (F2)	Timer/Counter 1 T1
241 (F1H)	Timer Mode TMR
128	Not Implemented
127 (7FH)	General-Purpose Registers
4	
3	Port 3 P3
2	Port 2 P2
1	Reserved P1
0 (00H)	Port 0 P0

Figure 12. Register File

## FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

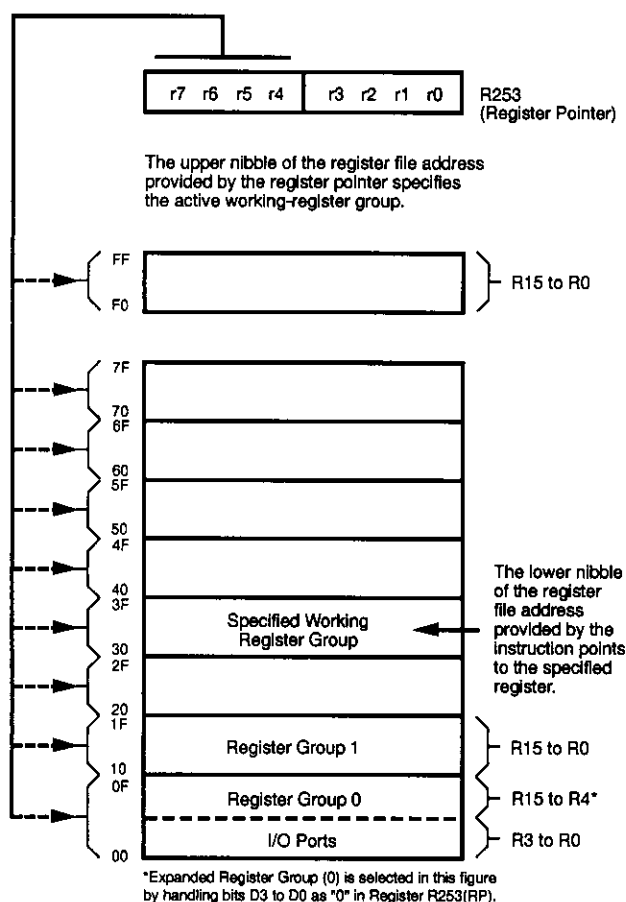


Figure 13. Register Pointer

**Stack Pointer.** The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

**General-Purpose Registers (GPR).** These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the  $V_{CC}$  voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

**Counter/Timer.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

## FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values  
 $V_{CC} = 5.0V @ 25^{\circ}C$ 

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 $\mu$ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

## Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values  
 $V_{CC} = 3.3V @ 25^{\circ}C$ 

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 $\mu$ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

## Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

**HALT Mode.** This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

**Note:** On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

**STOP Mode.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10  $\mu$ A. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

**Note:** A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

**Watch-Dog Timer (WDT).** The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

**Opcode WDT (5FH).** The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every  $T_{WDT}$ ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of  $T_{POR}$ , plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

**Opcode WDH (4FH).** When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

**Permanent WDT.** Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

**Auto Reset Voltage ( $V_{LV}$ ).** The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the  $V_{CC}$  below  $V_{LV}$ .

Figure 17 shows the Auto Reset Voltage versus temperature. If the  $V_{CC}$  drops below the VCC operating voltage range, the Z8 will function down to the  $V_{LV}$  unless the internal clock frequency is higher than the specified maximum  $V_{LV}$  frequency.

**FUNCTIONAL DESCRIPTION** (Continued)

**Internal Address Counter.** The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

**Programming Waveform.** Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 23 shows the flow chart of the Z8 programming algorithm.

**Table 8. Timing of Programming Waveforms**

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		$\mu$ s
2	Data Setup Time	2		$\mu$ s
3	V <sub>pp</sub> Setup	2		$\mu$ s
4	V <sub>cc</sub> Setup Time	2		$\mu$ s
5	Chip Enable Setup Time	2		$\mu$ s
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		$\mu$ s
8	OE Setup Time	2		$\mu$ s
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		$\mu$ s
13	PGM Setup Time	2		$\mu$ s
14	Address to OE Setup Time	2		$\mu$ s
15	Option Program Pulse Width	78		ms
16	OE Width	250		ns
17	Address Valid to OE Low	125		ns

# FUNCTIONAL DESCRIPTION (Continued)

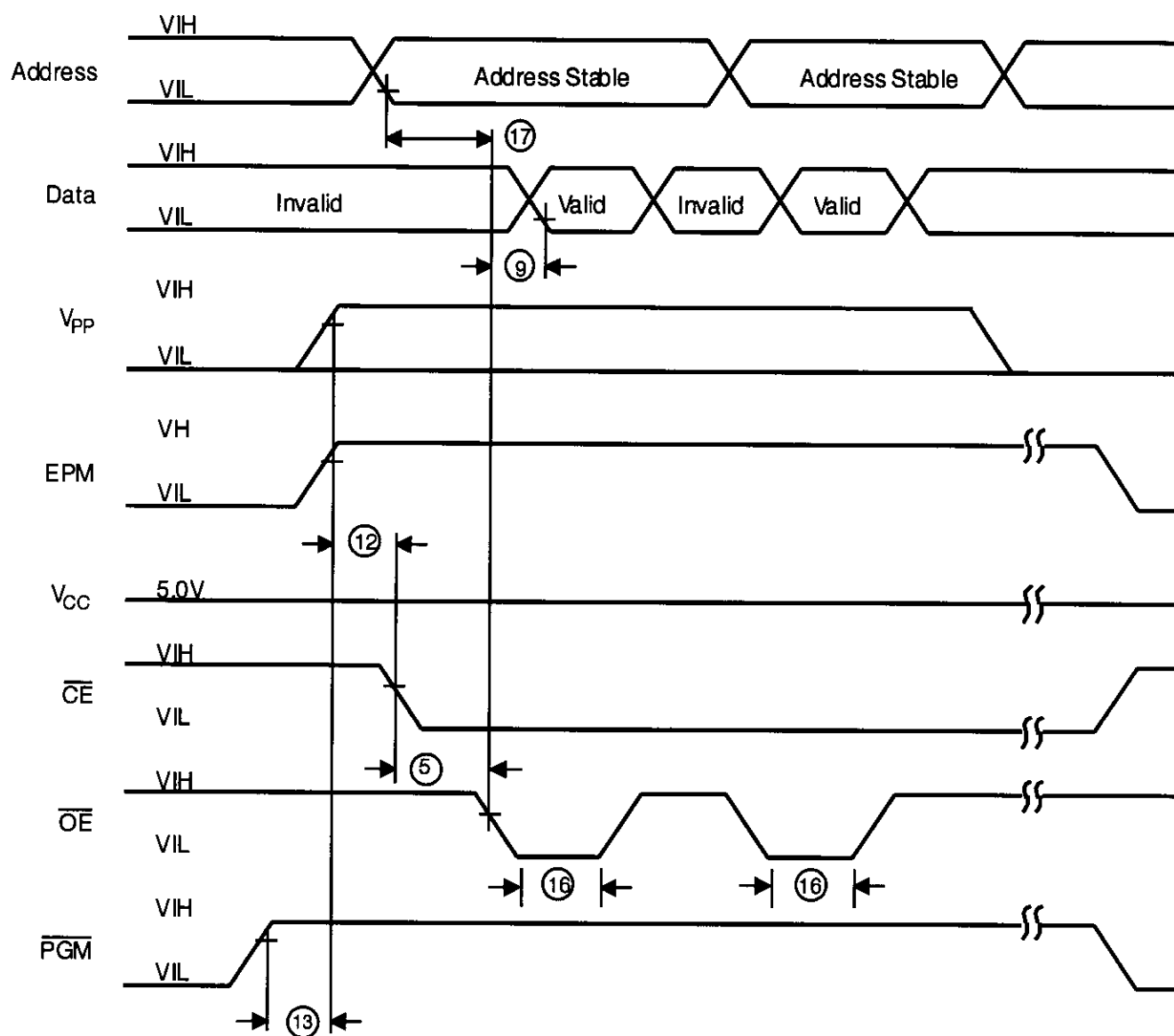


Figure 19. Z86E04/E08 Programming Waveform  
(EPROM Read)



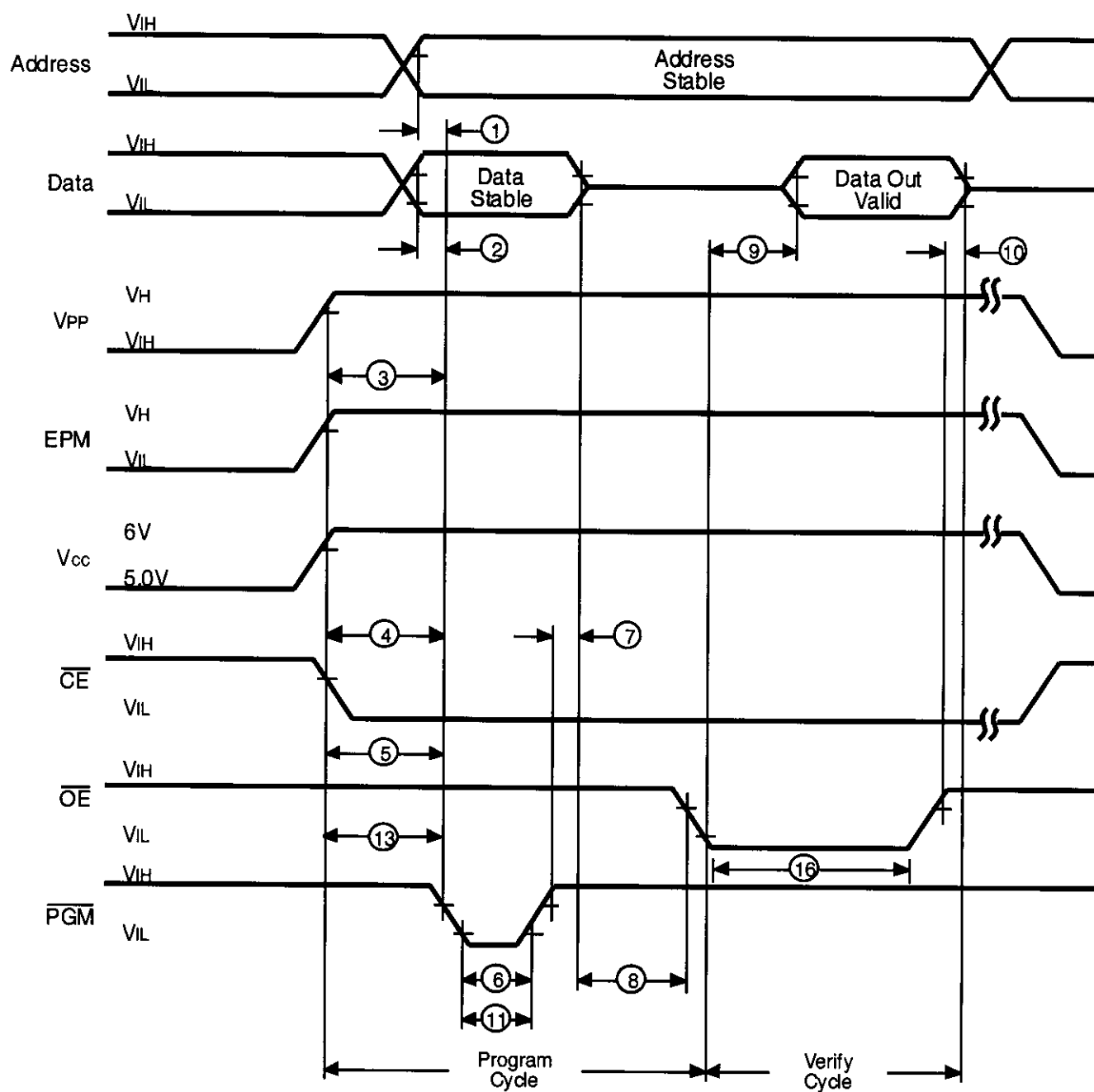


Figure 20. Z86E04/E08 Programming Waveform  
(Program and Verify)

# FUNCTIONAL DESCRIPTION (Continued)

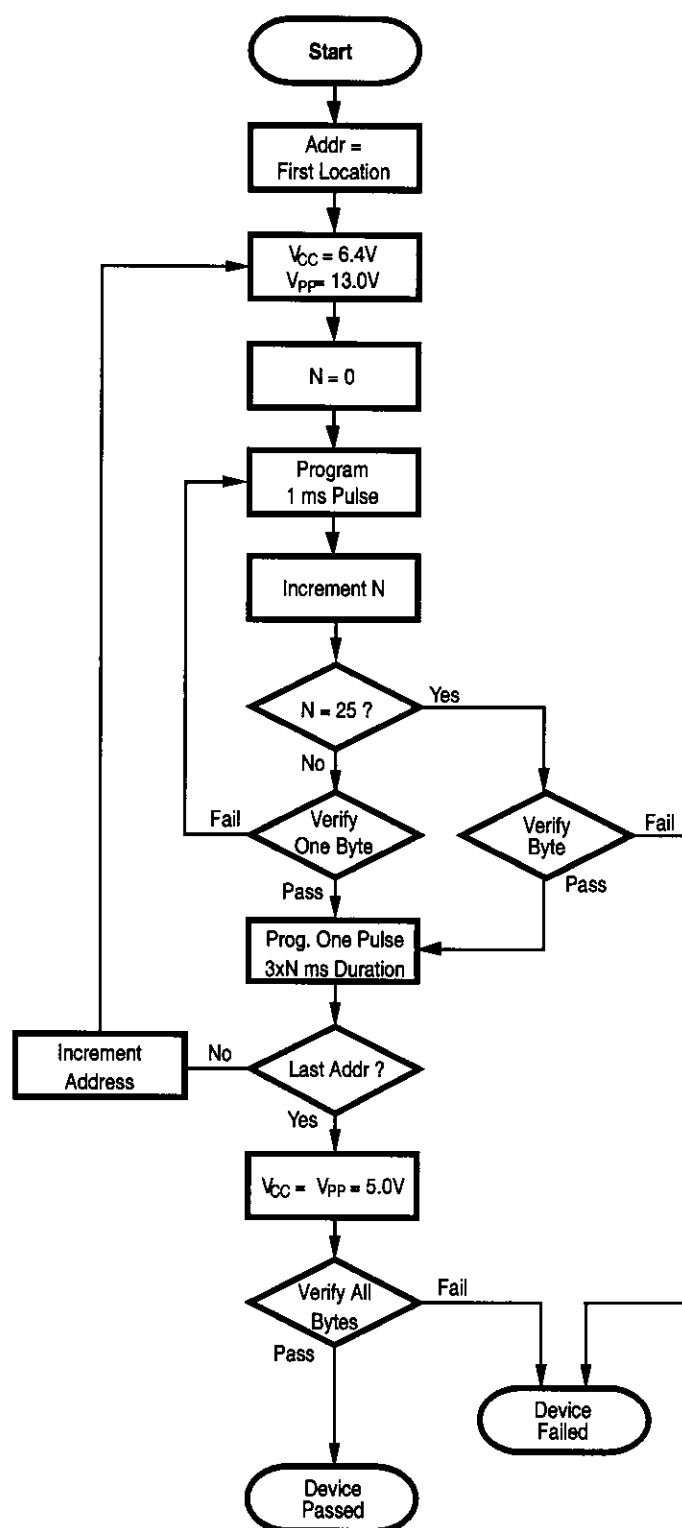


Figure 23. Z86E04/E08 Programming Algorithm

## Z8 CONTROL REGISTERS (Continued)

R248 P01M

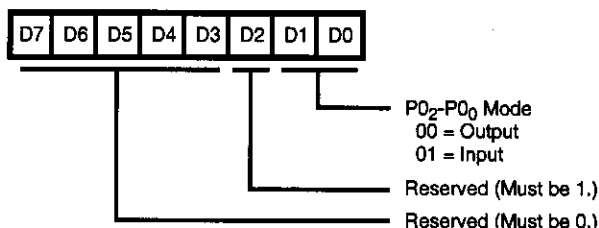


Figure 31. Port 0 and 1 Mode Register  
(F8<sub>H</sub>: Write Only)

R249 IPR

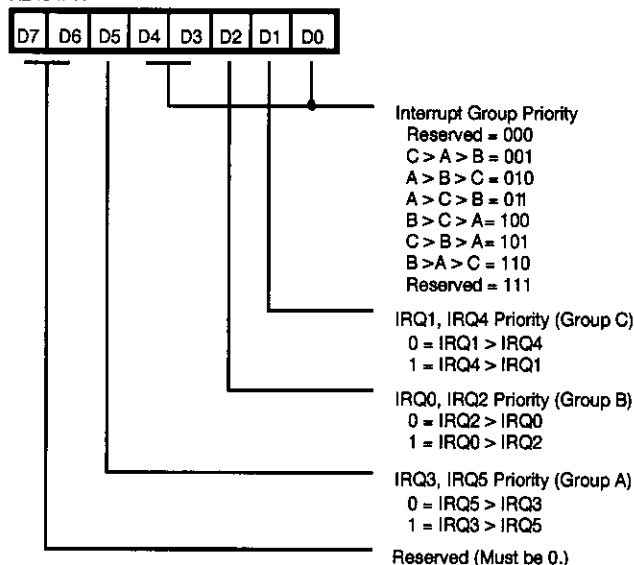


Figure 32. Interrupt Priority Register  
(F9<sub>H</sub>: Write Only)

R250 IRQ

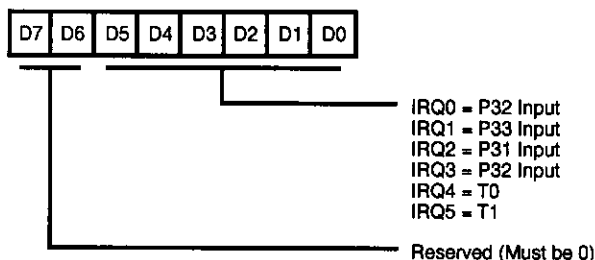


Figure 33. Interrupt Request Register  
(FA<sub>H</sub>: Read/Write)

R251 IMR

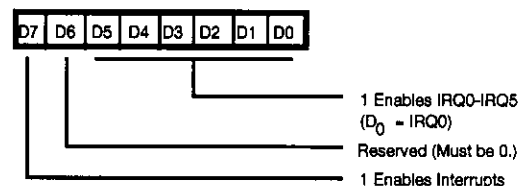


Figure 34. Interrupt Mask Register  
(FB<sub>H</sub>: Read/Write)

R252 Flags

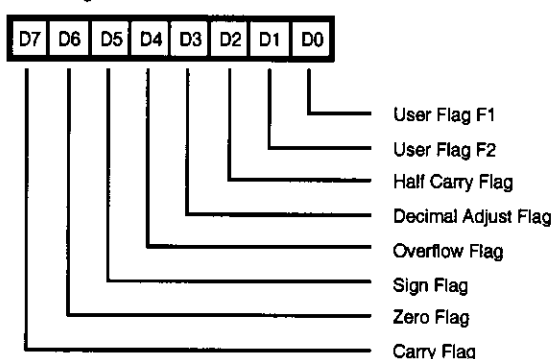


Figure 35. Flag Register  
(FC<sub>H</sub>: Read/Write)

R253 RP

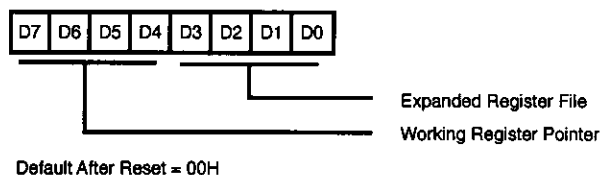


Figure 36. Register Pointer  
(FD<sub>H</sub>: Read/Write)

R255 SPL

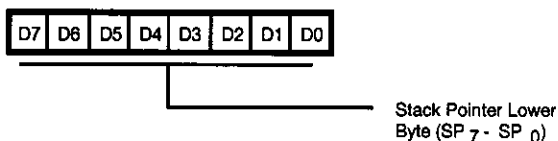
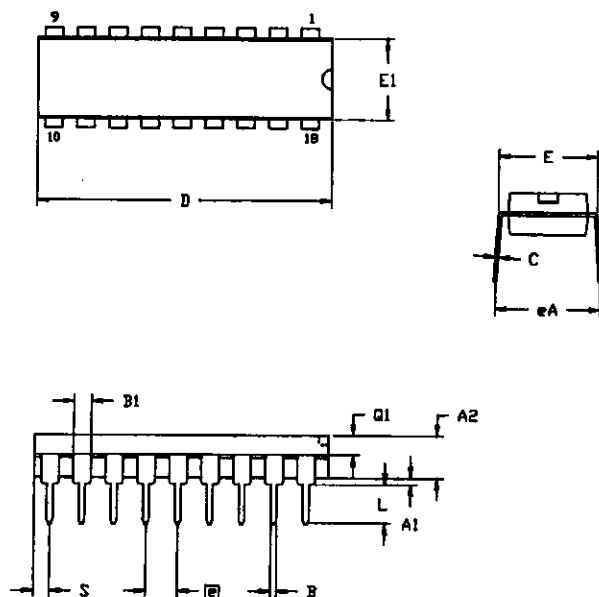


Figure 37. Stack Pointer  
(FF<sub>H</sub>: Read/Write)

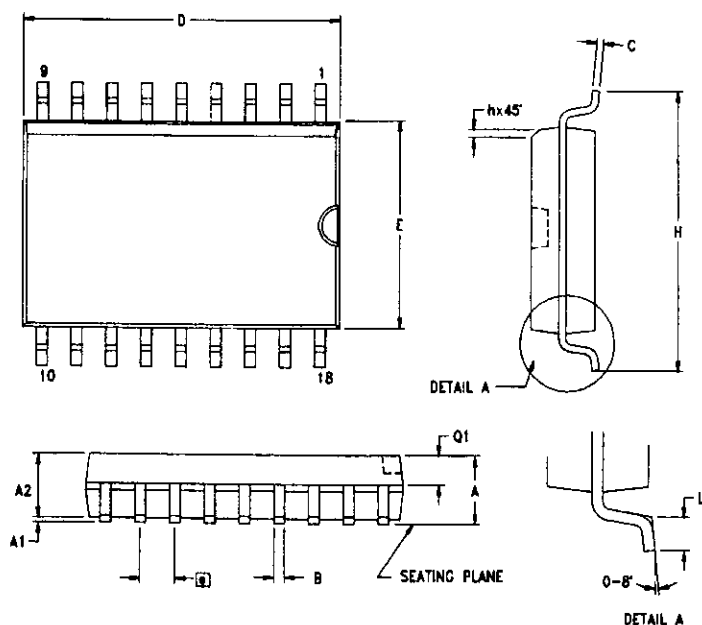
## PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

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