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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 125 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86e0412heg1903 |

## FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1µs @ 12 MHz)
- RAM Bytes (125)

## GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8® MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

**Note:** All Signals with an overline, "‾", are active Low, for example: B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

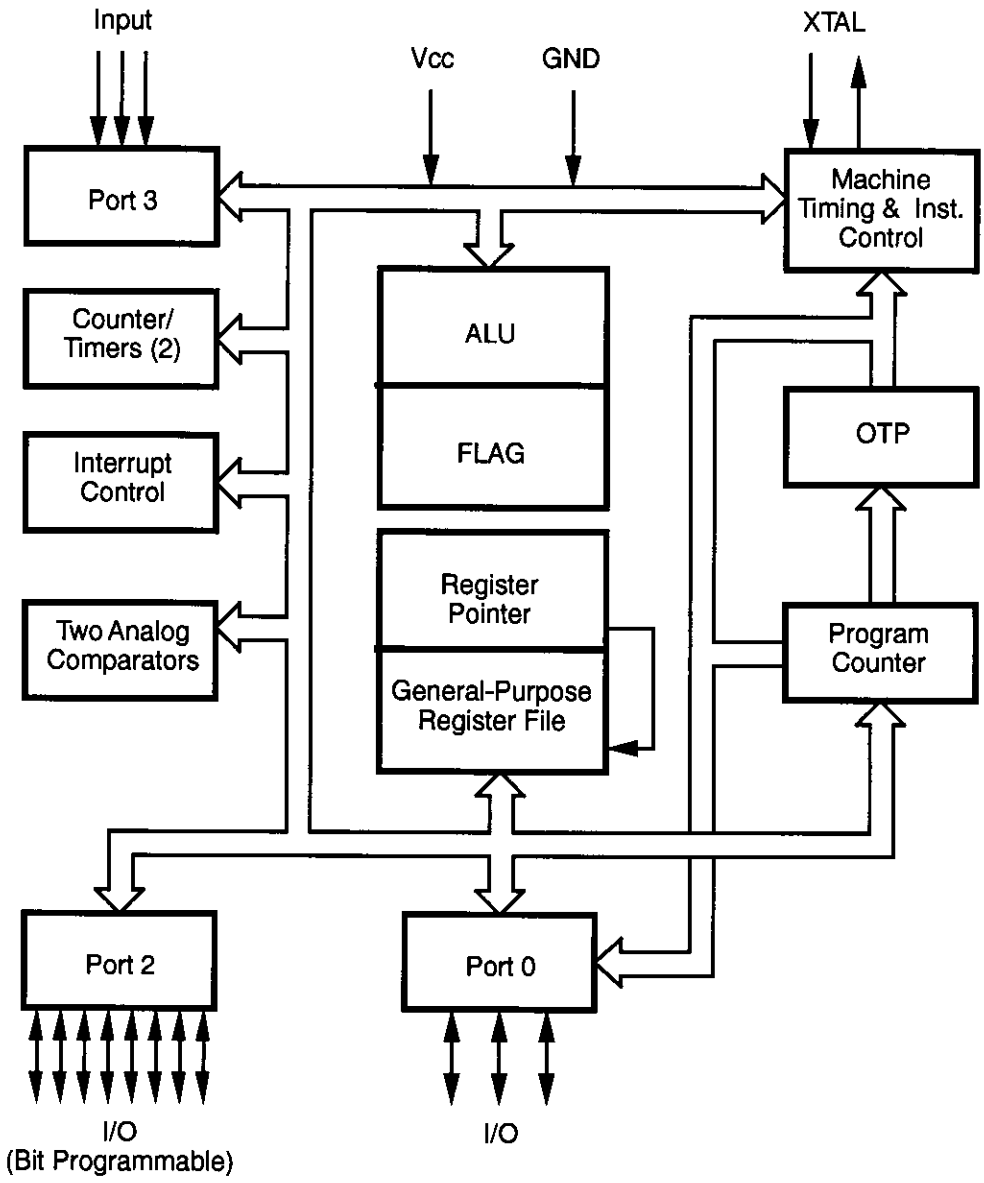


**Figure 1. Functional Block Diagram**

## PIN DESCRIPTION

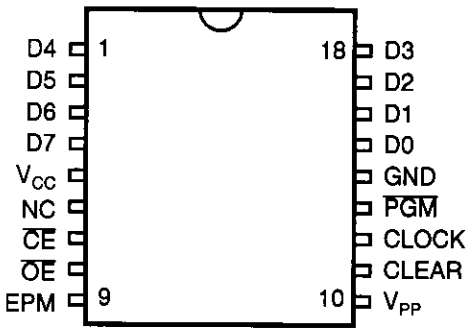


**Figure 3. 18-Pin EPROM Mode Configuration**

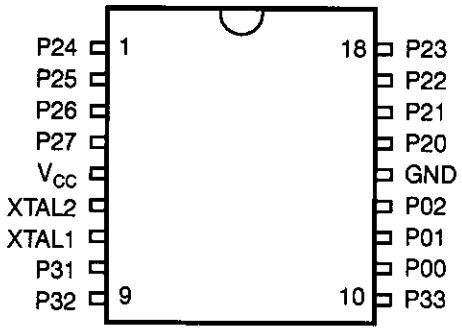


**Figure 4. 18-Pin DIP/SOIC Mode Configuration**

**Table 1. 18-Pin DIP Pin Identification**

| EPROM Programming Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | D4–D7 | Data 4, 5, 6, 7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | NC | No Connection | |
| 7 | $\overline{CE}$ | Chip Enable | Input |
| 8 | $\overline{OE}$ | Output Enable | Input |
| 9 | EPM | EPROM Prog Mode | Input |
| 10 | $V_{PP}$ | Prog Voltage | Input |
| 11 | Clear | Clear Clock | Input |
| 12 | Clock | Address | Input |
| 13 | $\overline{PGM}$ | Prog Mode | Input |
| 14 | GND | Ground | |
| 15–18 | D0–D3 | Data 0,1, 2, 3 | In/Output |

**Table 2. 18-Pin DIP/SOIC Pin Identification**

| Standard Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | P24–P27 | Port 2, Pins 4,5,6,7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Osc. Clock | Output |
| 7 | XTAL1 | Crystal Osc. Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11–13 | P00–P02 | Port 0, Pins 0,1,2 | In/Output |
| 14 | GND | Ground | |
| 15–18 | P20–P23 | Port 2, Pins 0,1,2,3 | In/Output |

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation = $V_{DD}$ x [$I_{DD}$–(sum of $I_{OH}$)]
+ sum of [($V_{DD}$–$V_{OH}$) x $I_{OH}$]
+ sum of ($V_{OL}$ x $I_{OL}$)

| Parameter | Min | Max | Units | Note |
|---|---|---|---|---|
| Ambient Temperature under Bias | –40 | +105 | C | |
| Storage Temperature | –65 | +150 | C | |
| Voltage on any Pin with Respect to $V_{SS}$ | –0.7 | +12 | V | 1 |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$ | –0.3 | +7 | V | |
| Voltage on Pins 7, 8, 9, 10 with Respect to $V_{SS}$ | –0.6 | $V_{DD}$+1 | V | 2 |
| Total Power Dissipation | | 1.65 | W | |
| Maximum Allowable Current out of $V_{SS}$ | | 300 | mA | |
| Maximum Allowable Current into $V_{DD}$ | | 220 | mA | |
| Maximum Allowable Current into an Input Pin | –600 | +600 | µA | 3 |
| Maximum Allowable Current into an Open-Drain Pin | –600 | +600 | µA | 4 |
| Maximum Allowable Output Current Sinked by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA | |
| Total Maximum Output Current Sinked by a Port | | 60 | mA | |
| Total Maximum Output Current Sourced by a Port | | 45 | mA | |

**Notes:**

1. This applies to all pins except where otherwise noted. Maximum current into pin must be ± 600 µA.
2. There is no input protection diode from pin to $V_{DD}$ (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current | 4.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 4.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 4.5V | | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| | | 5.5V | | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| $I_{CC1}$ | Standby Current | 4.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| | | 4.5V | | 7.0 | 4.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,7 |
| | | 5.5V | | 7.0 | 4.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | 5,7 |
| $I_{CC}$ | Supply Current (Low Noise Mode) | 4.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 4.5V | | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 4.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

## AC ELECTRICAL CHARACTERISTICS

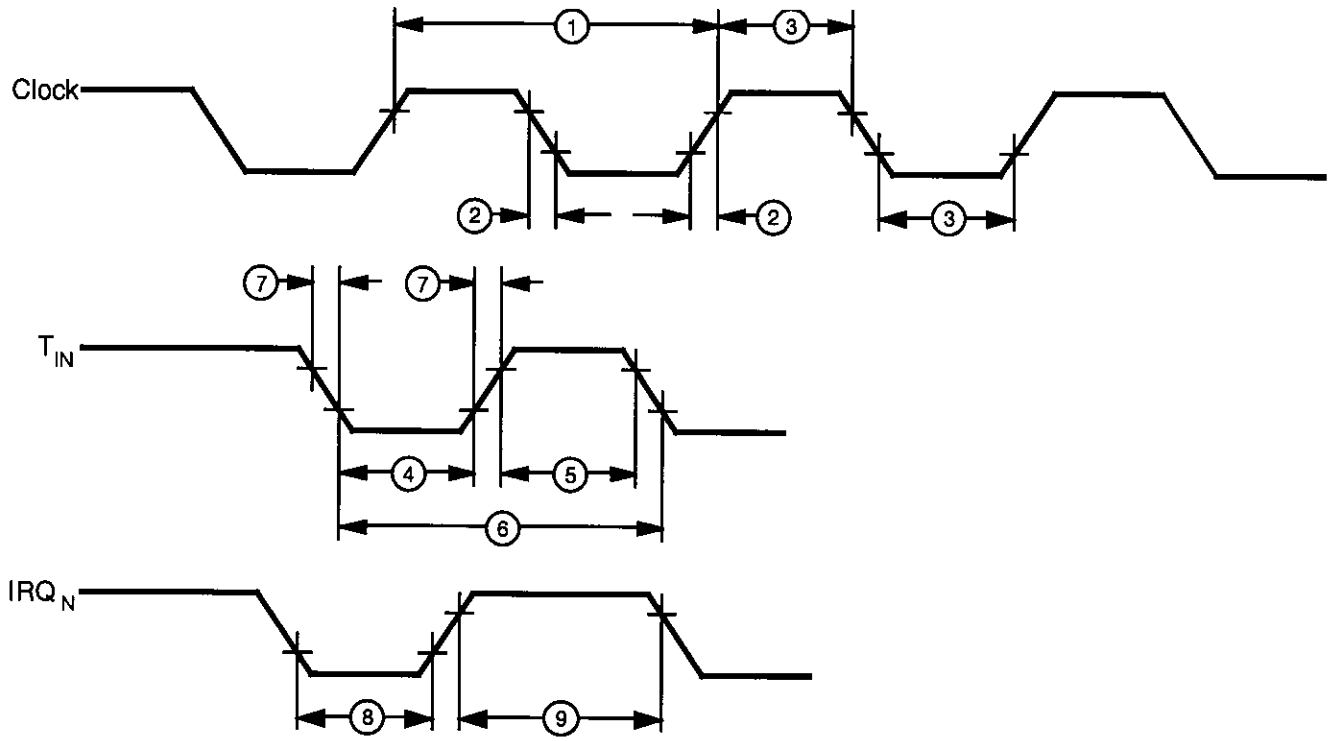


**Figure 6. AC Electrical Timing Diagram**

## AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

| | | | | $T_A$= –40 °C to +105 °C | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 4 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TPC | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC<br>TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4. | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 4TpC | 4TpC | | | 1 |
| | | | 5.5V | | 4TpC | 4TpC | | | 1 |
| 7 | TrTin,<br>TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 10 | | 10 | | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

# LOW NOISE VERSION

## Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

# PIN FUNCTIONS

## OTP Programming Mode

**D7–D0** *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

**$V_{CC}$** *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

**$\overline{CE}$** *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

**$\overline{OE}$** *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

**EPM** *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

**$V_{PP}$** *Program Voltage.* This pin supplies the program voltage.

**Clear** *Clear* (active High). This pin resets the internal address counter at the High Level.

**Clock** *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

**$\overline{PGM}$** *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

## Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above $V_{CC}$ occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the $V_{PP}$, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to $V_{CC}$.
- Adding a capacitor to the affected pin.

**Note:** Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

**Port 2, P27–P20.** Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

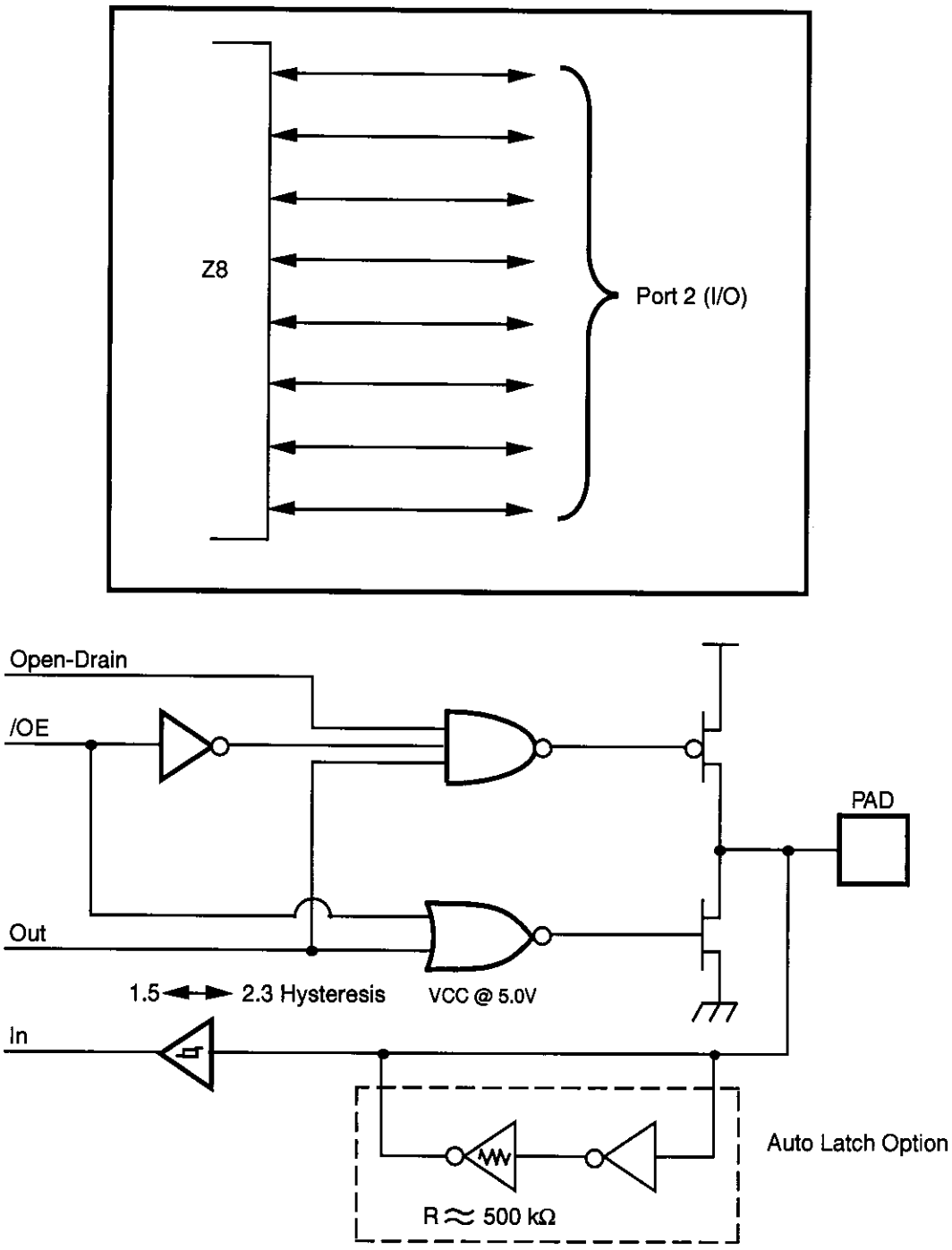


**Figure 8. Port 2 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0–4 V when the $V_{CC}$ is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or $T_{IN}$ through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

**RESET.** This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

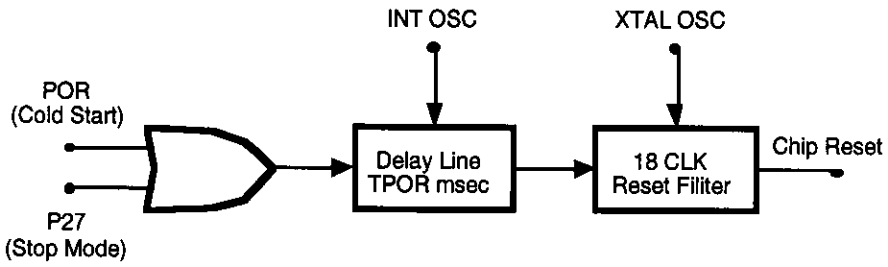


**Figure 10. Internal Reset Configuration**

**Power-On Reset (POR).** A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows $V_{CC}$ and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

**Watch-Dog Timer Reset.** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

## FUNCTIONAL DESCRIPTION (Continued)

**Table 3. Control Registers**

| | | Reset Condition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr.** | **Reg.** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Comments** |
| FF | SPL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FD | RP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FC | FLAGS | U | U | U | U | U | U | U | U | |
| FB | IMR | 0 | U | U | U | U | U | U | U | |
| FA | IRQ | U | U | 0 | 0 | 0 | 0 | 0 | 0 | IRQ3 is used for positive edge detection |
| F9 | IPR | U | U | U | U | U | U | U | U | |
| F8* | P01M | U | U | U | 0 | U | U | 0 | 1 | |
| F7* | P3M | U | U | U | U | U | U | 0 | 0 | |
| F6* | P2M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Inputs after reset |
| F5 | PRE0 | U | U | U | U | U | U | U | 0 | |
| F4 | T0 | U | U | U | U | U | U | U | U | |
| F3 | PRE1 | U | U | U | U | U | U | 0 | 0 | |
| F2 | T1 | U | U | U | U | U | U | U | U | |
| F1 | TMR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Note:** *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

**Program Memory.** The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

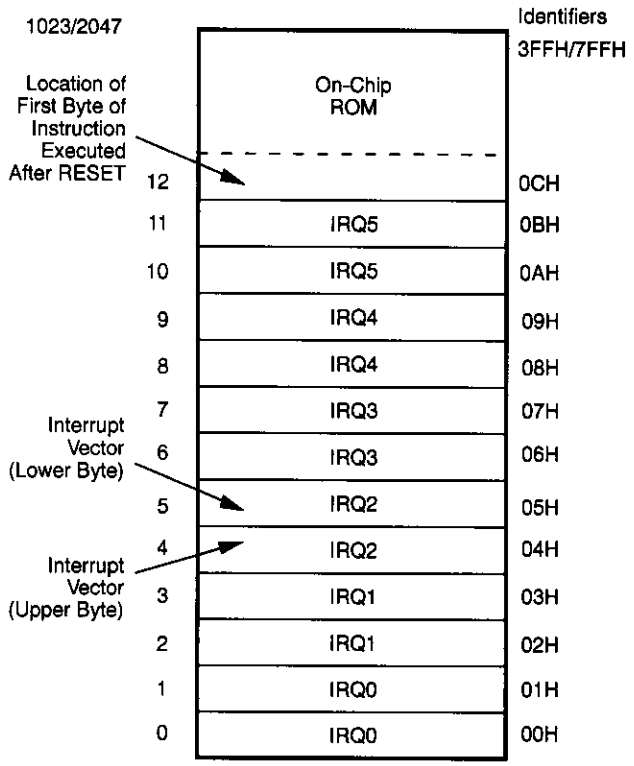


**Figure 11. Program Memory Map**

**Register File.** The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

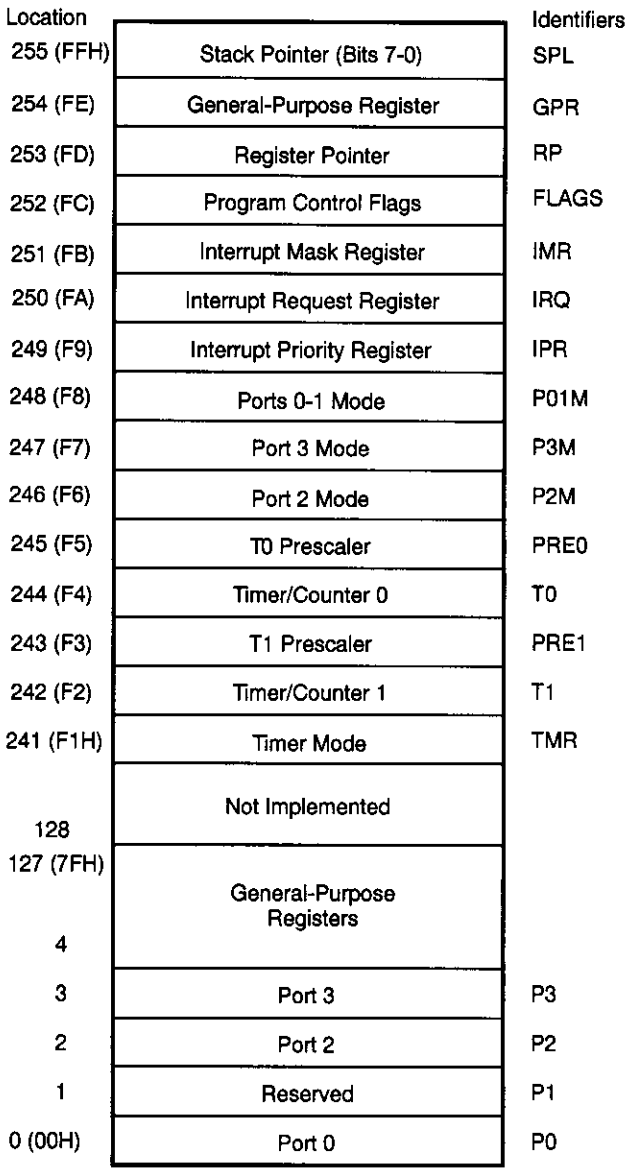


**Figure 12. Register File**

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

**Note:** User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

**Table 4. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | AN2(P32) | 0,1 | External (F)Edge |
| IRQ1 | REF(P33) | 2,3 | External (F)Edge |
| IRQ2 | AN1(P31) | 4,5 | External (F)Edge |
| IRQ3 | AN2(P32) | 6,7 | External (R)Edge |
| IRQ4 | T0 | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |

**Notes:**
F = Falling edge triggered
R = Rising edge triggered

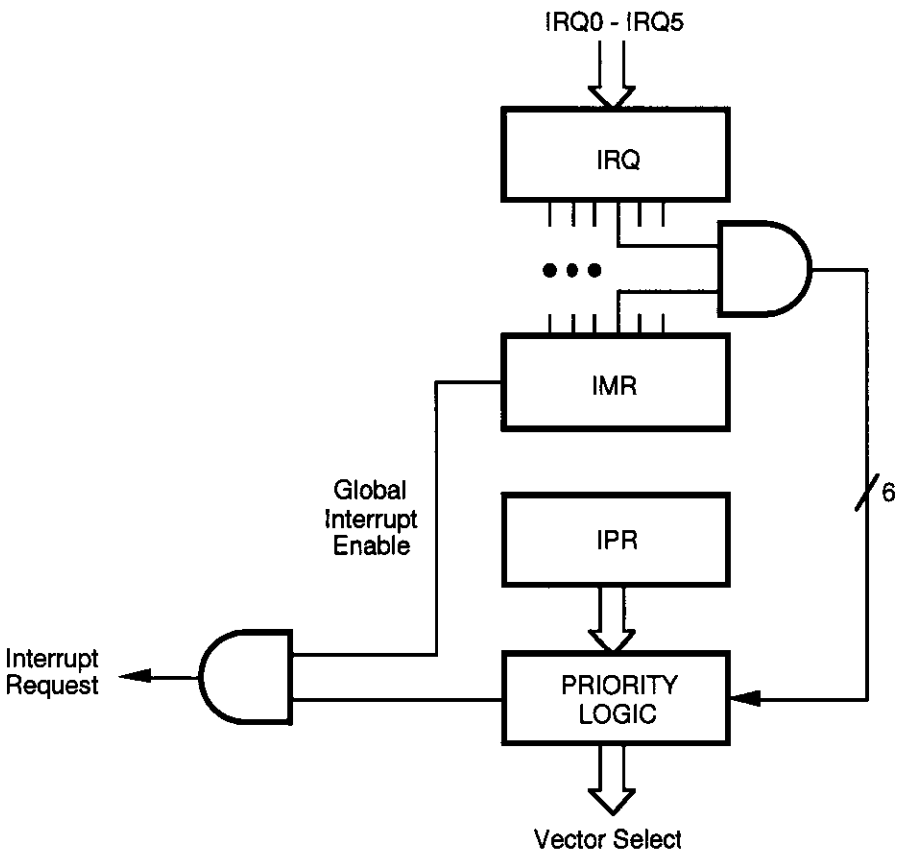


**Figure 15. Interrupt Block Diagram**

## FUNCTIONAL DESCRIPTION (Continued)

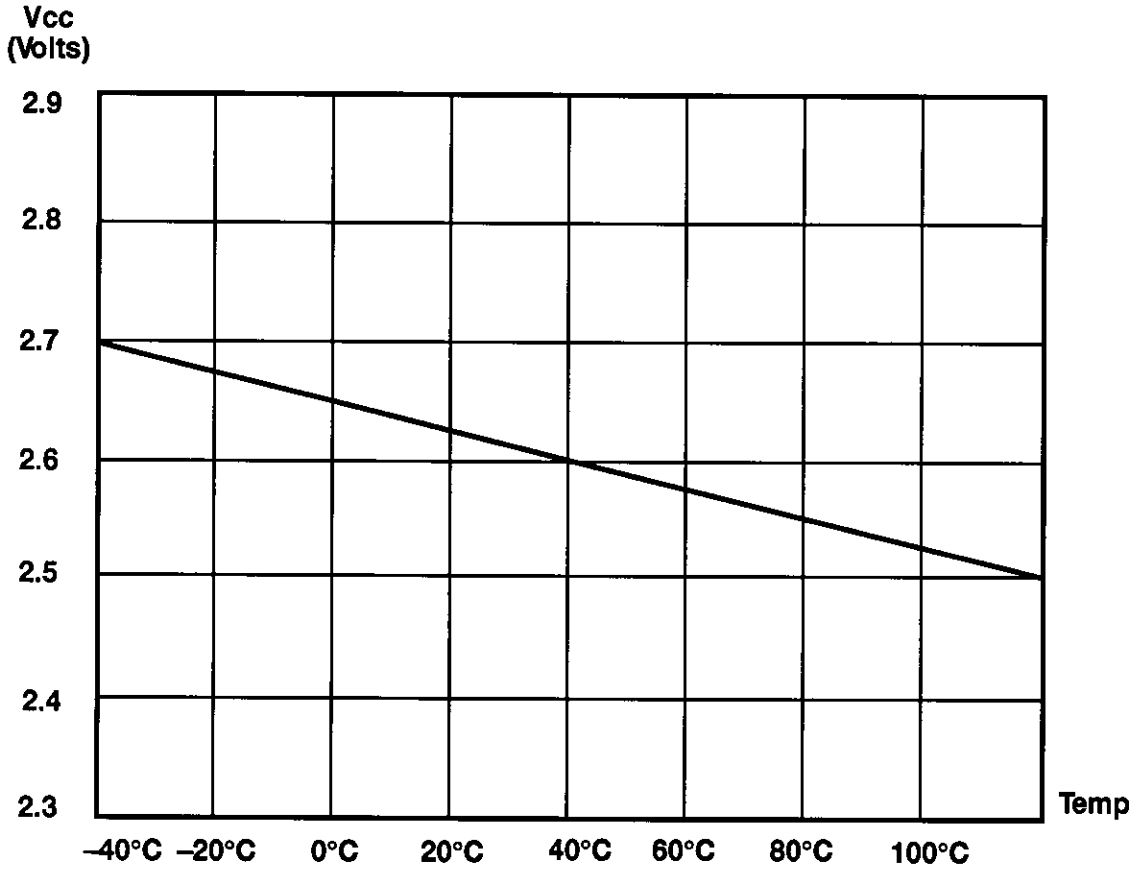


**Figure 17. Typical Auto Reset Voltage ($V_{LV}$) vs. Temperature**

## FUNCTIONAL DESCRIPTION (Continued)

**Internal Address Counter.** The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

**Programming Waveform.** Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 23 shows the flow chart of the Z8 programming algorithm.

**Table 8. Timing of Programming Waveforms**

| Parameters | Name | Min | Max | Units |
|---|---|---|---|---|
| 1 | Address Setup Time | 2 | | µs |
| 2 | Data Setup Time | 2 | | µs |
| 3 | $V_{PP}$ Setup | 2 | | µs |
| 4 | $V_{CC}$ Setup Time | 2 | | µs |
| 5 | Chip Enable Setup Time | 2 | | µs |
| 6 | Program Pulse Width | 0.95 | | ms |
| 7 | Data Hold Time | 2 | | µs |
| 8 | $\overline{OE}$ Setup Time | 2 | | µs |
| 9 | Data Access Time | 188 | | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | µs |
| 13 | $\overline{PGM}$ Setup Time | 2 | | µs |
| 14 | Address to $\overline{OE}$ Setup Time | 2 | | µs |
| 15 | Option Program Pulse Width | 78 | | ms |
| 16 | $\overline{OE}$ Width | 250 | | ns |
| 17 | Address Valid to $\overline{OE}$ Low | 125 | | ns |

## FUNCTIONAL DESCRIPTION (Continued)

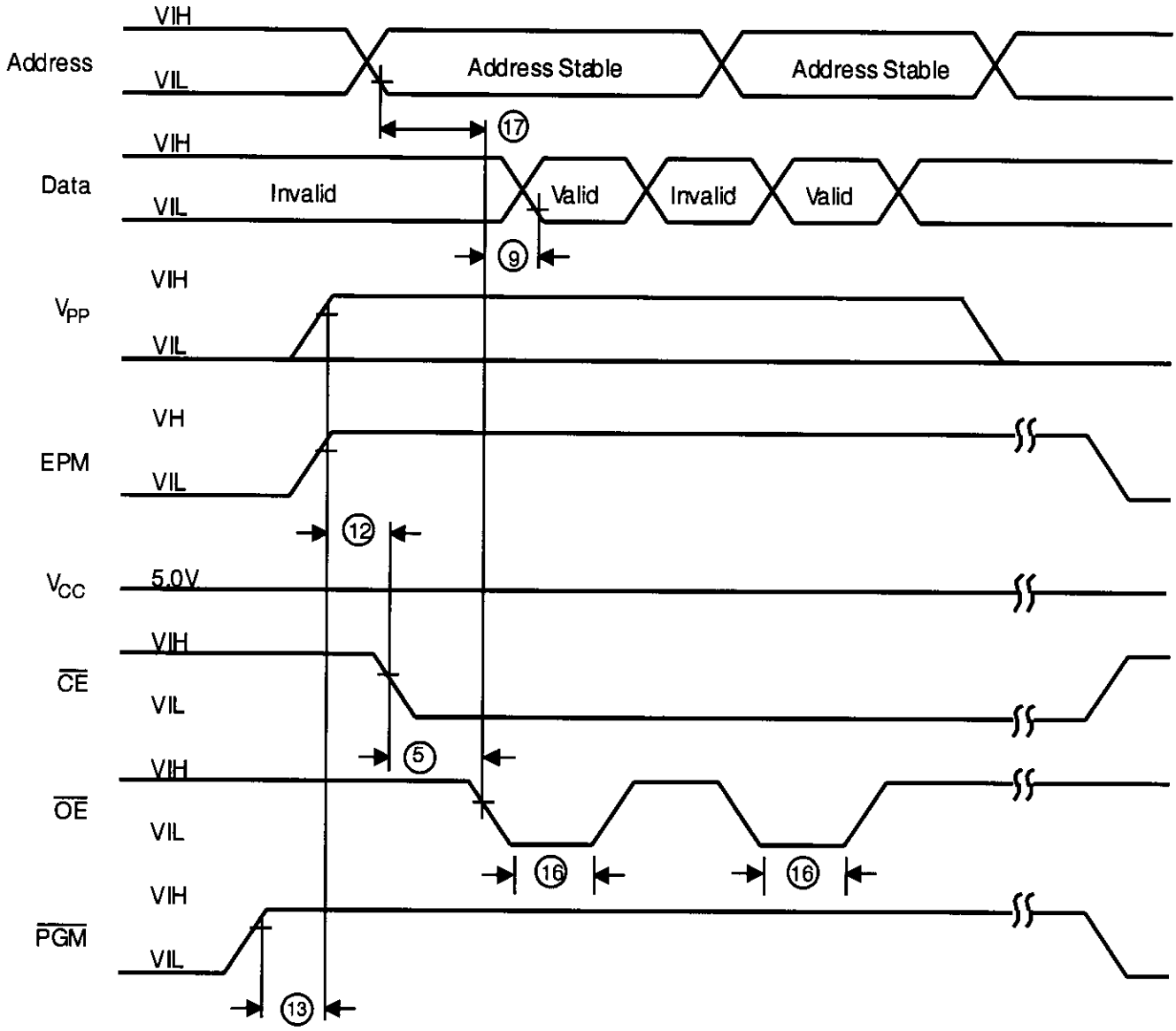


**Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)**

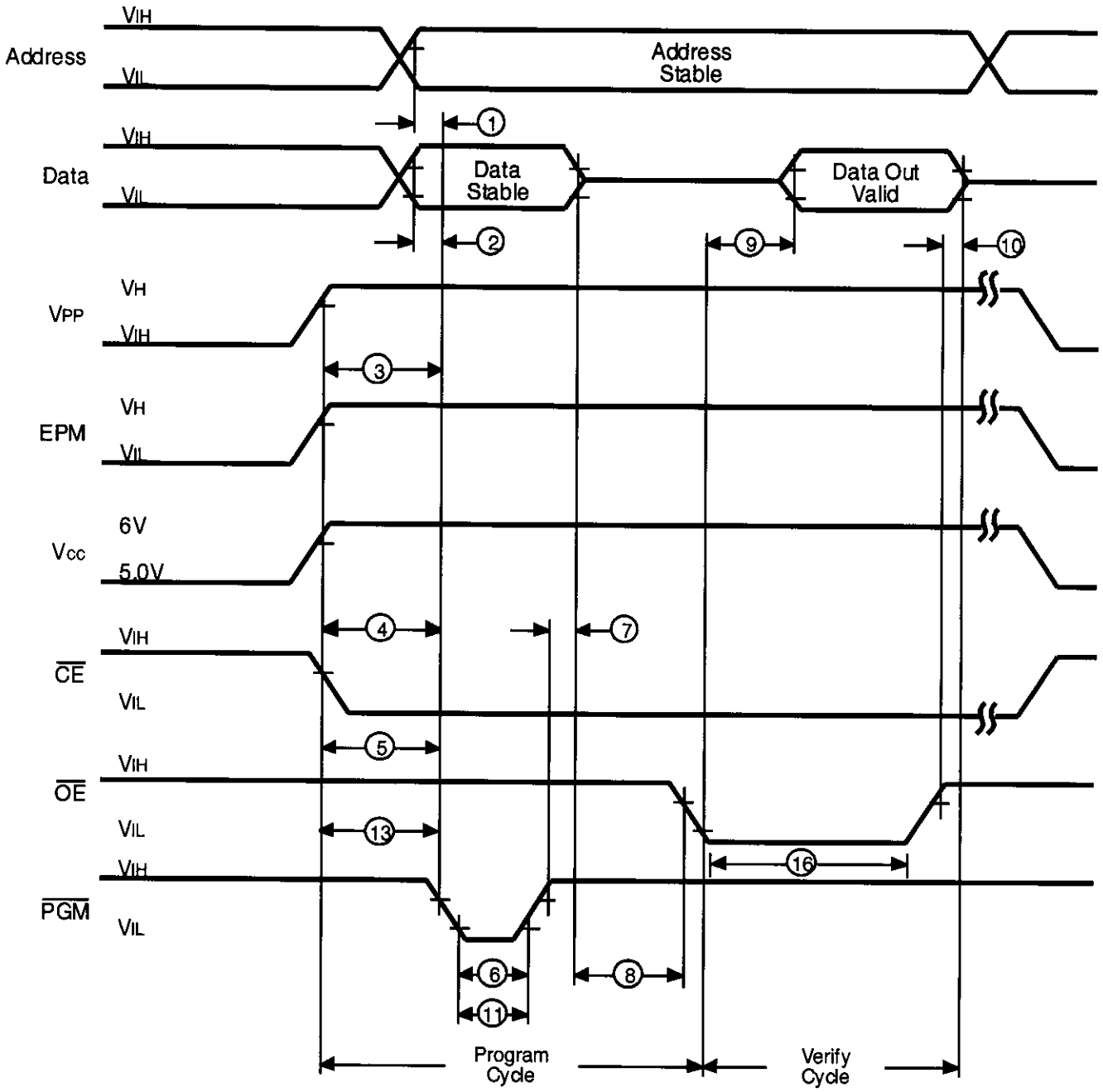


**Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)**

## FUNCTIONAL DESCRIPTION (Continued)

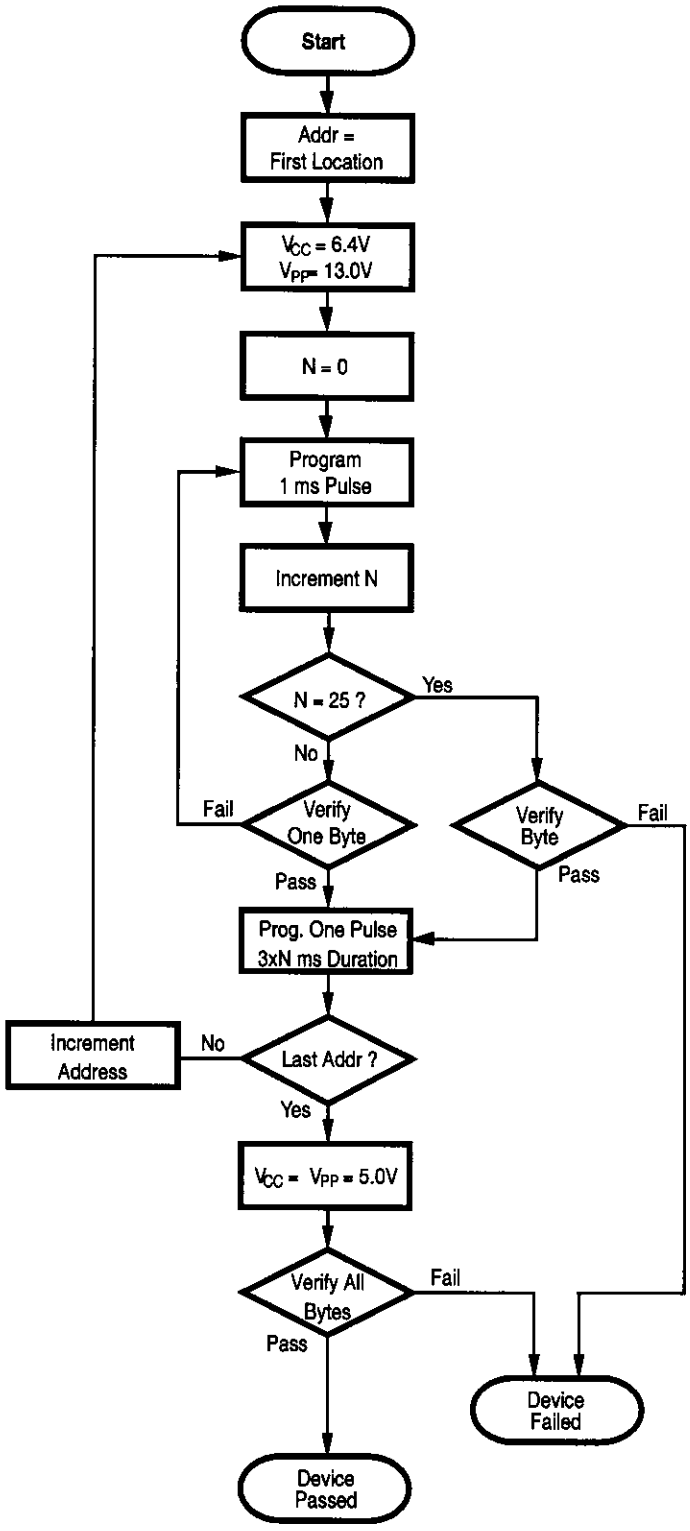


**Figure 23. Z86E04/E08 Programming Algorithm**

## Z8 CONTROL REGISTERS (Continued)

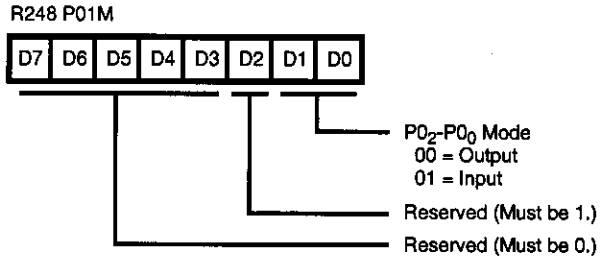


**Figure 31. Port 0 and 1 Mode Register ($F8_H$: Write Only)**

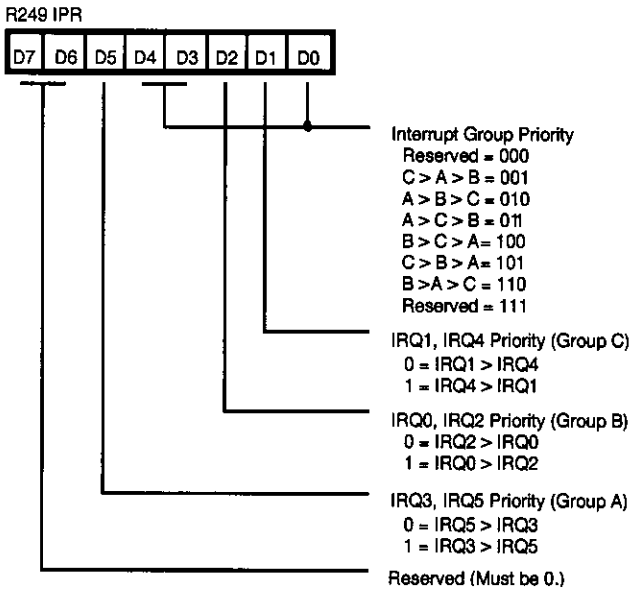


**Figure 32. Interrupt Priority Register ($F9_H$: Write Only)**

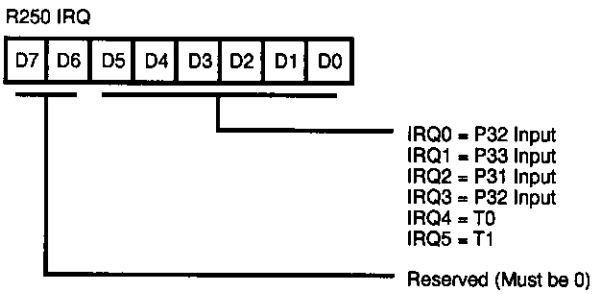


**Figure 33. Interrupt Request Register ($FA_H$: Read/Write)**

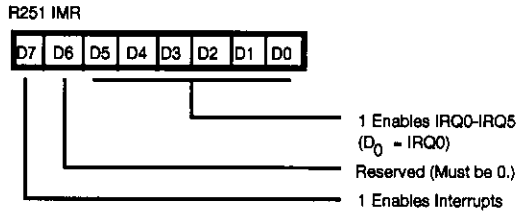


**Figure 34. Interrupt Mask Register ($FB_H$: Read/Write)**

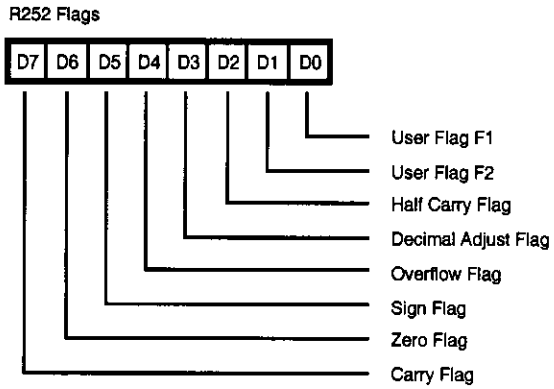


**Figure 35. Flag Register ($FC_H$: Read/Write)**

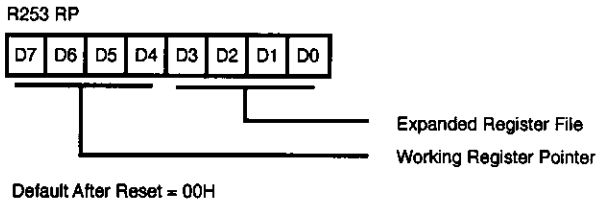


**Figure 36. Register Pointer ($FD_H$: Read/Write)**

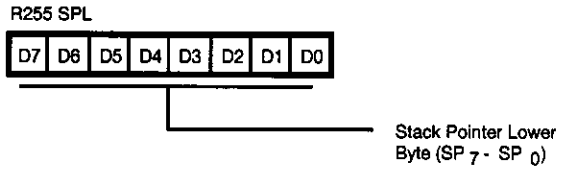


**Figure 37. Stack Pointer ($FF_H$: Read/Write)**

**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.



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