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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0412hsc1866tr

PIN DESCRIPTION

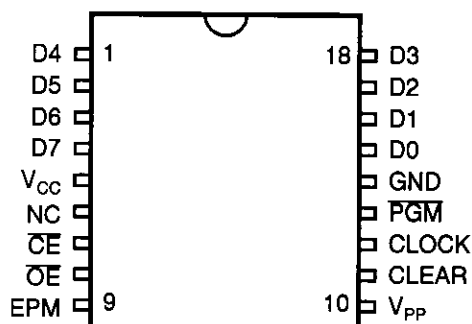


Figure 3. 18-Pin EPROM Mode Configuration

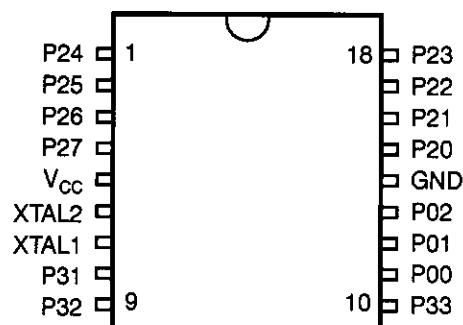


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode			
Pin #	Symbol	Function	Direction
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V _{CC}	Power Supply	
6	NC	No Connection	
7	CE	Chip Enable	Input
8	OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V _{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	PGM	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0,1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode			
Pin #	Symbol	Function	Direction
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V _{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

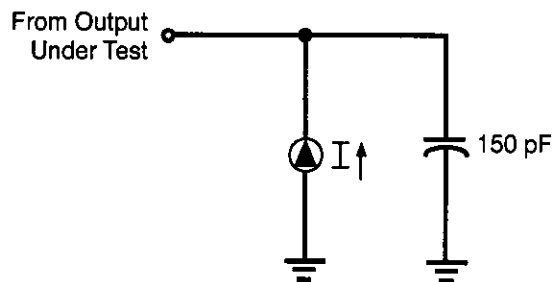


Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

Sym	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ Typical			Units	Conditions	Notes
		V_{CC} [4]	Min	Max @ 25°C			
I_{CC}	Supply Current	4.5V		11.0	6.8	mA All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		4.0	2.5	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	5,7
		5.5V		4.0	2.5	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA HALT Mode $V_{IN} = 0V$, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA All Output and I/O Pins Floating @ 4 MHz	7

DC ELECTRICAL CHARACTERISTICS

Extended Temperature

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V _{INMAX}	Max Input Voltage	4.5V		12.0		V	I _{IN} < 250 µA	1
		5.5V		12.0		V	I _{IN} < 250 µA	1
V _{CH}	Clock Input High Voltage	4.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
V _{IL}	Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage	4.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		4.5V	V _{CC} -0.4			V	Low Noise @ I _{OH} = -0.5 mA	
		5.5V	V _{CC} -0.4			V	Low Noise @ I _{OH} = -0.5 mA	
V _{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I _{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
V _{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I _{OL} = +12 mA,	5
		5.5V		1.0	0.3	V	I _{OL} = +12 mA,	5
V _{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V _{LV}	V _{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I _{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
		5.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	4.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
		5.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range		0	V _{CC} -1.5		V		

AC ELECTRICAL CHARACTERISTICS

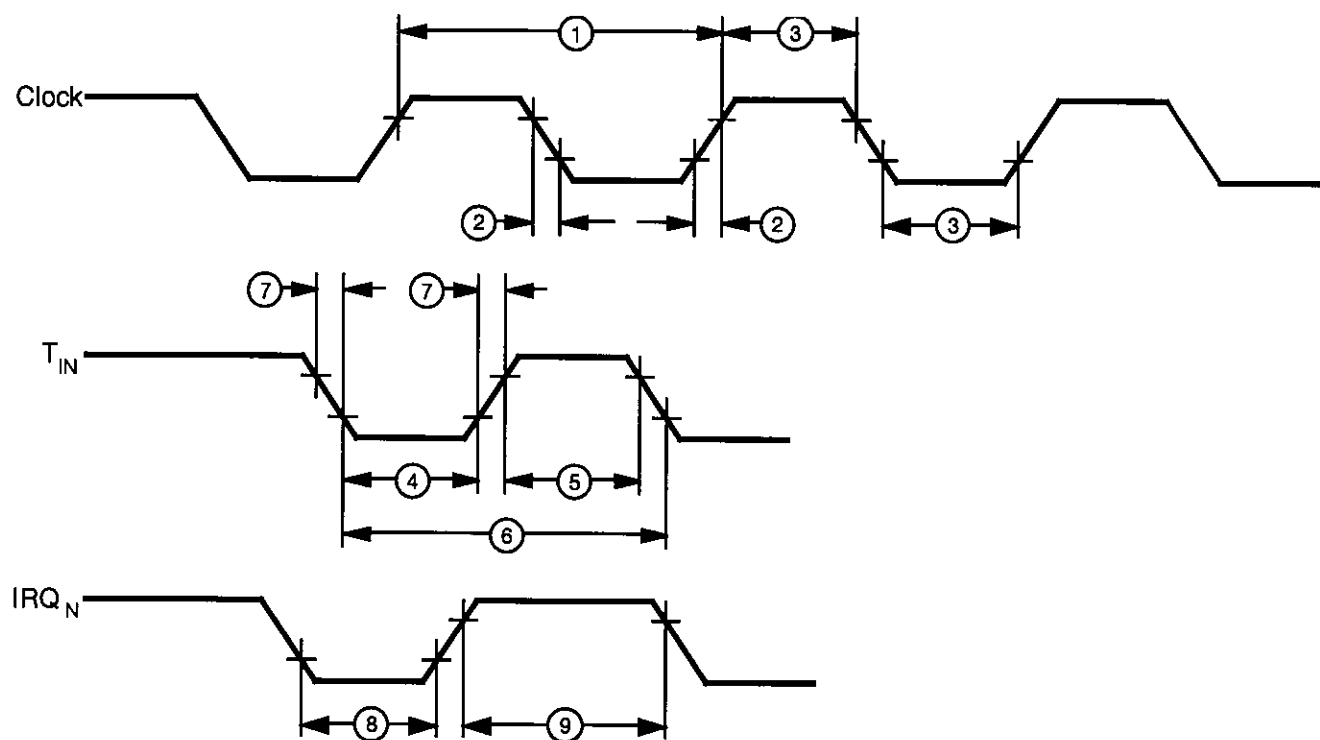


Figure 6. AC Electrical Timing Diagram

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

\overline{CE} Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

\overline{OE} Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear Clear (active High). This pin resets the internal address counter at the High Level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one with one clock cycle.

PGM Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V_{PP}, \overline{CE} , EPM, \overline{OE} pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).

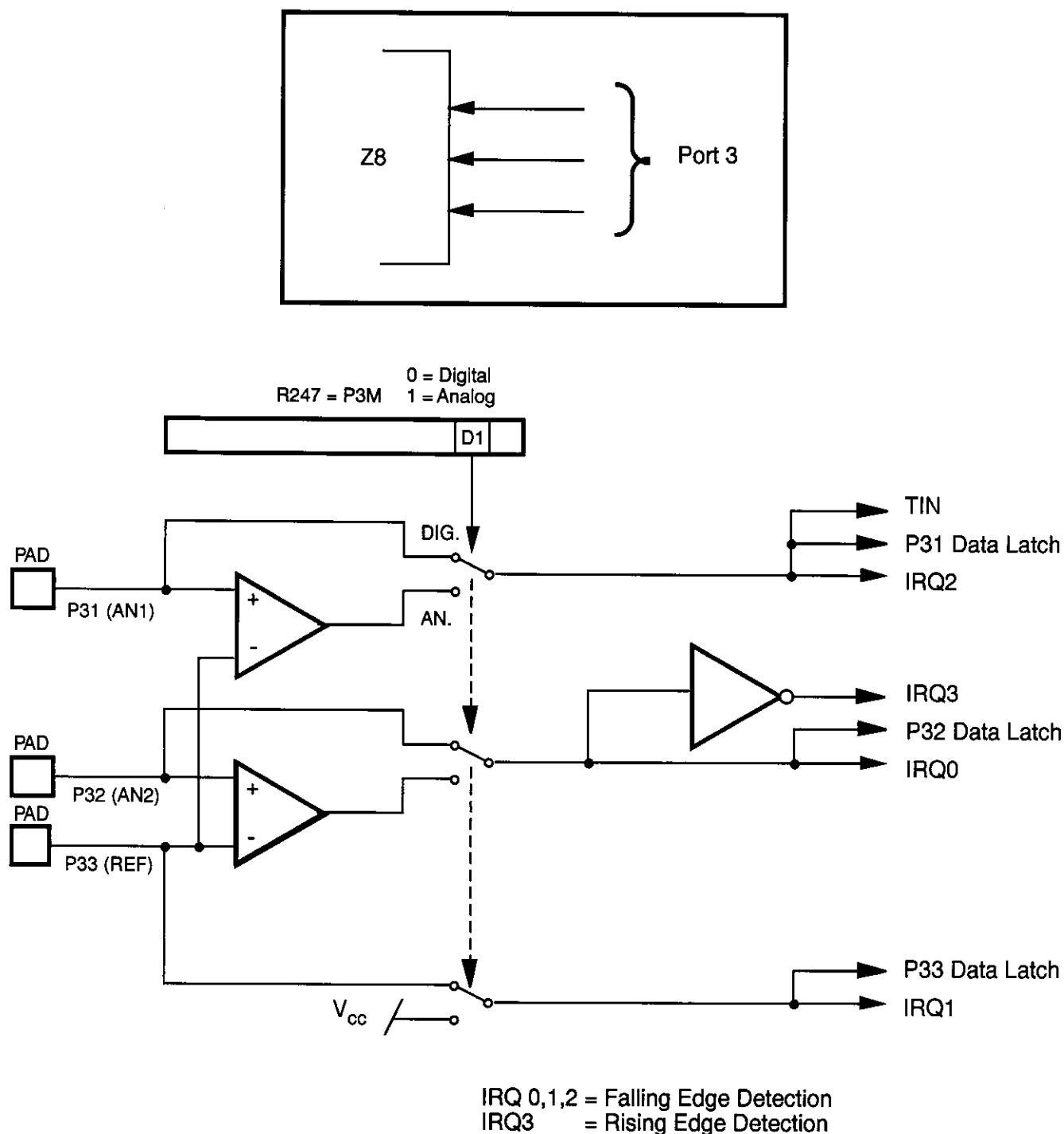


Figure 9. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

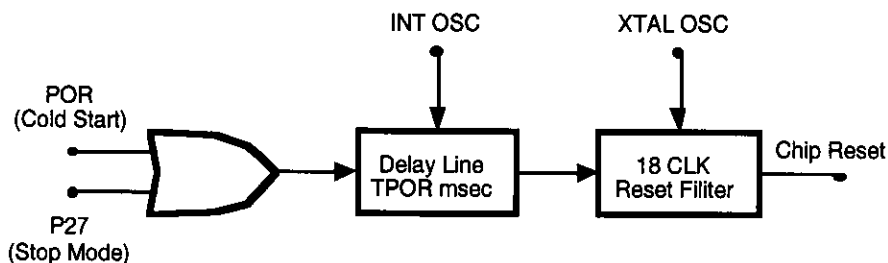


Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

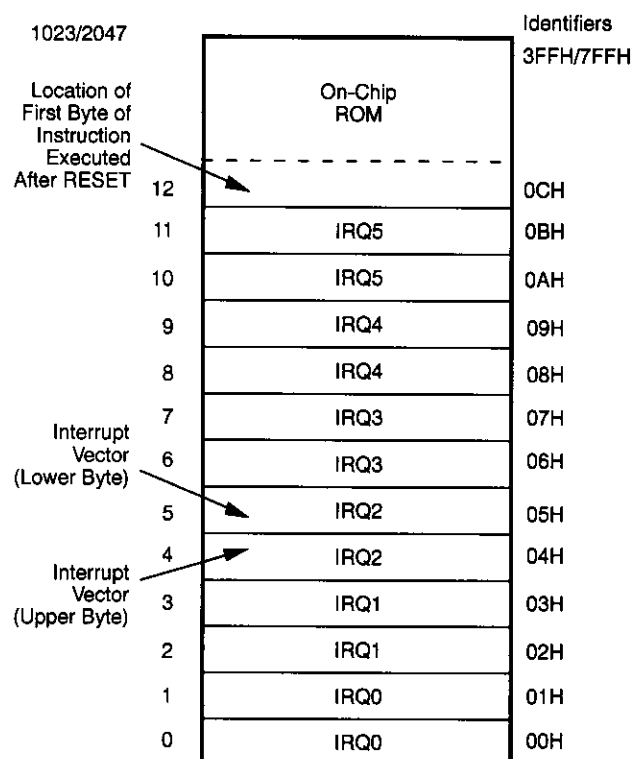


Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

Location	Identifiers
255 (FFH)	Stack Pointer (Bits 7-0) SPL
254 (FE)	General-Purpose Register GPR
253 (FD)	Register Pointer RP
252 (FC)	Program Control Flags FLAGS
251 (FB)	Interrupt Mask Register IMR
250 (FA)	Interrupt Request Register IRQ
249 (F9)	Interrupt Priority Register IPR
248 (F8)	Ports 0-1 Mode P01M
247 (F7)	Port 3 Mode P3M
246 (F6)	Port 2 Mode P2M
245 (F5)	T0 Prescaler PRE0
244 (F4)	Timer/Counter 0 T0
243 (F3)	T1 Prescaler PRE1
242 (F2)	Timer/Counter 1 T1
241 (F1H)	Timer Mode TMR
128	Not Implemented
127 (7FH)	General-Purpose Registers
4	
3	Port 3 P3
2	Port 2 P2
1	Reserved P1
0 (00H)	Port 0 P0

Figure 12. Register File

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:

F = Falling edge triggered

R = Rising edge triggered

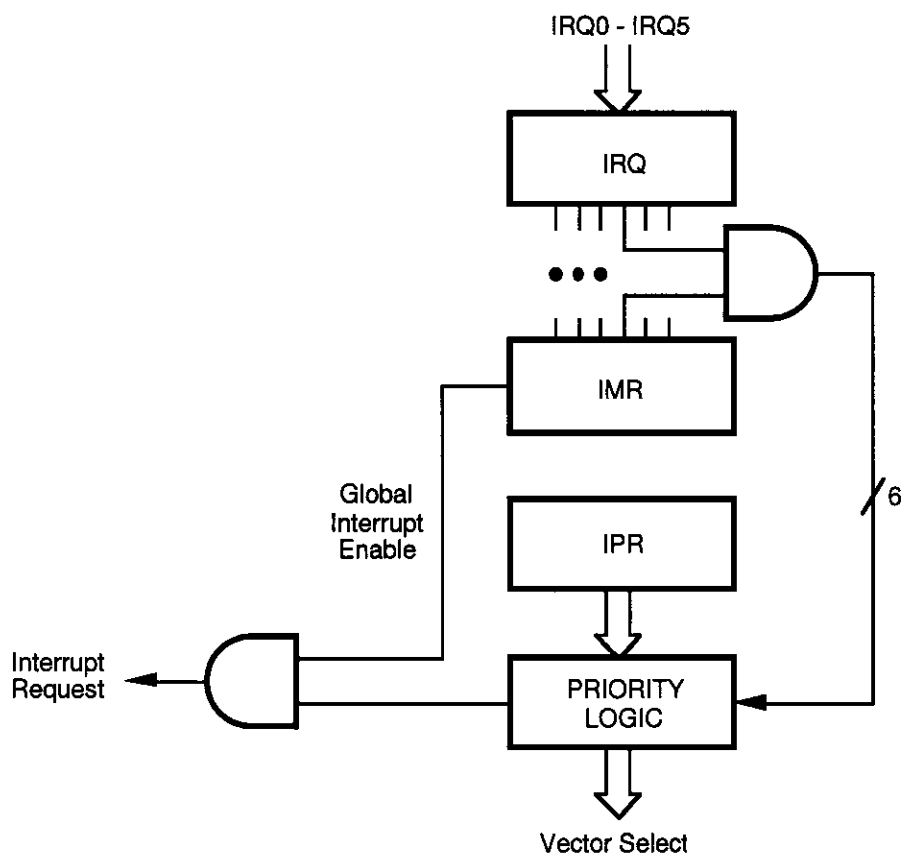
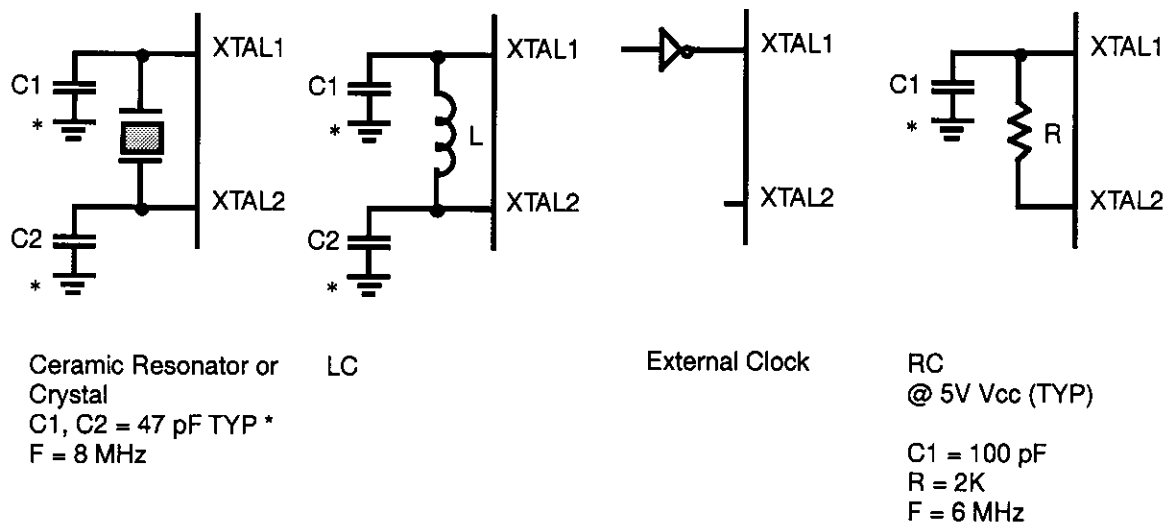


Figure 15. Interrupt Block Diagram

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS} , Pin 14 to reduce Ground noise injection.



* Typical value including pin parasitics

Figure 16. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

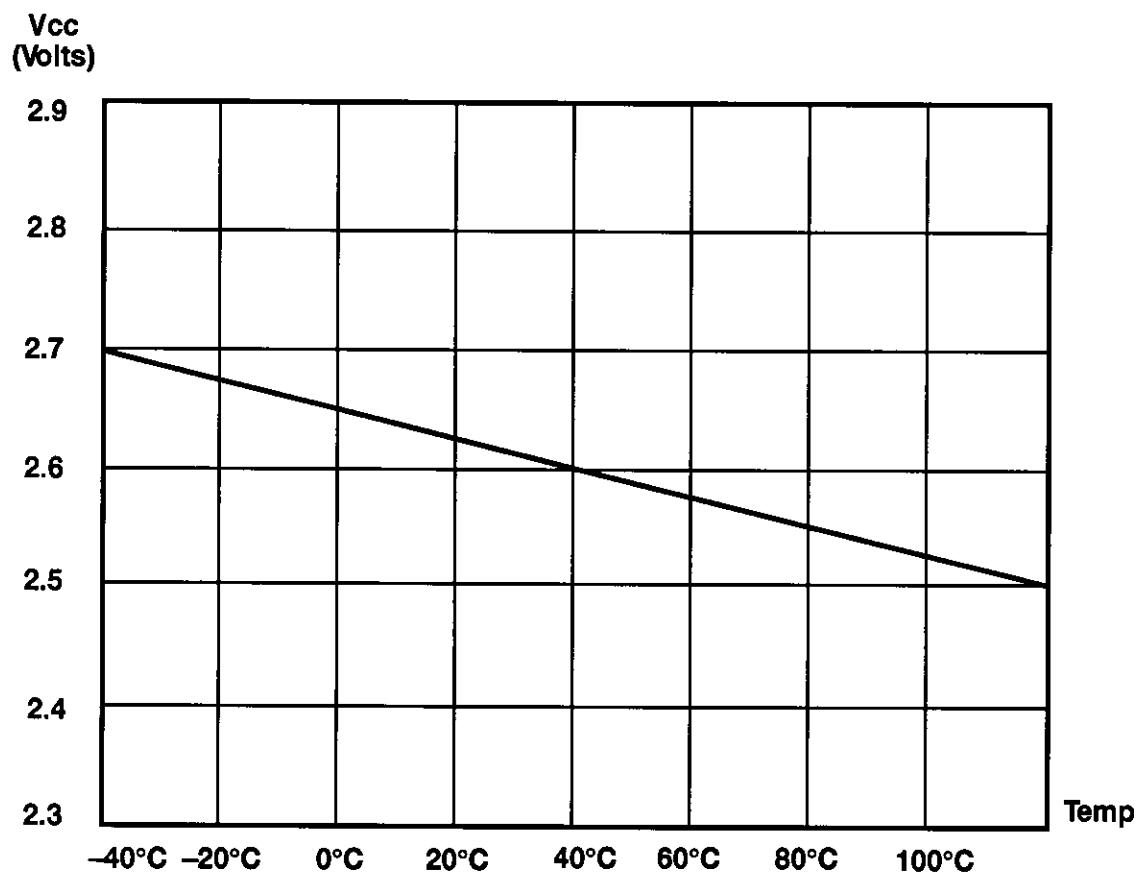
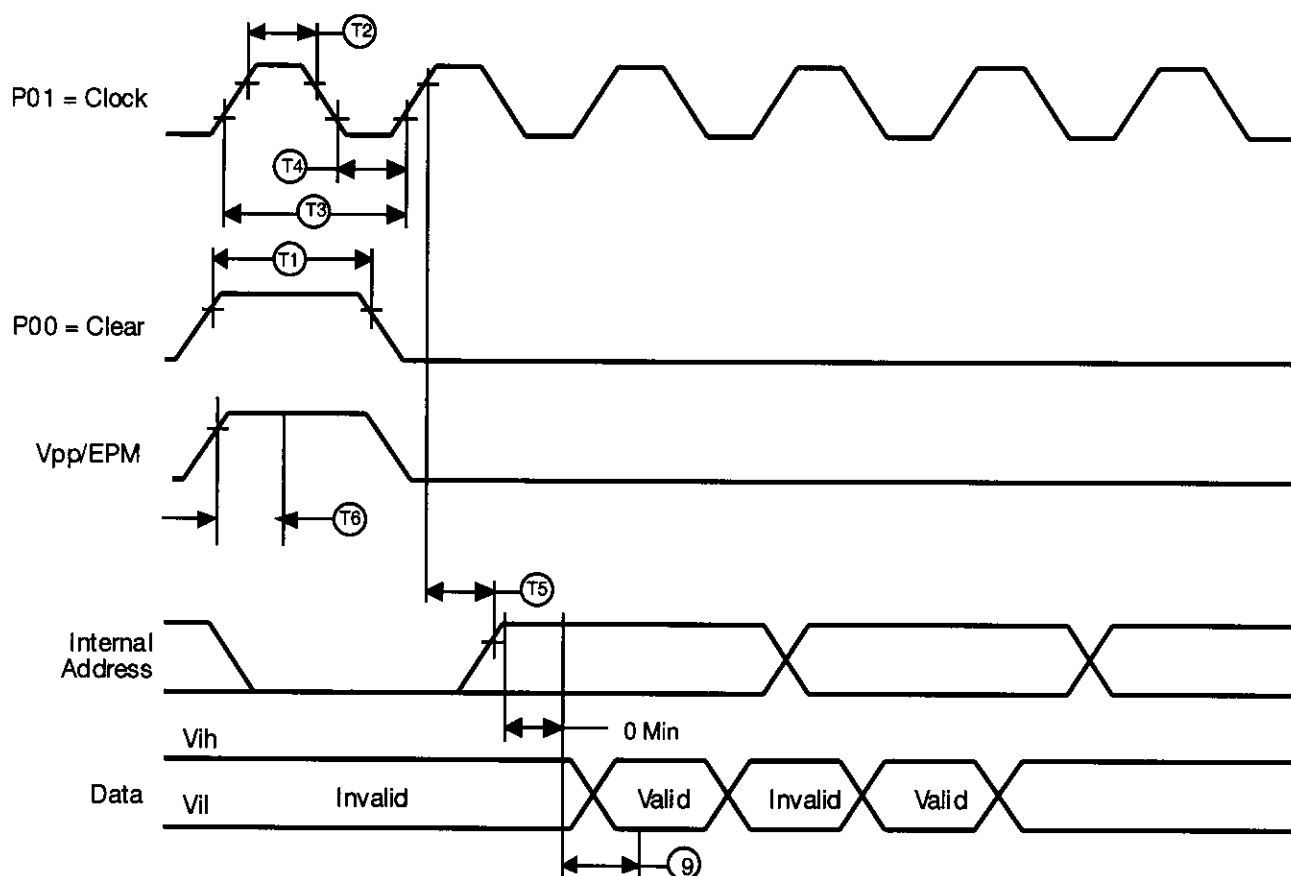


Figure 17. Typical Auto Reset Voltage
(V_{LV}) vs. Temperature



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 μ s Min

Figure 18. Z86E04/E08 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

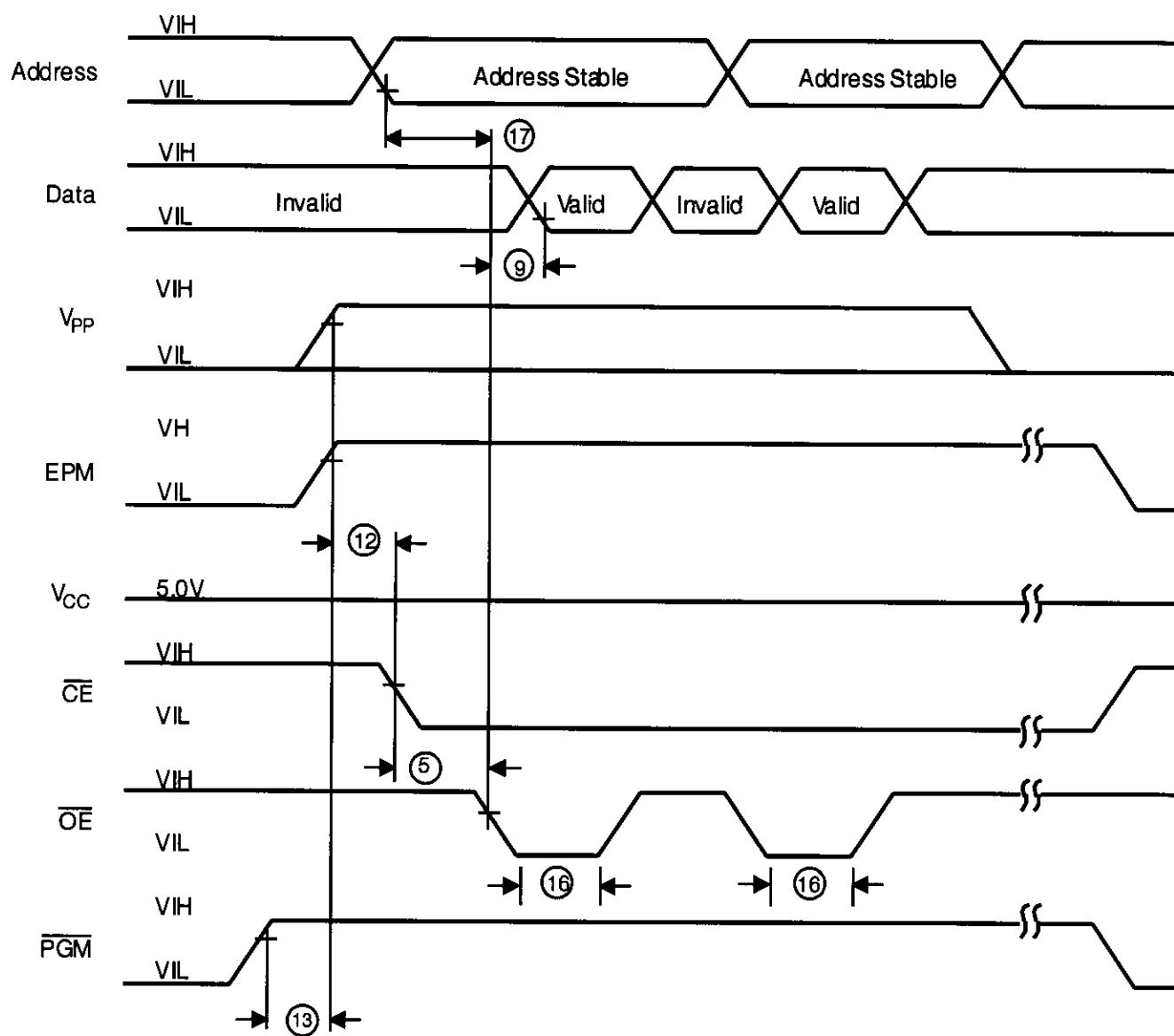


Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)

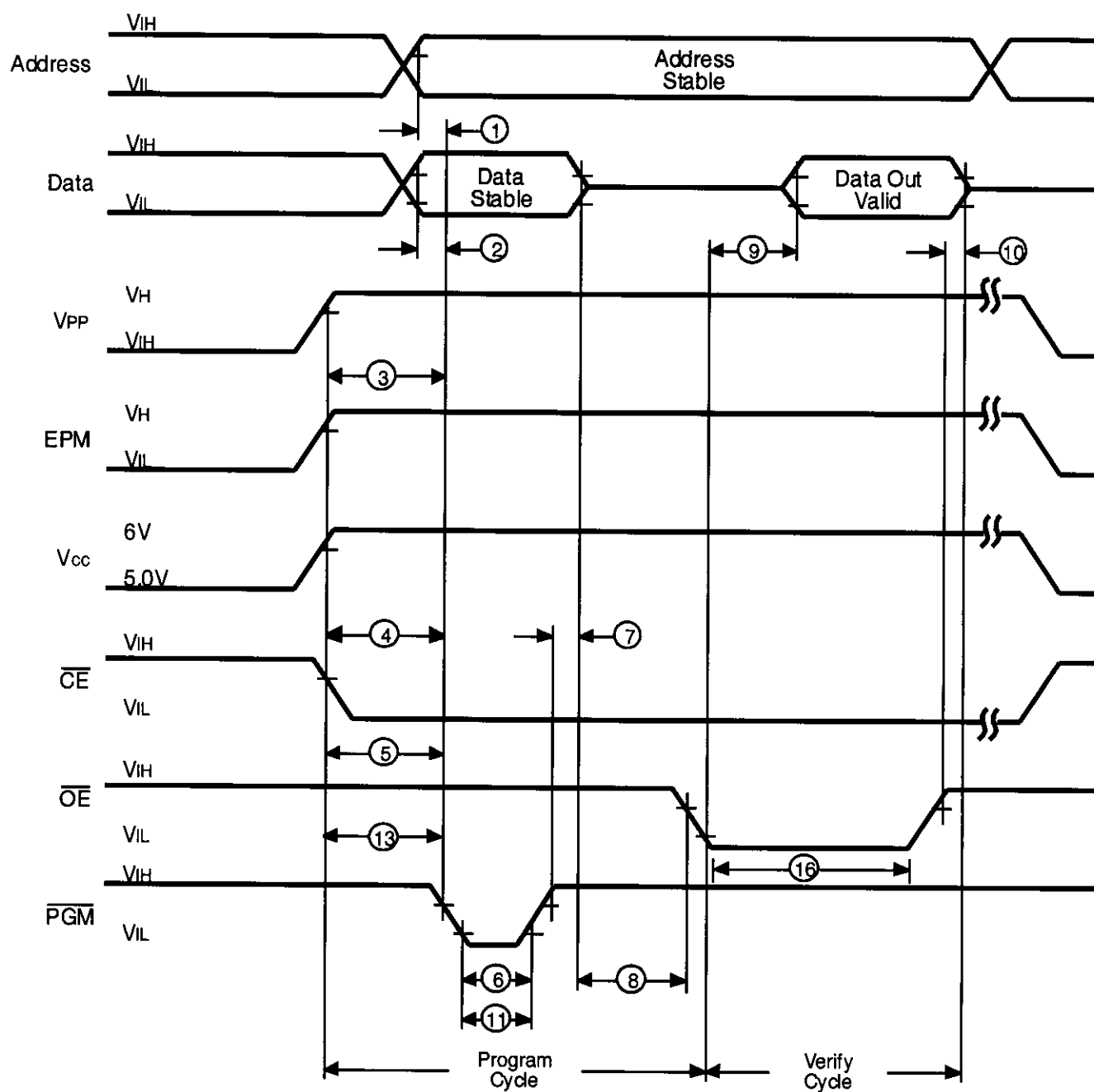


Figure 20. Z86E04/E08 Programming Waveform
(Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

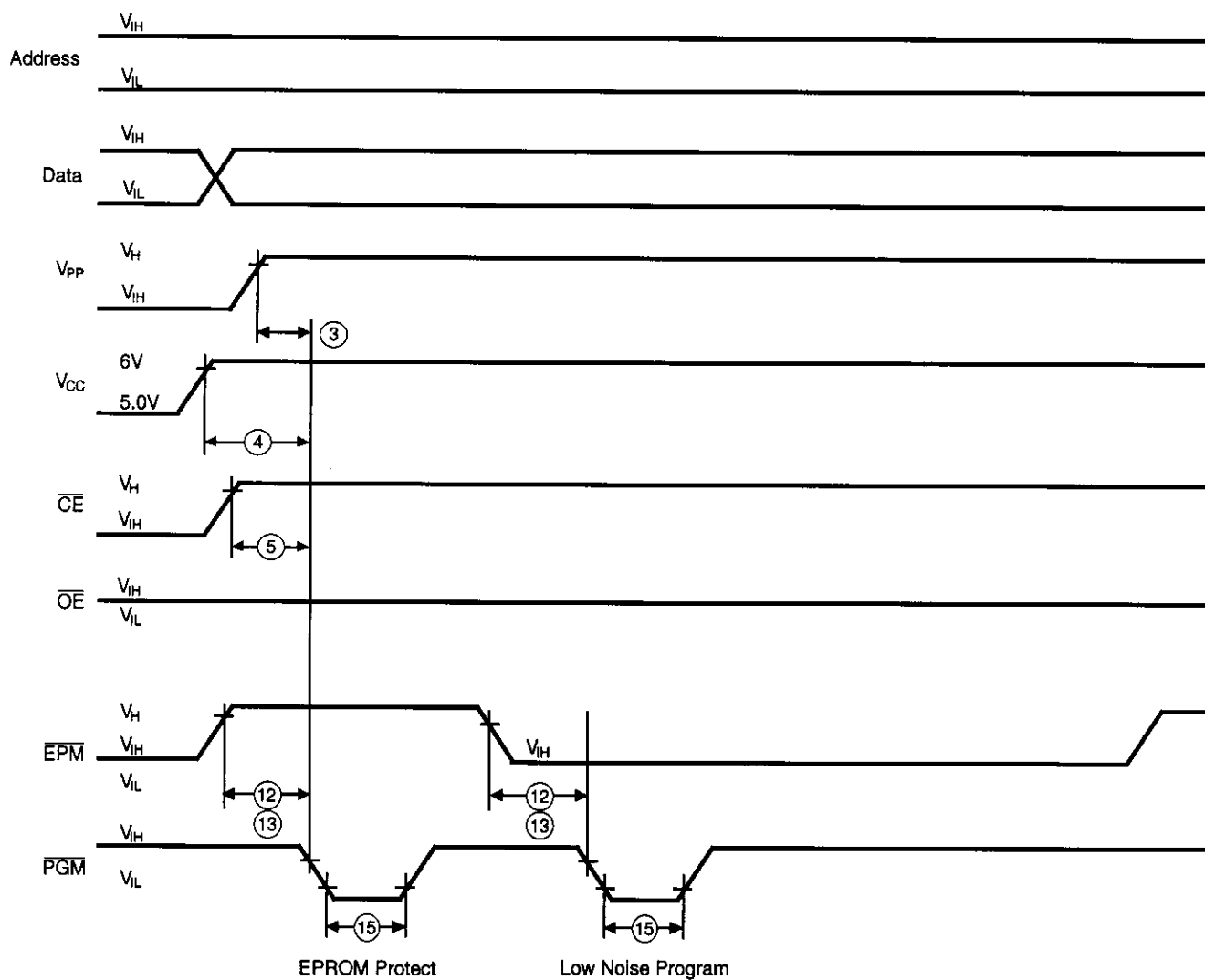
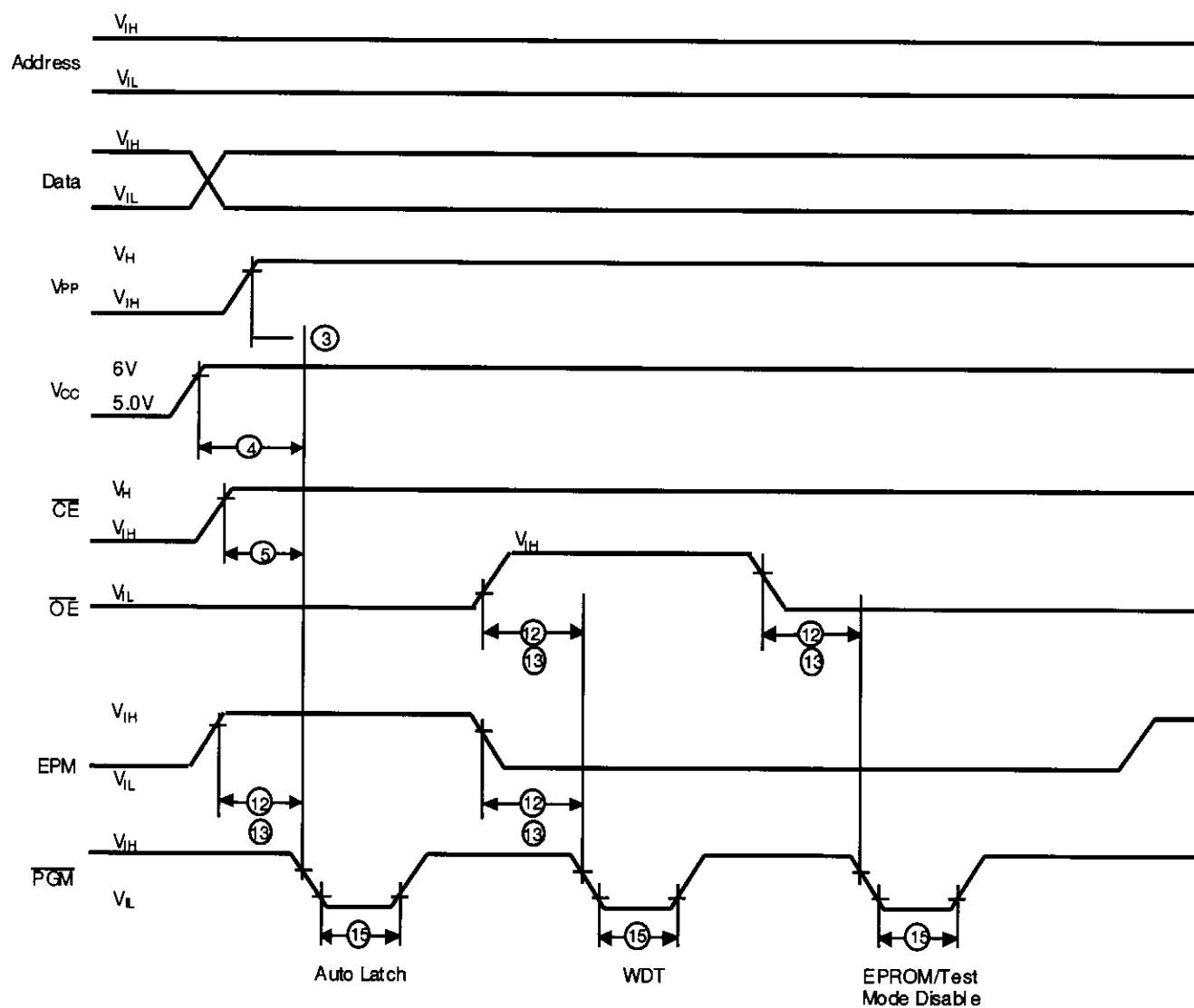


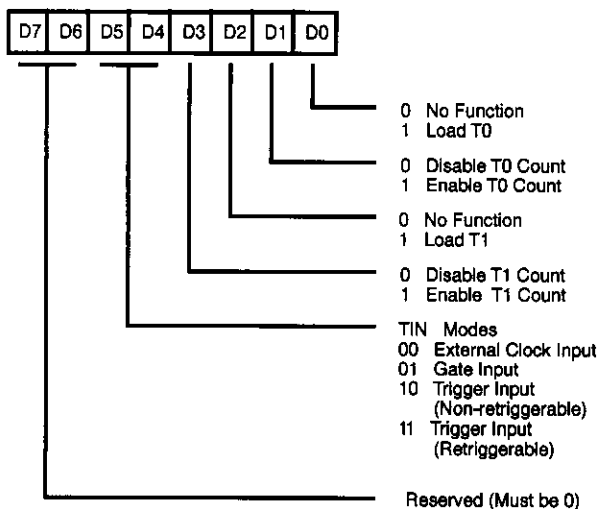
Figure 21. Z86E04/E08 Programming Options Waveform
(EPROM Protect and Low Noise Program)



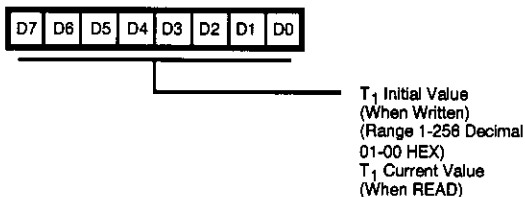
**Figure 22. Z86E04/E08 Programming Options Waveform
(Auto Latch Disable, Permanent WDT Enable and
EPROM/Test Mode Disable)**

Z8 CONTROL REGISTERS

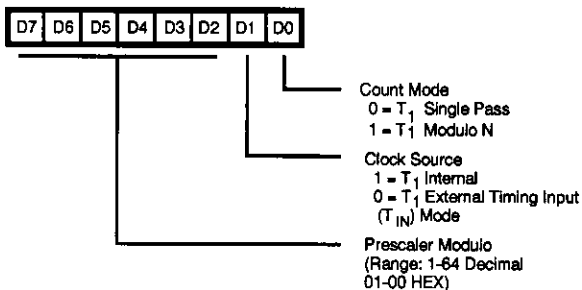
R241 TMR

Figure 24. Timer Mode Register (F1_H: Read/Write)

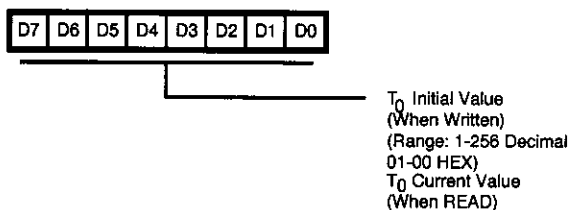
R242 T1

Figure 25. Counter Timer 1 Register (F2_H: Read/Write)

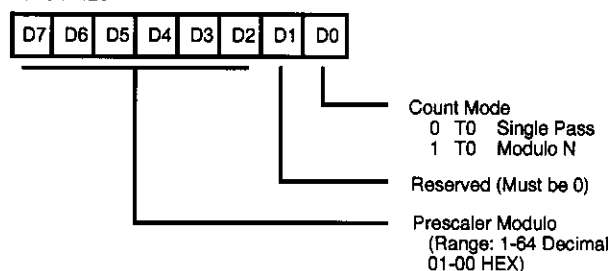
R243 PRE1

Figure 26. Prescaler 1 Register (F3_H: Write Only)

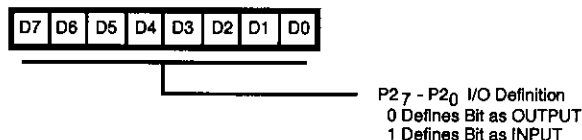
R244 T0

Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

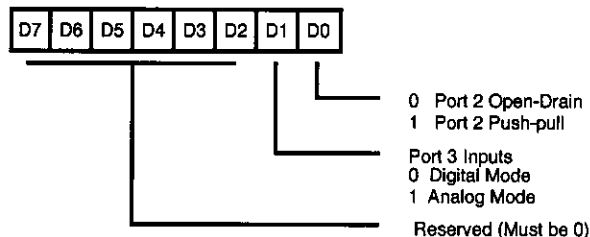
R245 PRE0

Figure 28. Prescaler 0 Register (F5_H: Write Only)

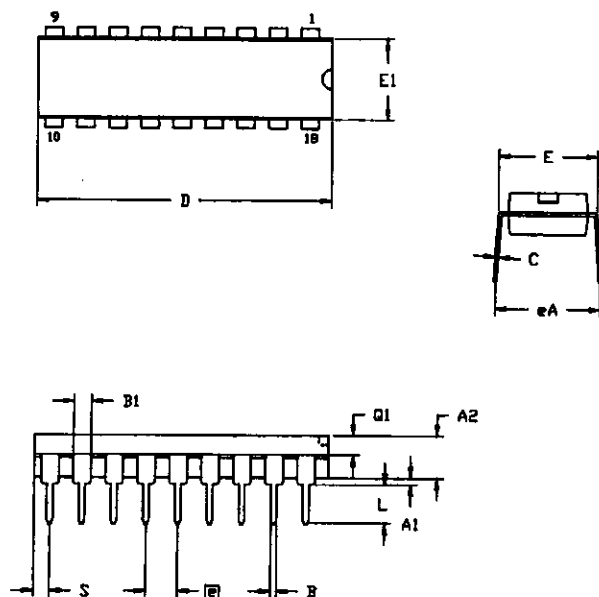
R246 P2M

Figure 29. Port 2 Mode Register (F6_H: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7_H: Write Only)

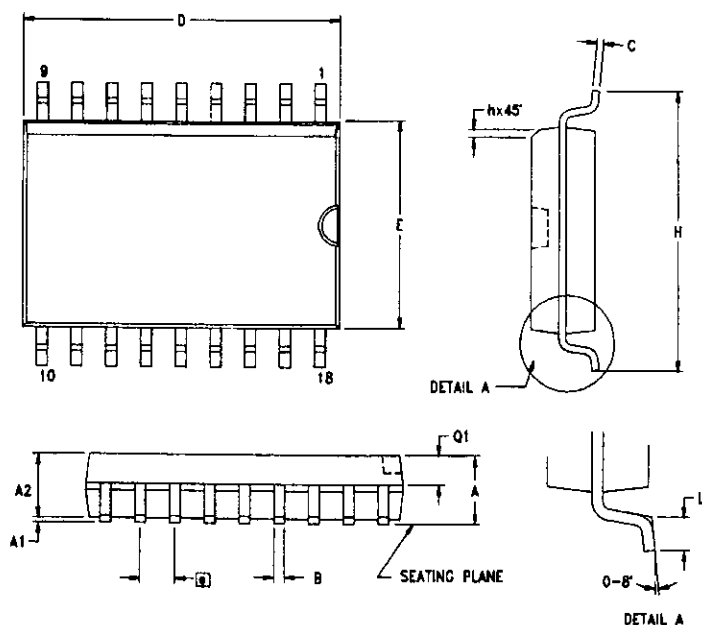
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram