Zilog - Z86E0412HSC1903 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0412hsc1903

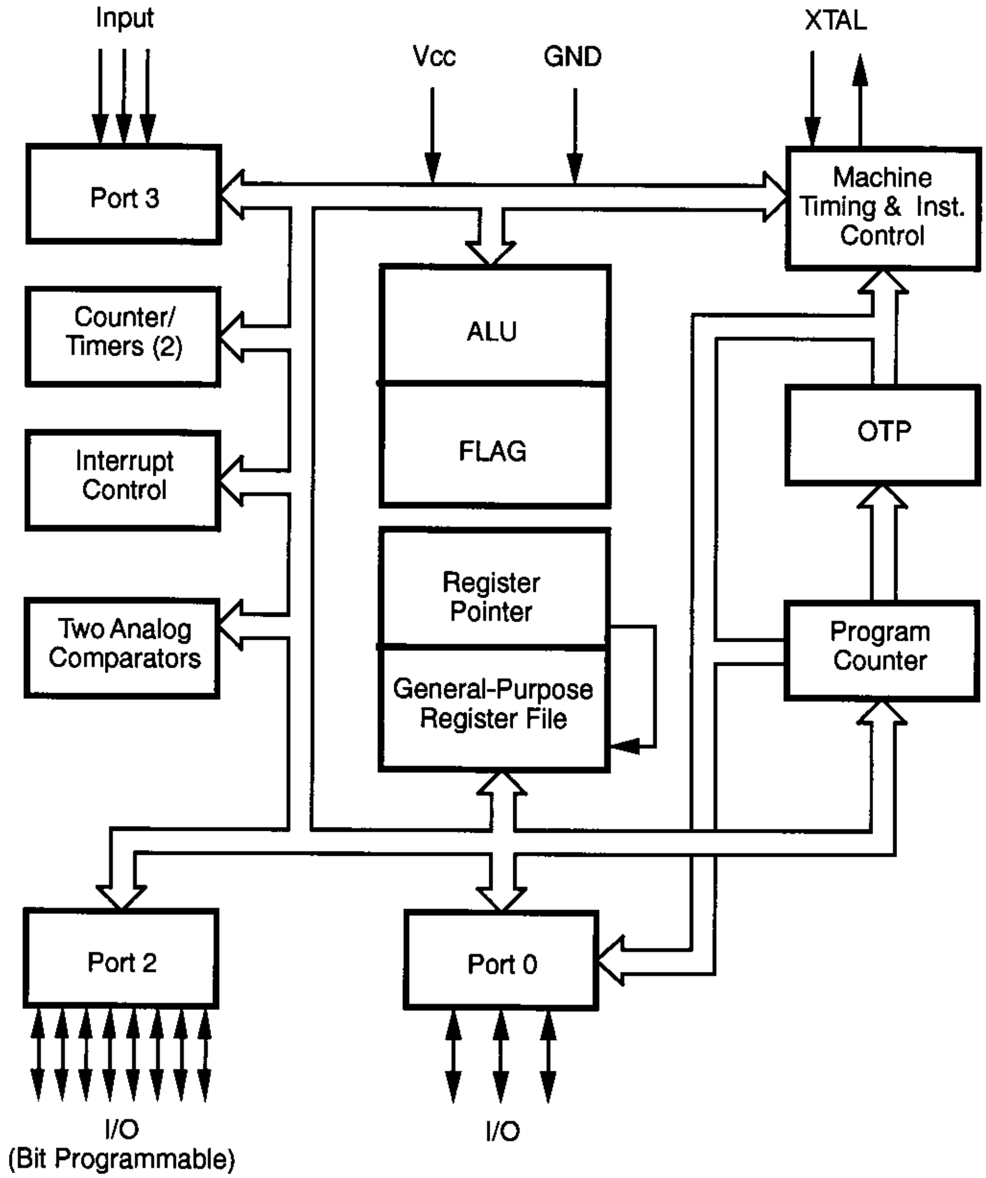


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION (Continued)

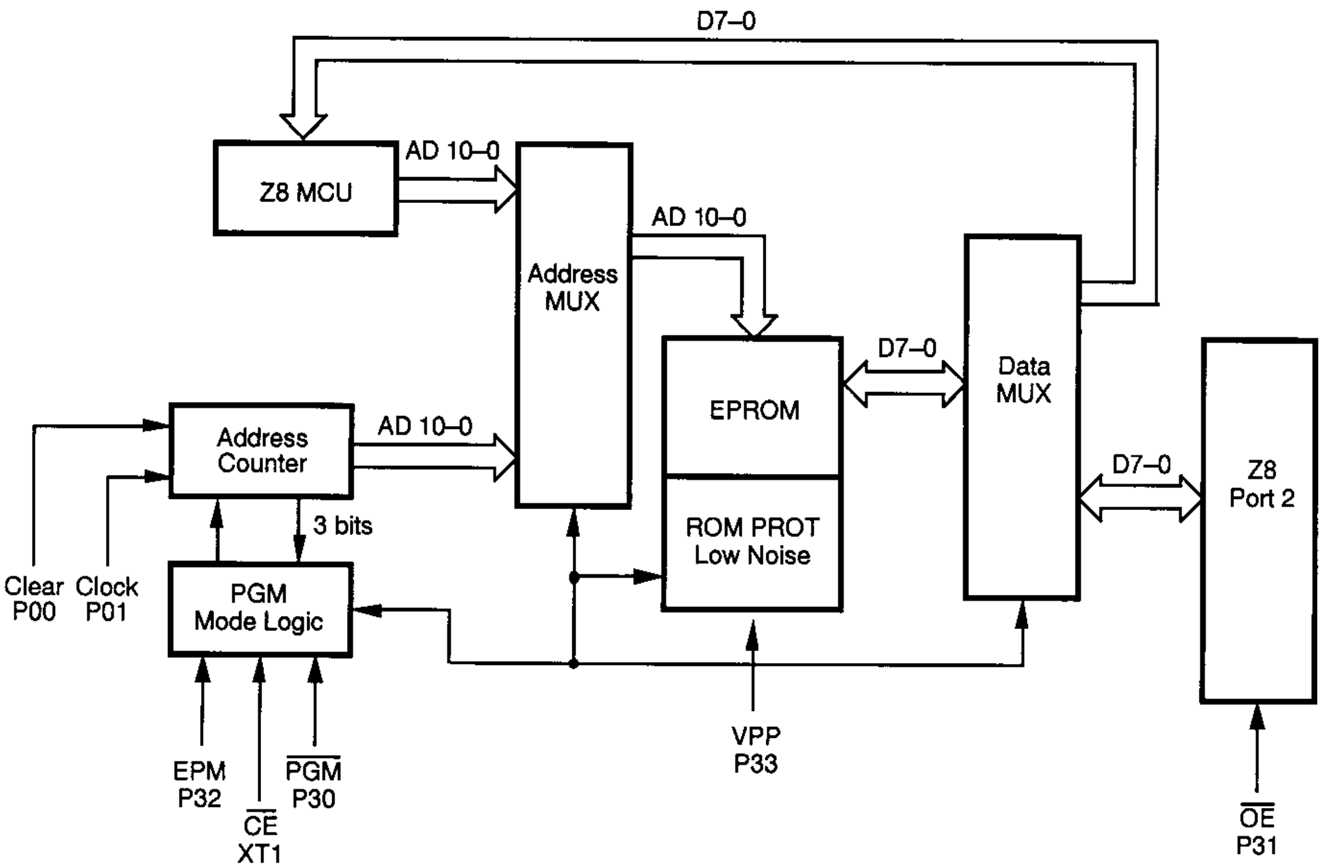


Figure 2. EPROM Programming Mode Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation = V_{DD} x [I_{DD}–(sum of I_{OH})]
+ sum of [(V_{DD}–V_{OH}) x I_{OH}]
+ sum of (V_{0L} x I_{0L})

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on Pins 7, 8, 9, 10 with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.65	W	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		220	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Total Maximum Output Current Sinked by a Port		60	mA	
Total Maximum Output Current Sourced by a Port		45	mA	

Notes:
1. This applies to all pins except where otherwise noted. Maximum current into pin must be ± 600 µA.
2. There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V,V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		32.0	16	µA	0V < V_{IN} < V_{CC}	
		5.5V		32.0	16	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	4.5V		–16.0	–8.0	µA	0V < V_{IN} < V_{CC}	
		5.5V		–16.0	–8.0	µA	0V < V_{IN} < V_{CC}	

Notes:
1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5 to 5.5V, typical values measured at V_{CC} = 5.0V.
   The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

DC ELECTRICAL CHARACTERISTICS
Extended Temperature

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{INMAX}	Max Input Voltage	4.5V		12.0		V	I_{IN} < 250 µA	1
		5.5V		12.0		V	I_{IN} < 250 µA	1
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		4.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I_{OL} = +12 mA,	5
		5.5V		1.0	0.3	V	I_{OL} = +12 mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} –1.5		V		

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS

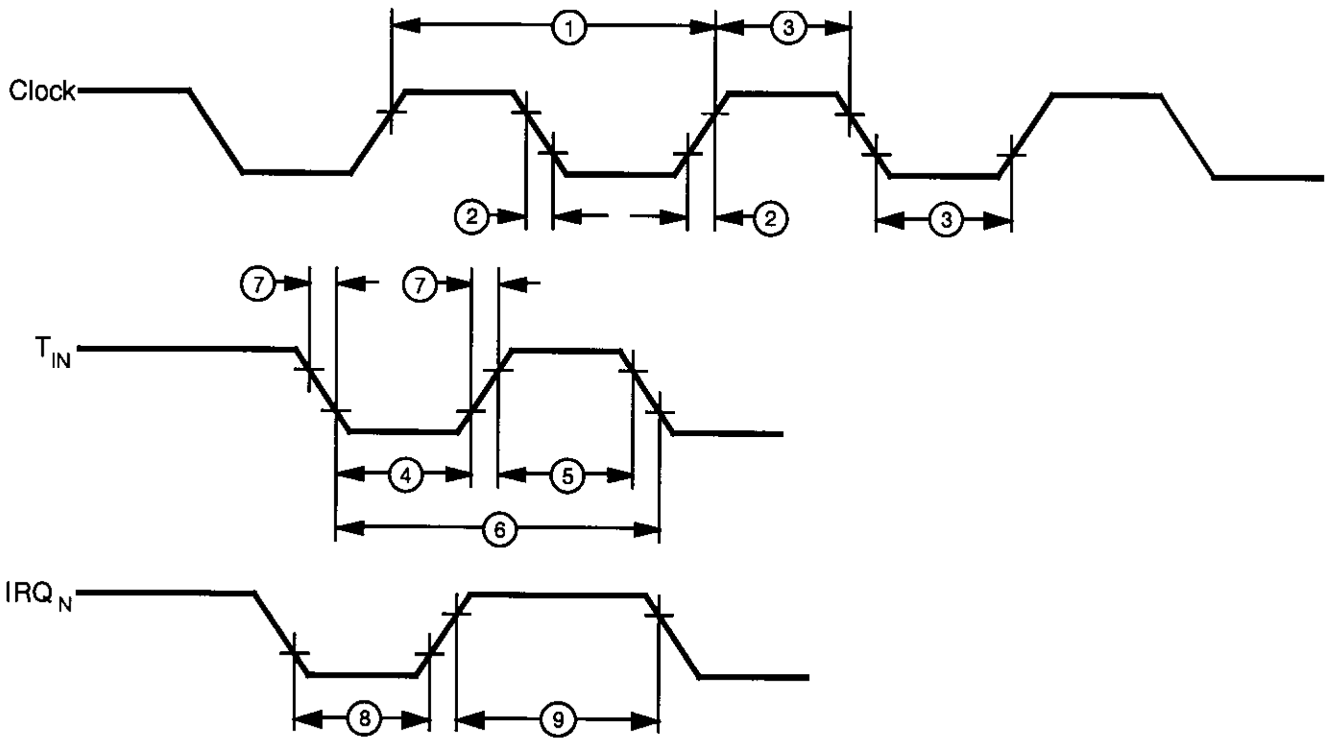


Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode, Standard Temperature

				T_A= 0 °C to +70 °C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

V_{CC} *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

$\overline{CE}$ *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

$\overline{PGM}$ *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the V_{PP}, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

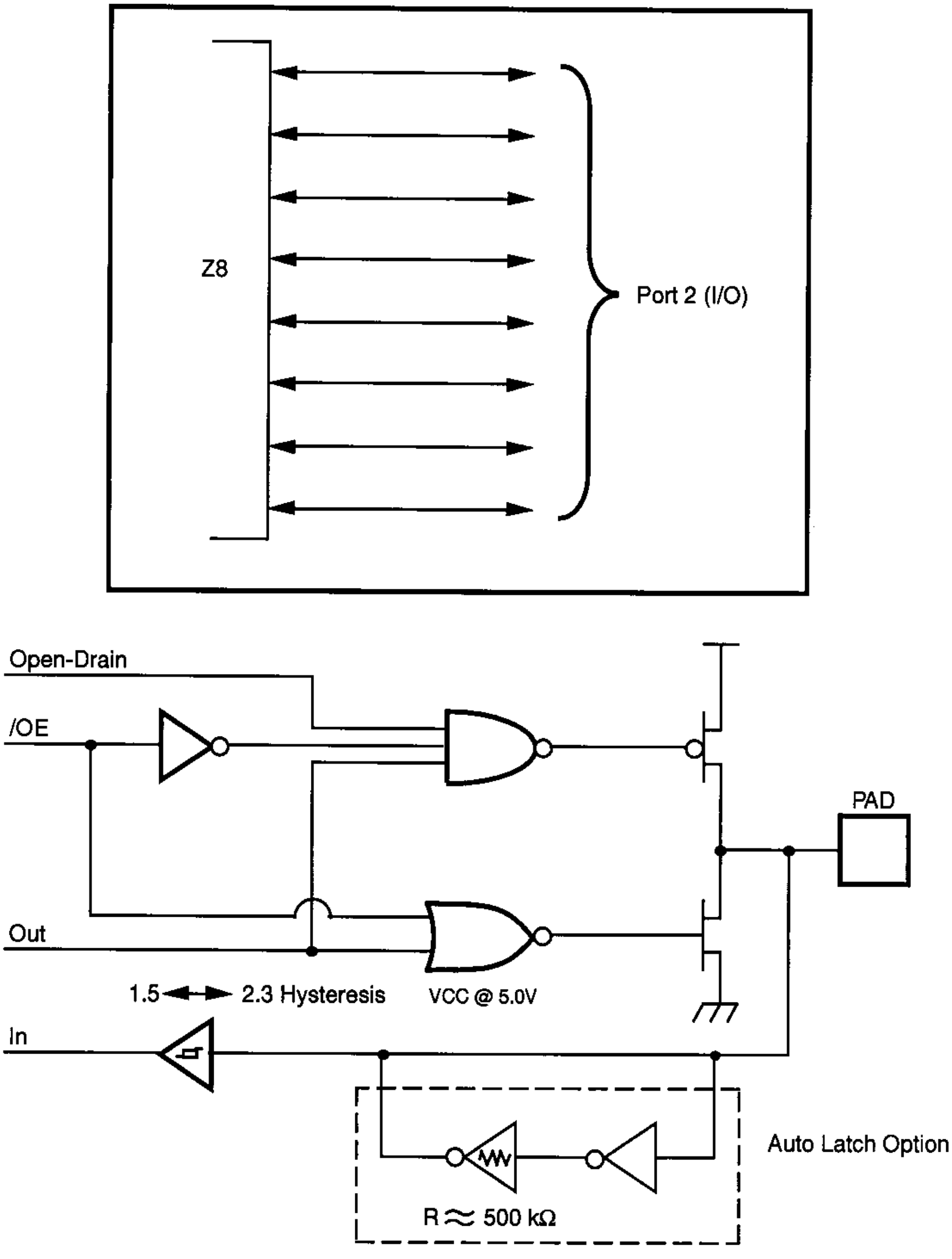


Figure 8. Port 2 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
V_{CC} = 5.0V @ 25°C

	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1µFd	
Resistor (R)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
V_{CC} = 3.3V @ 25°C

	Load Capacitor							
Resistor (R)	33 pFd		56 pFd		100 pFd		0.00 1µFd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

FUNCTIONAL DESCRIPTION (Continued)

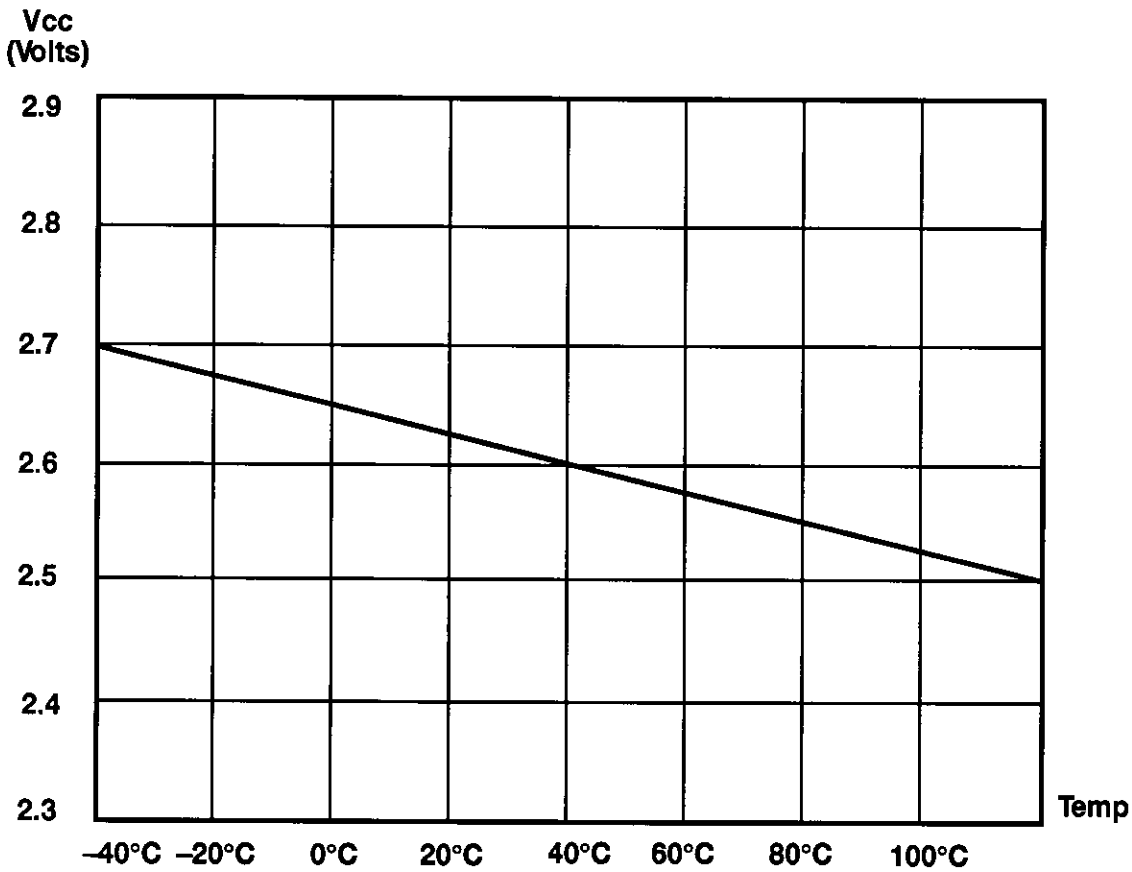


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

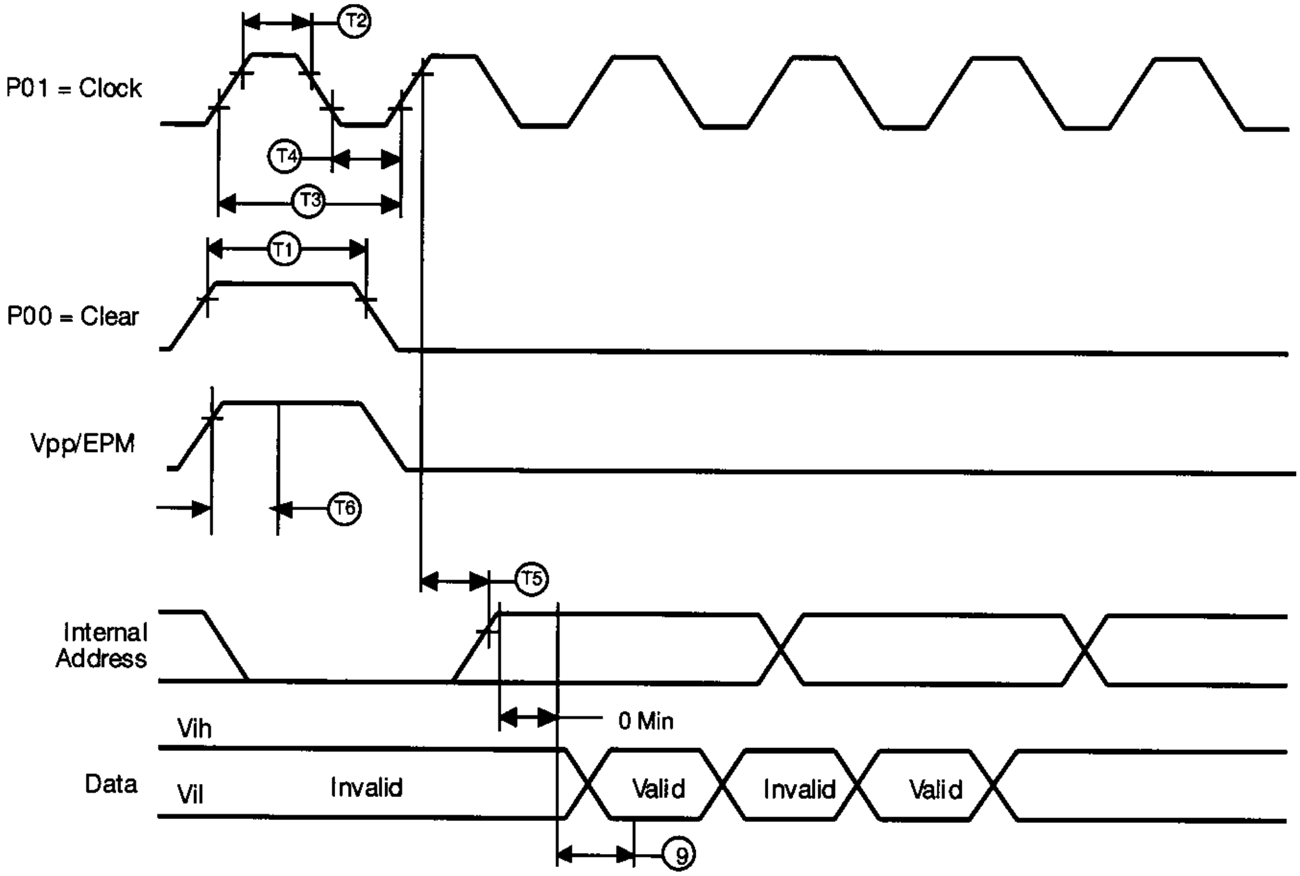
Internal Address Counter. The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

Programming Waveform. Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

Programming Algorithm. Figure 23 shows the flow chart of the Z8 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms
16	$\overline{OE}$ Width	250		ns
17	Address Valid to $\overline{OE}$ Low	125		ns



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 µs Min

Figure 18. Z86E04/E08 Address Counter Waveform

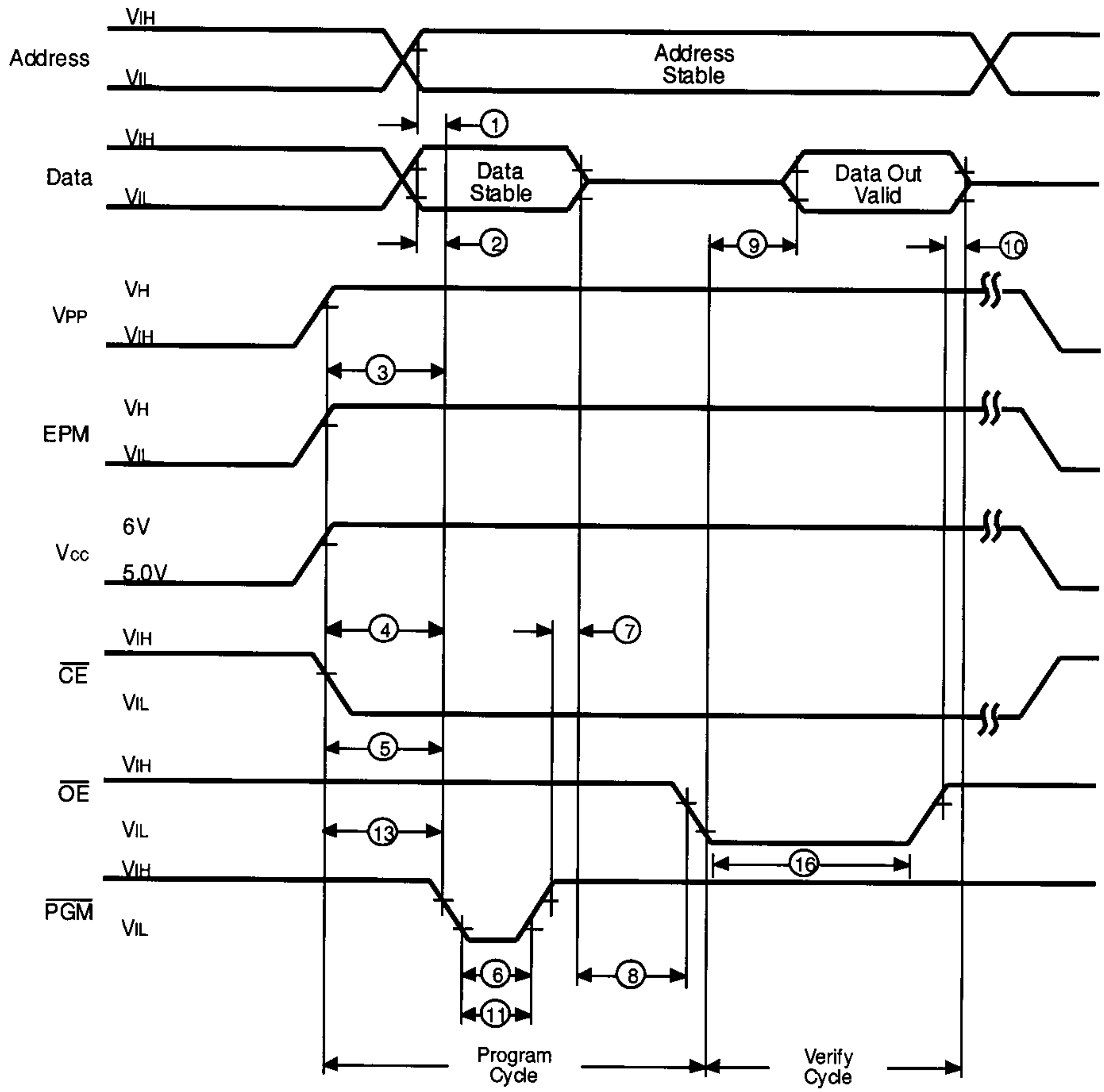


Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

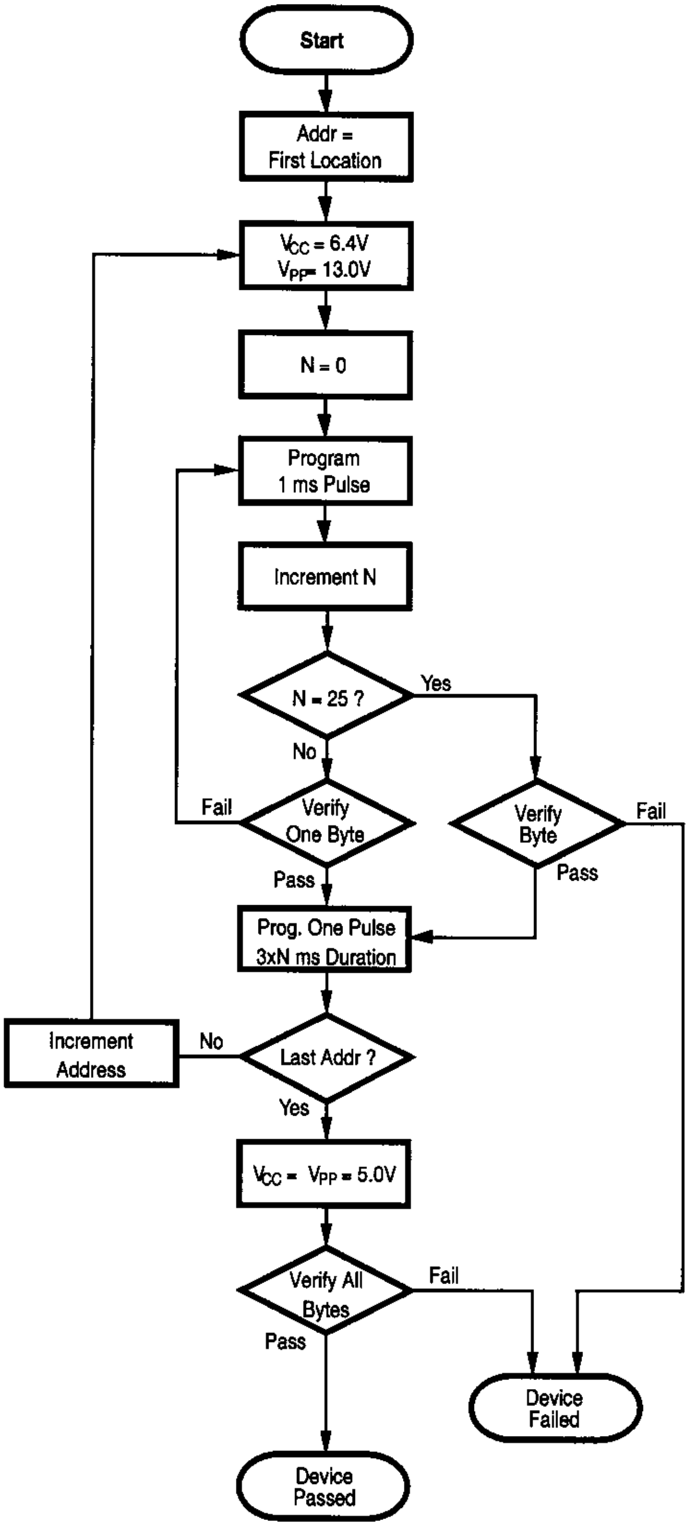
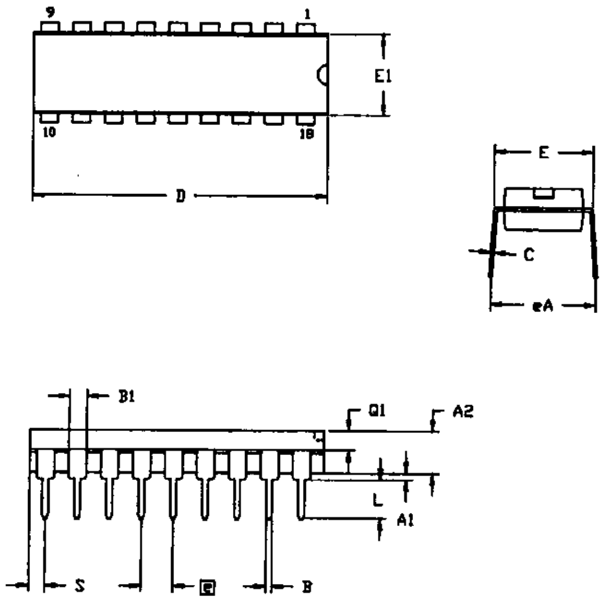


Figure 23. Z86E04/E08 Programming Algorithm

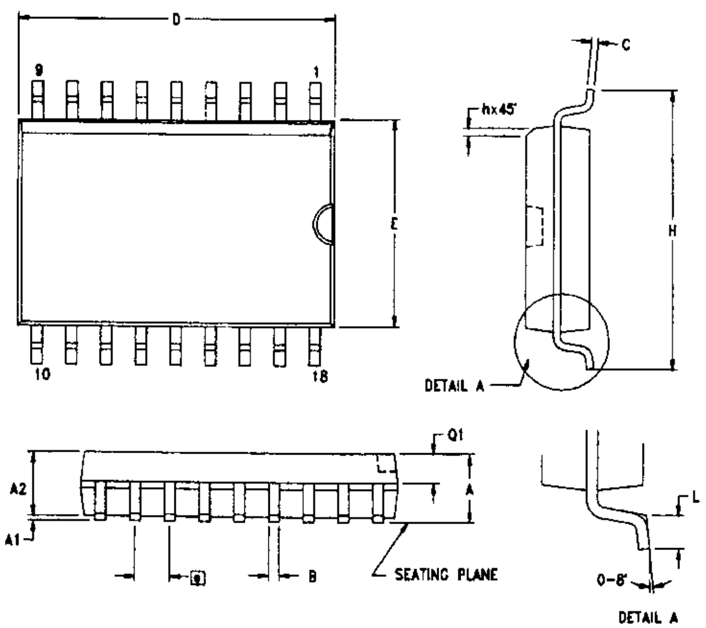
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com