What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

|	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0412psg1903
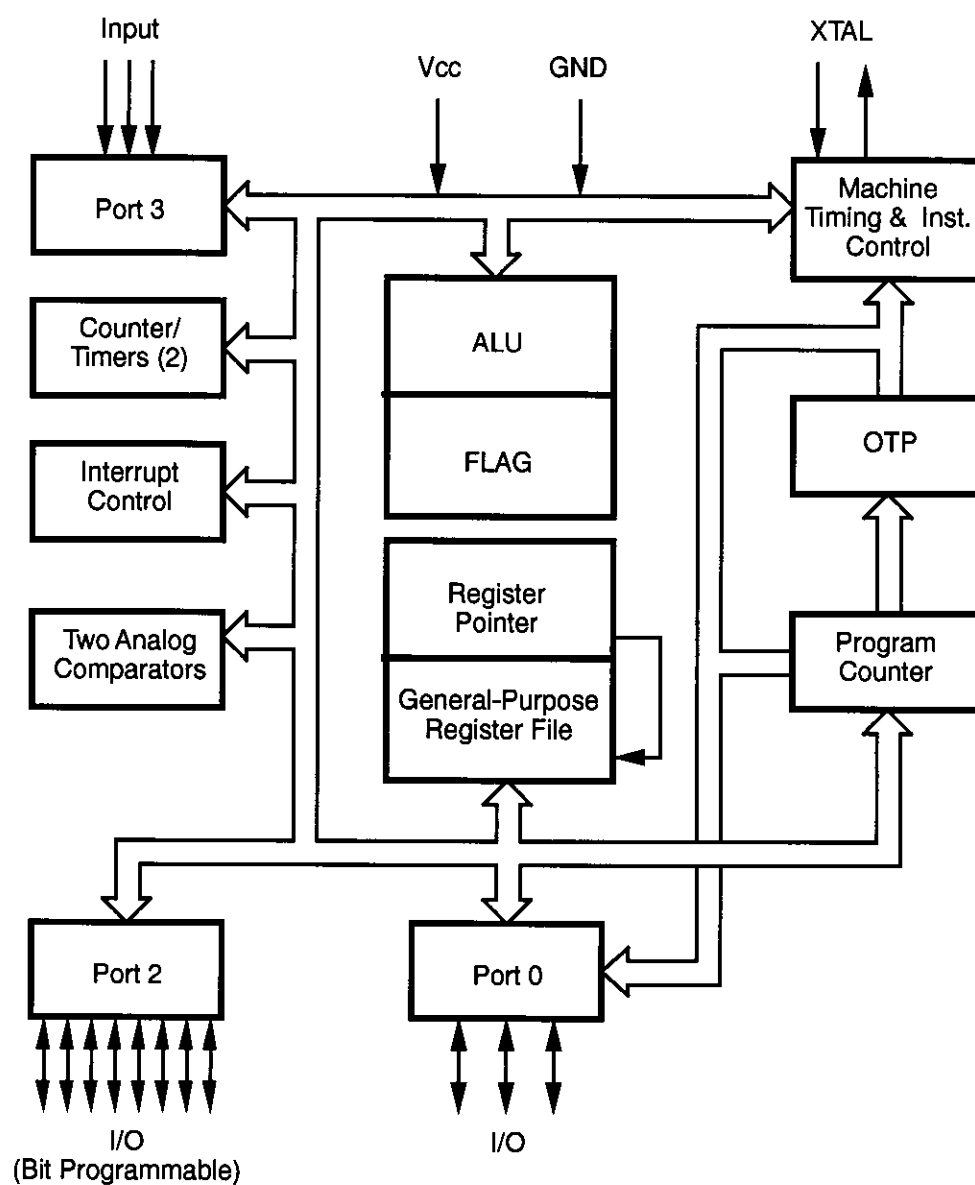
Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})]$$
$$+ \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}]$$
$$+ \text{sum of } (V_{0L} \times I_{0L})$$

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	−40	+105	C	
Storage Temperature	−65	+150	C	
Voltage on any Pin with Respect to V_{SS}	−0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	−0.3	+7	V	
Voltage on Pins 7, 8, 9, 10 with Respect to V_{SS}	−0.6	V_{DD}+1	V	2
Total Power Dissipation		1.65	W	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		220	mA	
Maximum Allowable Current into an Input Pin	−600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	−600	+600	µA	4
Maximum Allowable Output Current Sinked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Total Maximum Output Current Sinked by a Port		60	mA	
Total Maximum Output Current Sourced by a Port		45	mA	

Notes:
1. This applies to all pins except where otherwise noted. Maximum current into pin must be ± 600 µA.
2. There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

DC ELECTRICAL CHARACTERISTICS
Standard Temperature

Sym	Parameter	V_{CC} [4]	$T_A = 0°C$ to $+70°C$ Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{INMAX}	Max Input Voltage	4.5V		12		V	I_{in}<250 µA	1
		5.5V		12		V	I_{in}<250 µA	1
V_{CH}	Clock Input High Voltage	4.5V	$0.8\,V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
		5.5V	$0.8\,V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2\,V_{CC}$	1.7	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2\,V_{CC}$	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7\,V_{CC}$	$V_{CC}+0.3$	2.8	V		
		5.5V	$0.7\,V_{CC}$	$V_{CC}+0.3$	2.8	V		
V_{IL}	Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2\,V_{CC}$	1.5	V		
		5.5V	$V_{SS}-0.3$	$0.2\,V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		4.5V	$V_{CC}-0.4$		4.8	V	Low Noise @ $I_{OH} = -0.5$ mA	
		5.5V	$V_{CC}-0.4$		4.8	V	Low Noise @ $I_{OH} = -0.5$ mA	
V_{OL1}	Output Low Voltage	4.5V		0.8	0.1	V	$I_{OL} = +4.0$ mA	5
		5.5V		0.4	0.1	V	$I_{OL} = +4.0$ mA	5
		4.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
		5.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
V_{OL2}	Output Low Voltage	4.5V		0.8	0.8	V	$I_{OL} = +12$ mA,	5
		5.5V		0.8	0.8	V	$I_{OL} = +12$ mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.2	3.0	2.8	V	@ 6 MHz Max. Int. CLK Freq.	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	-1.0	1.0		µA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1.0	1.0		µA	$V_{IN} = 0V, V_{CC}$	
I_{OL}	Output Leakage	4.5V	-1.0	1.0		µA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1.0	1.0		µA	$V_{IN} = 0V, V_{CC}$	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	$V_{CC}-1.0$		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	$T_A = 0°C$ to $+70°C$		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		10.0	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{CC} WDT is not Running	7,8
		5.5V		10.0	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		−16.0	−8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		−16.0	−8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Port 2 and Port 0 only
2. $V_{SS} = 0V = GND$
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. $V_{CC} = 4.5$ to 5.5V, typical values measured at $V_{CC} = 5.0V$.
   The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at $V_{CC} = 5.0V$.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C					
				8 MHz		**12 MHz**			
No	**Symbol**	**Parameter**	V_{CC}	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Extended Temperature

No	Symbol	Parameter	V_{CC}	8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1
11	Tpor	Power-On Reset Time	4.5V	12	100	12	100	ms	1
			5.5V	12	100	12	100	ms	1

T_A = –40 °C to +105 °C

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode, Standard Temperature

| No | Symbol | Parameter | V_{CC} | $T_A= 0$ °C to +70 °C | | | | Units | Notes |
| | | | | 1 MHz | | 4 MHz | | | |
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

No	Symbol	Parameter	V_{CC}	1 MHz Min	1 MHz Max	4 MHz Min	4 MHz Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V		4TpC	4TpC			1
			5.5V		4TpC	4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

■ All pre-driver slew rates reduced to 10 ns typical.

■ Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

■ Output drivers have resistances of 500 Ohms (typical).

■ Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

V_{CC} V_{CC} *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

OE *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

PGM *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if *excessive noise* surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by *excessive noise* surges on the V_{PP}, CE, EPM, OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

■ Using a clamping diode to V_{CC}.

■ Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).
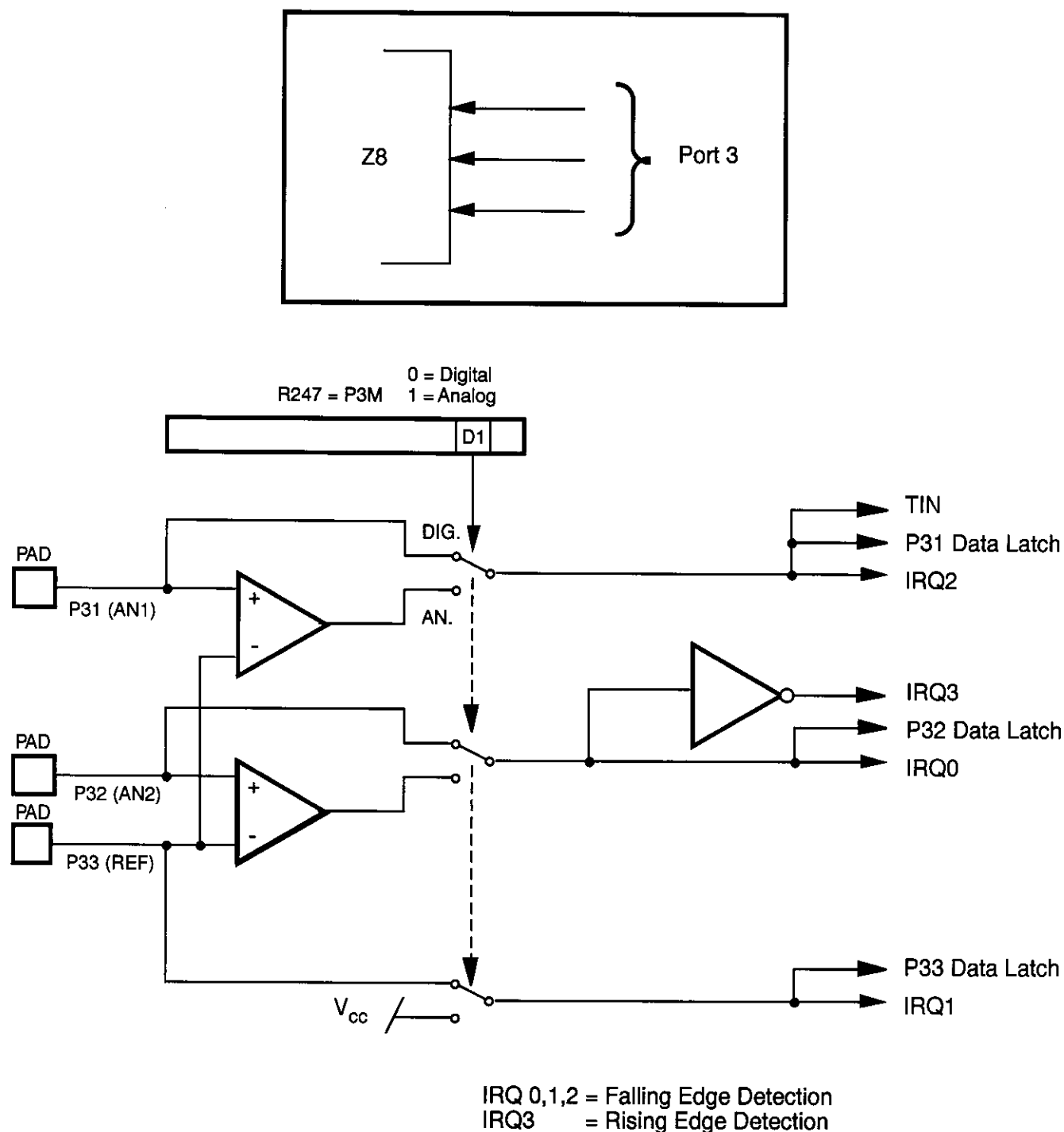

Figure 9. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

Addr.	Reg.	D7	D6	D5	D4	D3	D2	D1	D0	Comments
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.
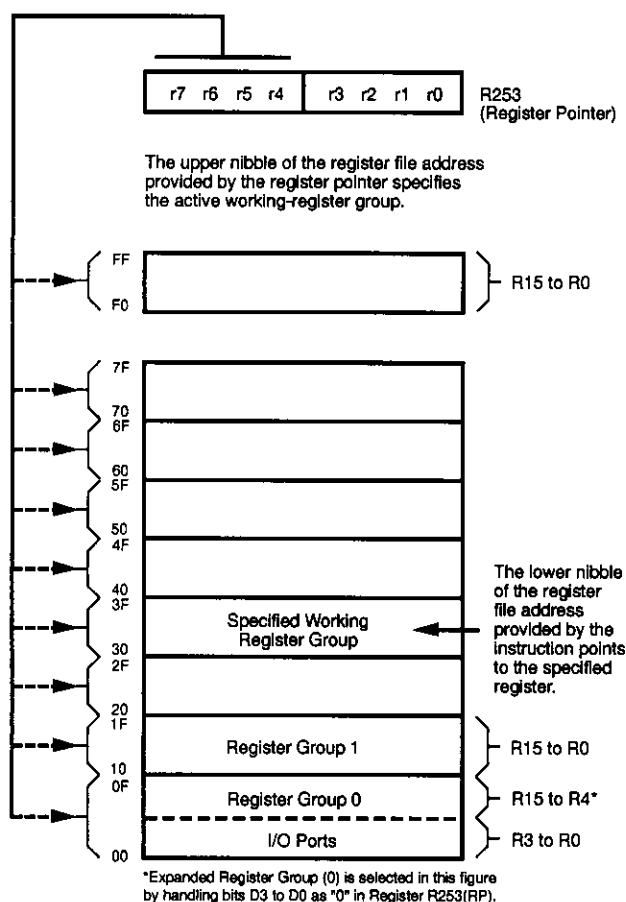

Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
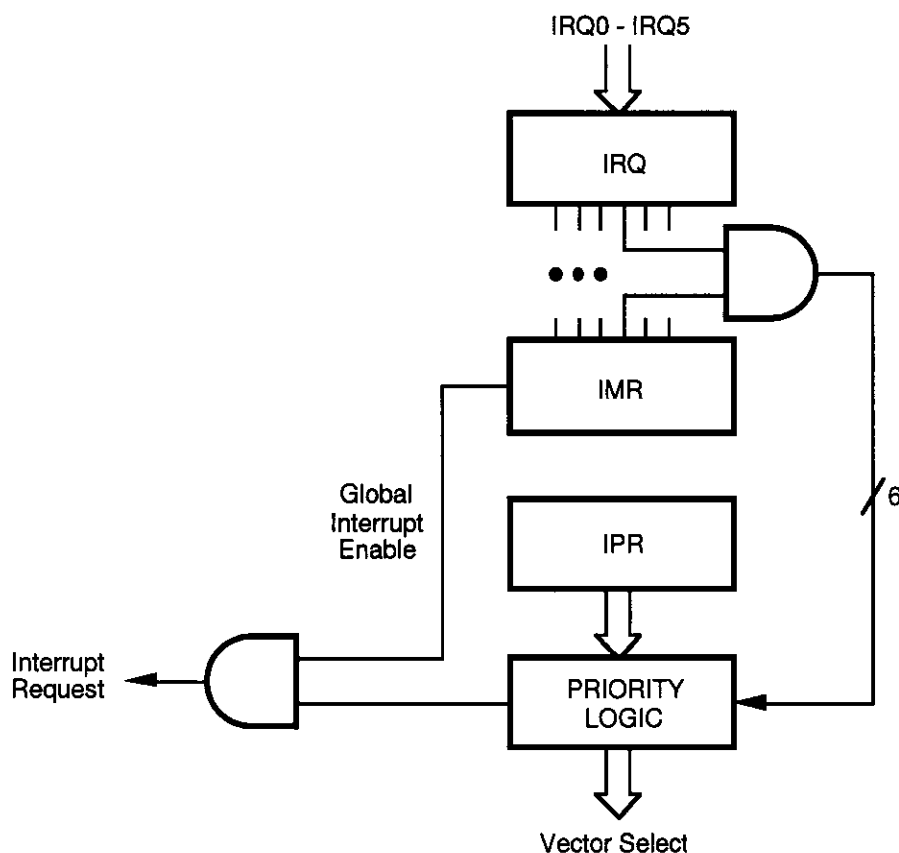F = Falling edge triggered
R = Rising edge triggered

Figure 15. Interrupt Block Diagram

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD              P2M, #1XXX XXXXB
NOP
STOP
```

    X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
            or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

    WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}.

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.
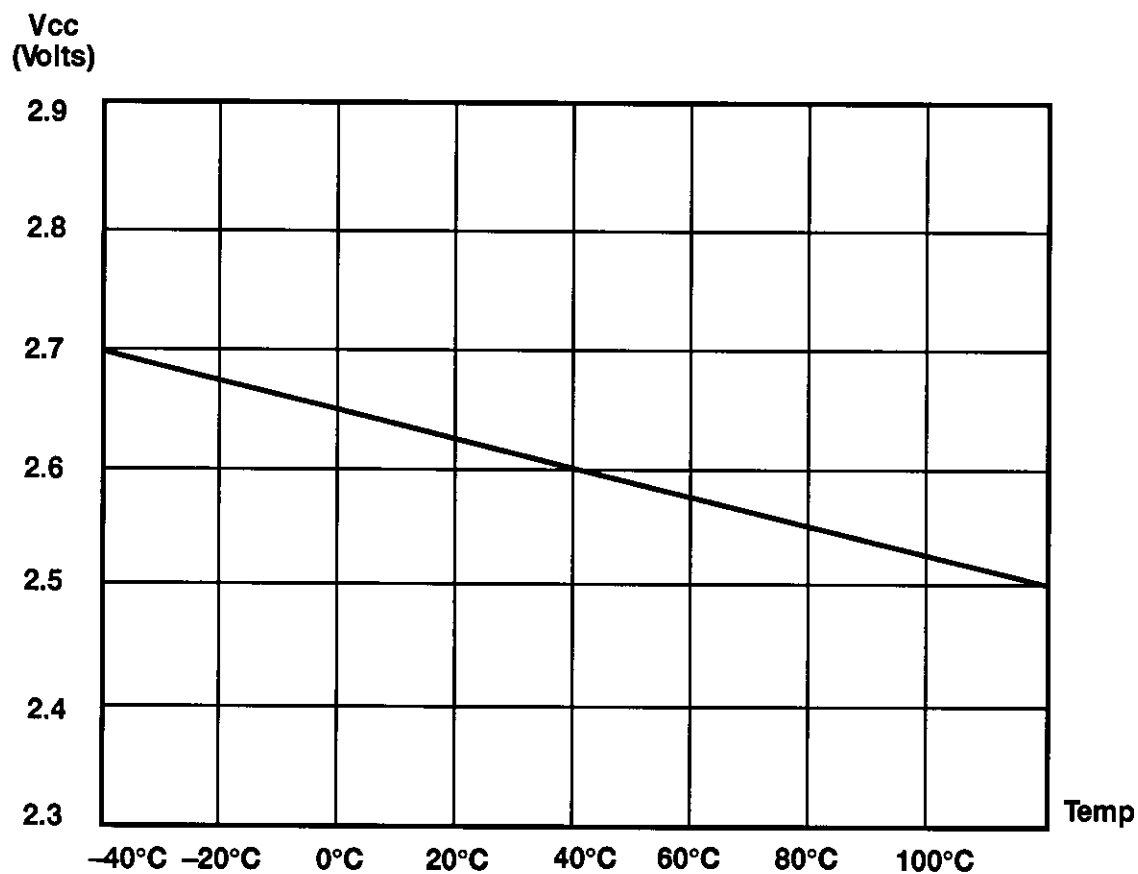
FUNCTIONAL DESCRIPTION (Continued)

Figure 17. Typical Auto Reset Voltage
(V_{LV}) vs. Temperature

Low EMI Emission

The Z8 can be programmed to operate in a low EMI Emission (Low Noise) Mode by means of an EPROM programmable bit option. Use of this feature results in:

■ Less than 1 mA consumed during HALT Mode.

■ All drivers slew rates reduced to 10 ns (typical).

■ Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time.

■ Output drivers have resistances of 500 ohms (typical).

■ Oscillator divide-by-two circuitry eliminated.

In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM Mode. XTAL2 has no function, XTAL1 functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as $\overline{PGM}$.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI **are supported** (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will not automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and $\overline{CE}$ pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP Mode. The V_{PP} requires both a diode and a 100 pF capacitor.

Auto Latch Disable. Auto Latch Disable option bit when programmed will globally disable all Auto Latches.

WDT Enable. The WDT Enable option bit, when programmed, will have the hardware enabled Permanent WDT enabled after exiting reset and can not be stopped in Halt or Stop Mode.

EPROM/Test Mode Disable. The EPROM/Test Mode Disable option bit, when programmed, will disable the EPROM Mode and the Factory Test Mode. Reading, verifying, and programming the Z8 will be disabled. To fully verify that this mode is disabled, the device must be power cycled.

User Modes. Table 7 shows the programming voltage of each mode.

Table 7. OTP Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ	NU	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.0V
PROGRAM	V_H	V_{IH}	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_{IH}	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.4V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
AUTO LATCH DISABLE	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V
WDT ENABLE	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
EPROM/TEST MODE	V_H	V_{IL}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V

Notes:
1. V_H =12.75V ± 0.25 V_{DC} .
2. V_{IH} = As per specific Z8 DC specification.
3. V_{IL} = As per specific Z8 DC specification.
4. X = Not used, but must be set to V_H or V_{IH} level.
5. NU = Not used, but must be set to either V_{IH} or V_{IL} level.
6. I_{PP} during programming = 40 mA maximum.
7. I_{CC} during programming, verify, or read = 40 mA maximum.
8. * V_{CC} has a tolerance of ±0.25V.

Figure 18. Z86E04/E08 Address Counter Waveform
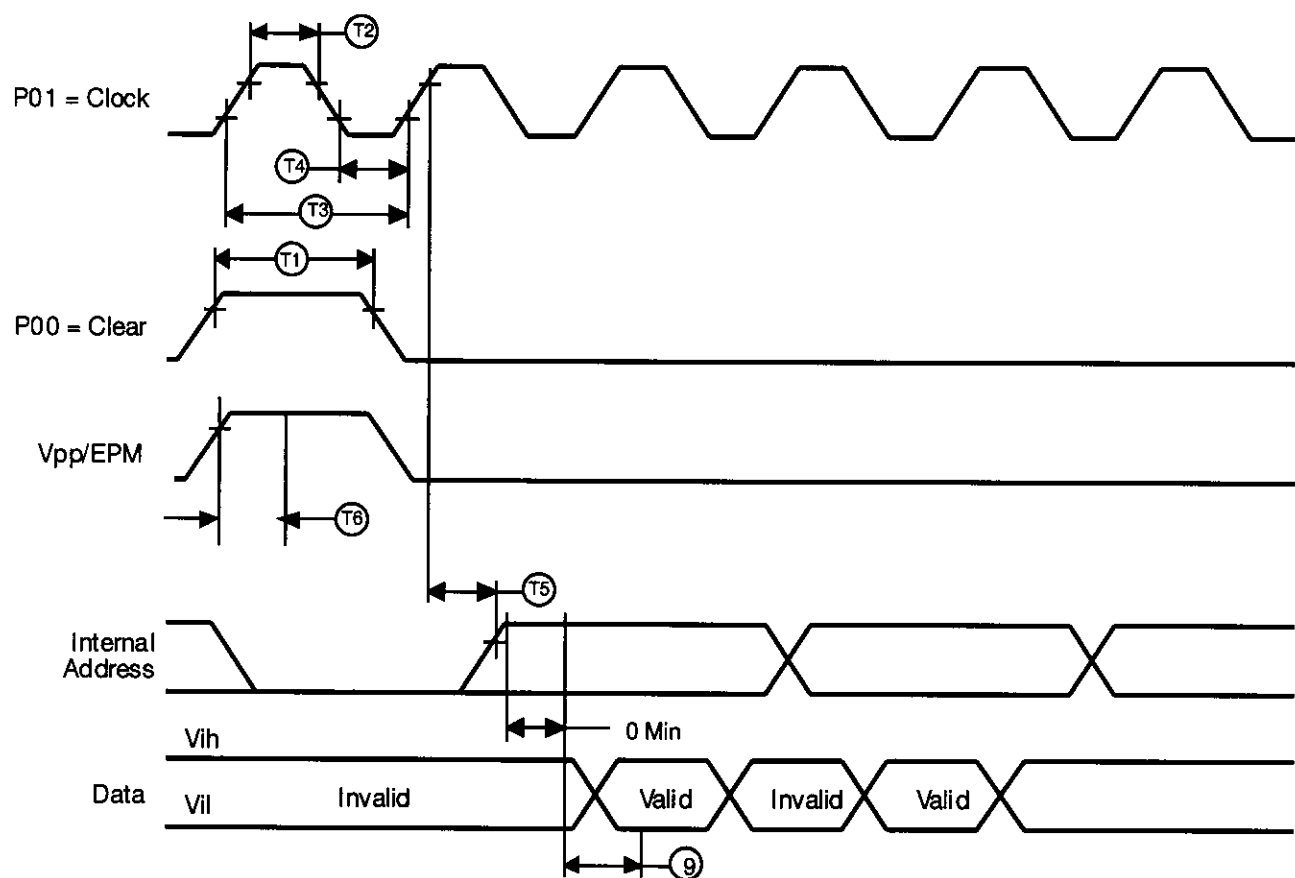
Legend:

T1	Reset Clock Width	30 ns Min
T2	Input Clock High	100 ns Min
T3	Input Clock Period	200 ns Min
T4	Input Clock Low	100 ns Min
T5	Clock to Address Counter Out Delay	15 ns Max
T6	Epm/Vpp Set up Time	40 μs Min

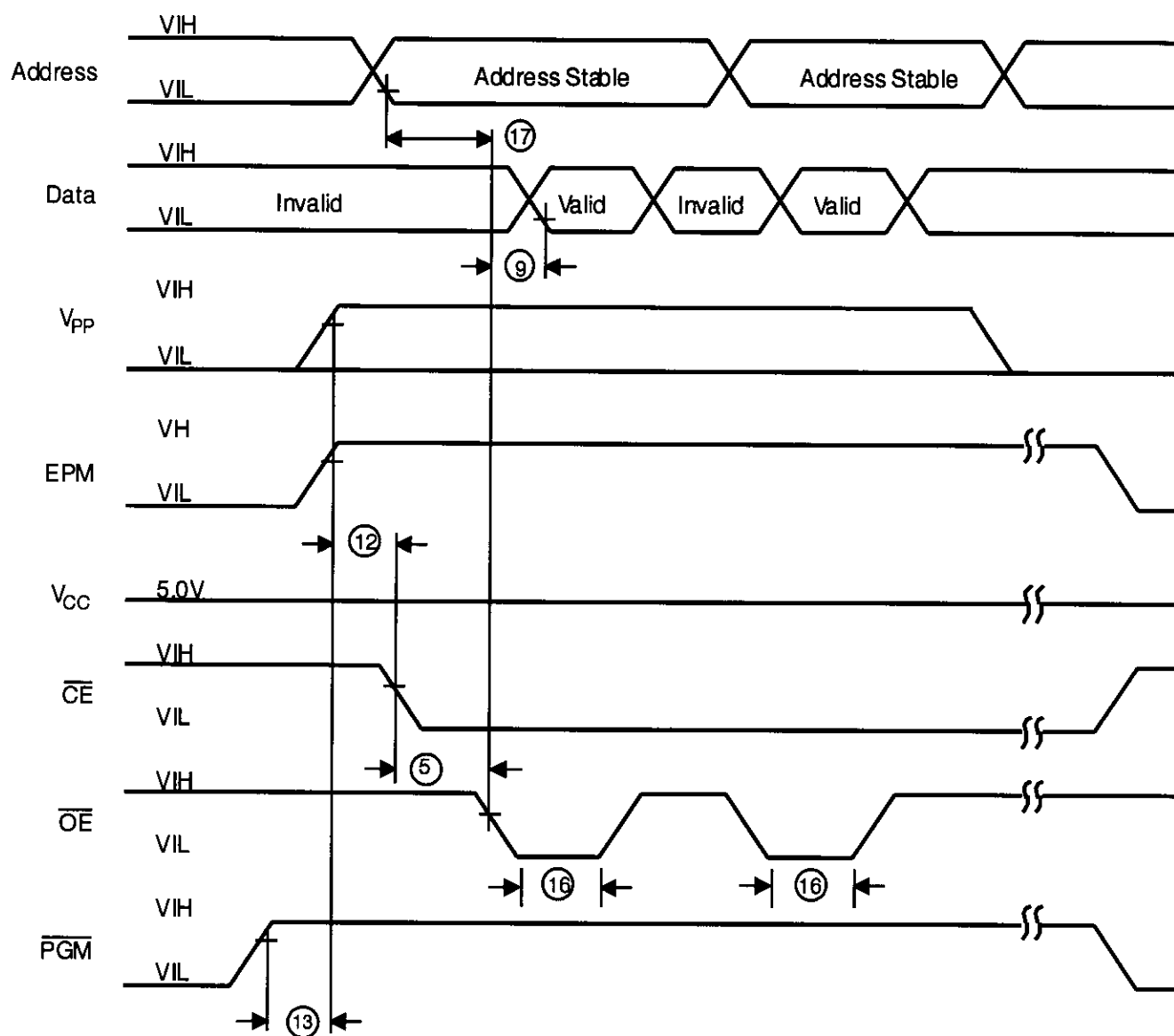## FUNCTIONAL DESCRIPTION (Continued)

**Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)**

FUNCTIONAL DESCRIPTION (Continued)

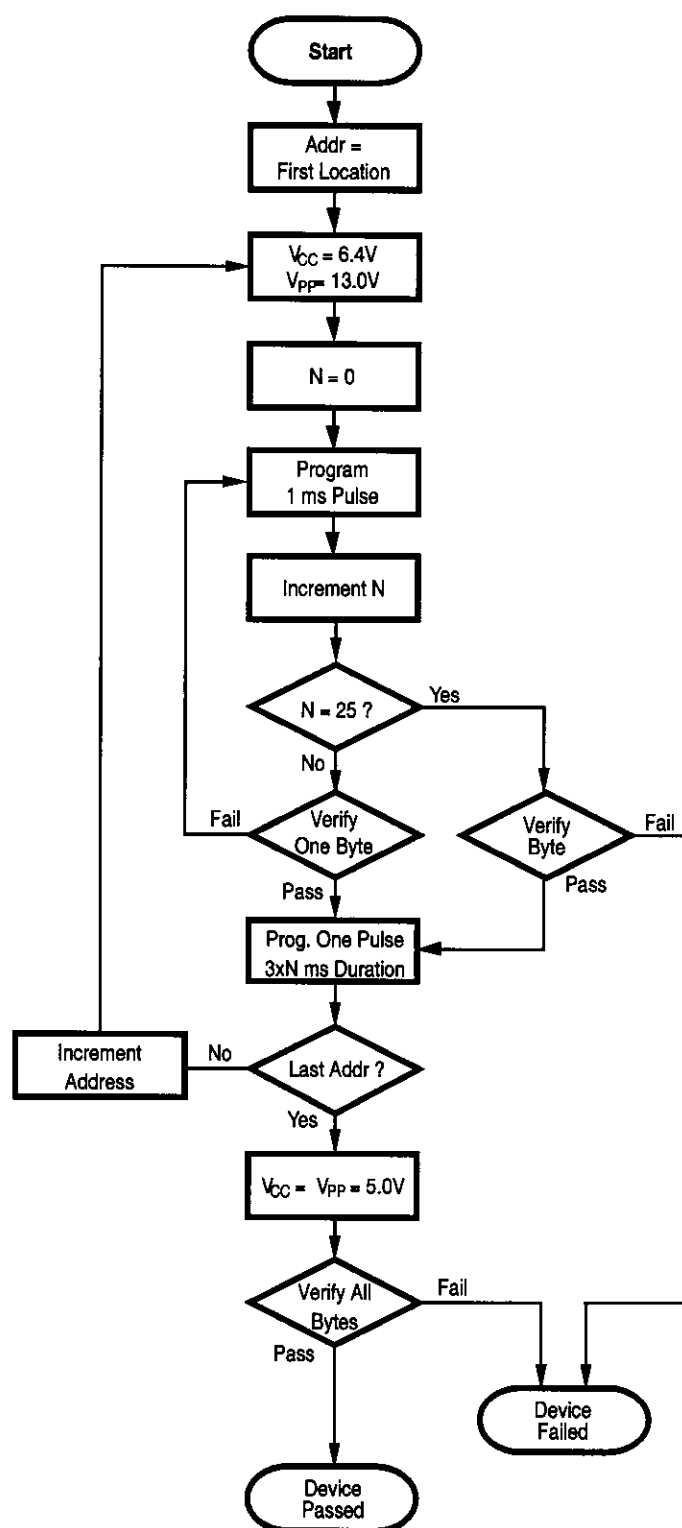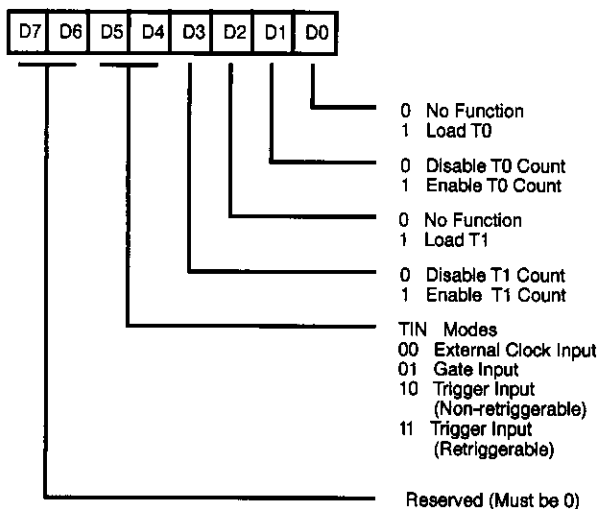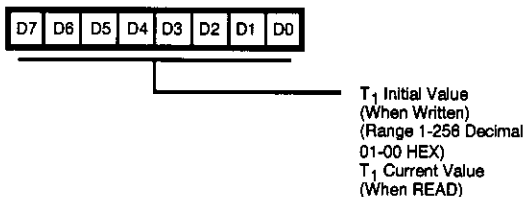
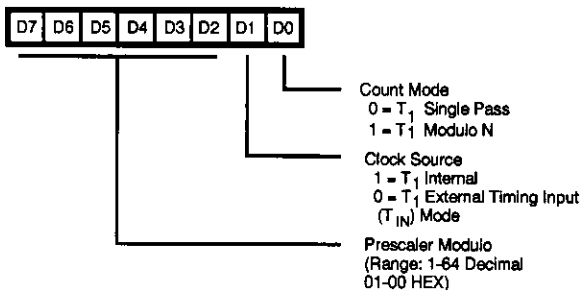**Figure 23. Z86E04/E08 Programming Algorithm**

Z8 CONTROL REGISTERS

R241 TMR

D7	D6	D5	D4	D3	D2	D1	D0

0 No Function
1 Load T0

0 Disable T0 Count
1 Enable T0 Count

0 No Function
1 Load T1

0 Disable T1 Count
1 Enable T1 Count

TIN Modes
00 External Clock Input
01 Gate Input
10 Trigger Input
   (Non-retriggerable)
11 Trigger Input
   (Retriggerable)

Reserved (Must be 0)

Figure 24. Timer Mode Register (F1$_H$: Read/Write)

R242 T1

D7	D6	D5	D4	D3	D2	D1	D0

T_1 Initial Value
(When Written)
(Range 1-256 Decimal
01-00 HEX)
T_1 Current Value
(When READ)

Figure 25. Counter Timer 1 Register (F2$_H$: Read/Write)

R243 PRE1

D7	D6	D5	D4	D3	D2	D1	D0

Count Mode
0 = T_1 Single Pass
1 = T_1 Modulo N

Clock Source
1 = T_1 Internal
0 = T_1 External Timing Input
(T_{IN}) Mode

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

Figure 26. Prescaler 1 Register (F3$_H$: Write Only)

R244 T0

D7	D6	D5	D4	D3	D2	D1	D0

T_0 Initial Value
(When Written)
(Range: 1-256 Decimal
01-00 HEX)
T_0 Current Value
(When READ)
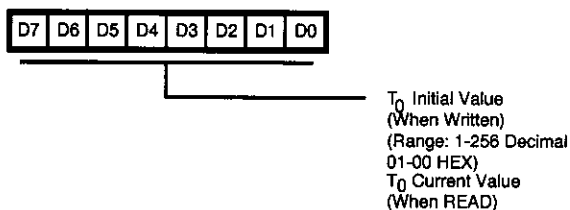
**Figure 27. Counter/Timer 0 Register
(F4$_H$: Read/Write)**

R245 PRE0

D7	D6	D5	D4	D3	D2	D1	D0

Count Mode
0 T0 Single Pass
1 T0 Modulo N

Reserved (Must be 0)

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
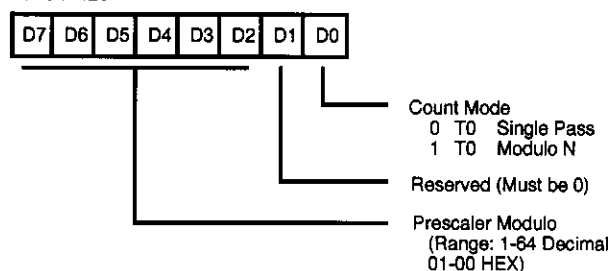
Figure 28. Prescaler 0 Register (F5$_H$: Write Only)

R246 P2M

D7	D6	D5	D4	D3	D2	D1	D0

$P2_7$ - $P2_0$ I/O Definition
0 Defines Bit as OUTPUT
1 Defines Bit as INPUT
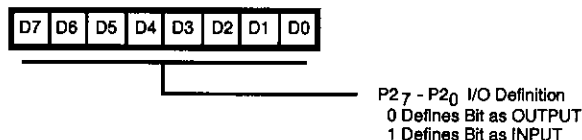
Figure 29. Port 2 Mode Register (F6$_H$: Write Only)

R247 P3M

D7	D6	D5	D4	D3	D2	D1	D0

0 Port 2 Open-Drain
1 Port 2 Push-pull

Port 3 Inputs
0 Digital Mode
1 Analog Mode

Reserved (Must be 0)
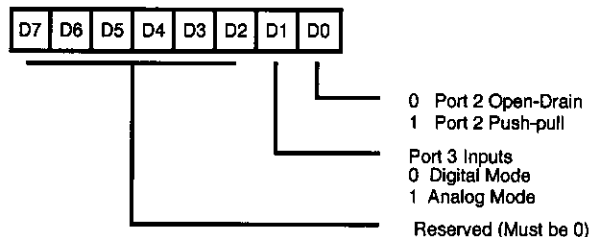
Figure 30. Port 3 Mode Register (F7$_H$: Write Only)