What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0412seg1903

GENERAL DESCRIPTION (Continued)

Figure 2. EPROM Programming Mode Block Diagram
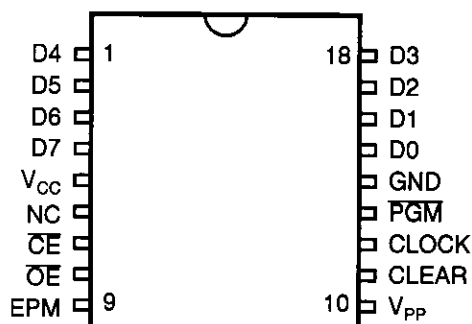
PRELIMINARY

PIN DESCRIPTION

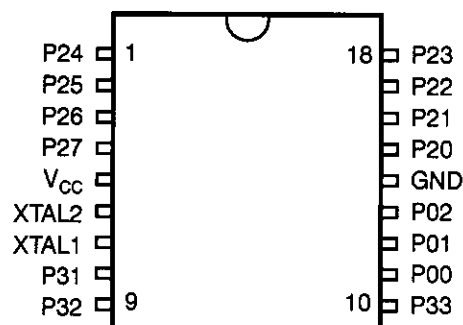
Figure 3. 18-Pin EPROM Mode Configuration

Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	NC	No Connection	
7	$\overline{CE}$	Chip Enable	Input
8	$\overline{OE}$	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	$\overline{PGM}$	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0, 1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode

Pin #	Symbol	Function	Direction
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

DC ELECTRICAL CHARACTERISTICS
Extended Temperature

Sym	Parameter	V_{CC} [4]	$T_A = -40°C$ to $+105°C$		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V_{INMAX}	Max Input Voltage	4.5V		12.0		V	$I_{IN} < 250 \mu A$	1
		5.5V		12.0		V	$I_{IN} < 250 \mu A$	1
V_{CH}	Clock Input High Voltage	4.5V	$0.8 V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
		5.5V	$0.8 V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.7	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.8	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.8	V		
V_{IL}	Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		4.5V	$V_{CC}-0.4$			V	Low Noise @ $I_{OH} = -0.5$ mA	
		5.5V	$V_{CC}-0.4$			V	Low Noise @ $I_{OH} = -0.5$ mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	$I_{OL} = +4.0$ mA	5
		5.5V		0.4	0.1	V	$I_{OL} = +4.0$ mA	5
		4.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
		5.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	$I_{OL} = +12$ mA,	5
		5.5V		1.0	0.3	V	$I_{OL} = +12$ mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
I_{OL}	Output Leakage	4.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	$V_{CC} -1.5$		V		

Sym	Parameter	V_{CC} [4]	$T_A = -40°C$ to $+105°C$ Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{CC} WDT is not Running	7,8
		5.5V		20	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		-20.0	-8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:
1. Port 2 and Port 0 only
2. $V_{SS} = 0V = GND$
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. $V_{CC} = 4.5V$ to $5.5V$, typical values measured at $V_{CC} = 5.0V$
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C					
				8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Extended Temperature

No	Symbol	Parameter	V_{CC}	8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1
11	Tpor	Power-On Reset Time	4.5V	12	100	12	100	ms	1
			5.5V	12	100	12	100	ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS
Low Noise Mode, Standard Temperature

No	Symbol	Parameter	V_{CC}	1 MHz Min	1 MHz Max	4 MHz Min	4 MHz Max	Units	Notes
				T_A= 0 °C to +70 °C					
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

PRELIMINARY

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

■ All pre-driver slew rates reduced to 10 ns typical.

■ Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

■ Output drivers have resistances of 500 Ohms (typical).

■ Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

V$_{CC}$ *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

$\overline{CE}$ *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V$_{PP}$ *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

$\overline{PGM}$ *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if *excessive noise* surges above V$_{CC}$ occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by *excessive noise* surges on the V$_{PP}$, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

■ Using a clamping diode to V$_{CC}$.

■ Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).
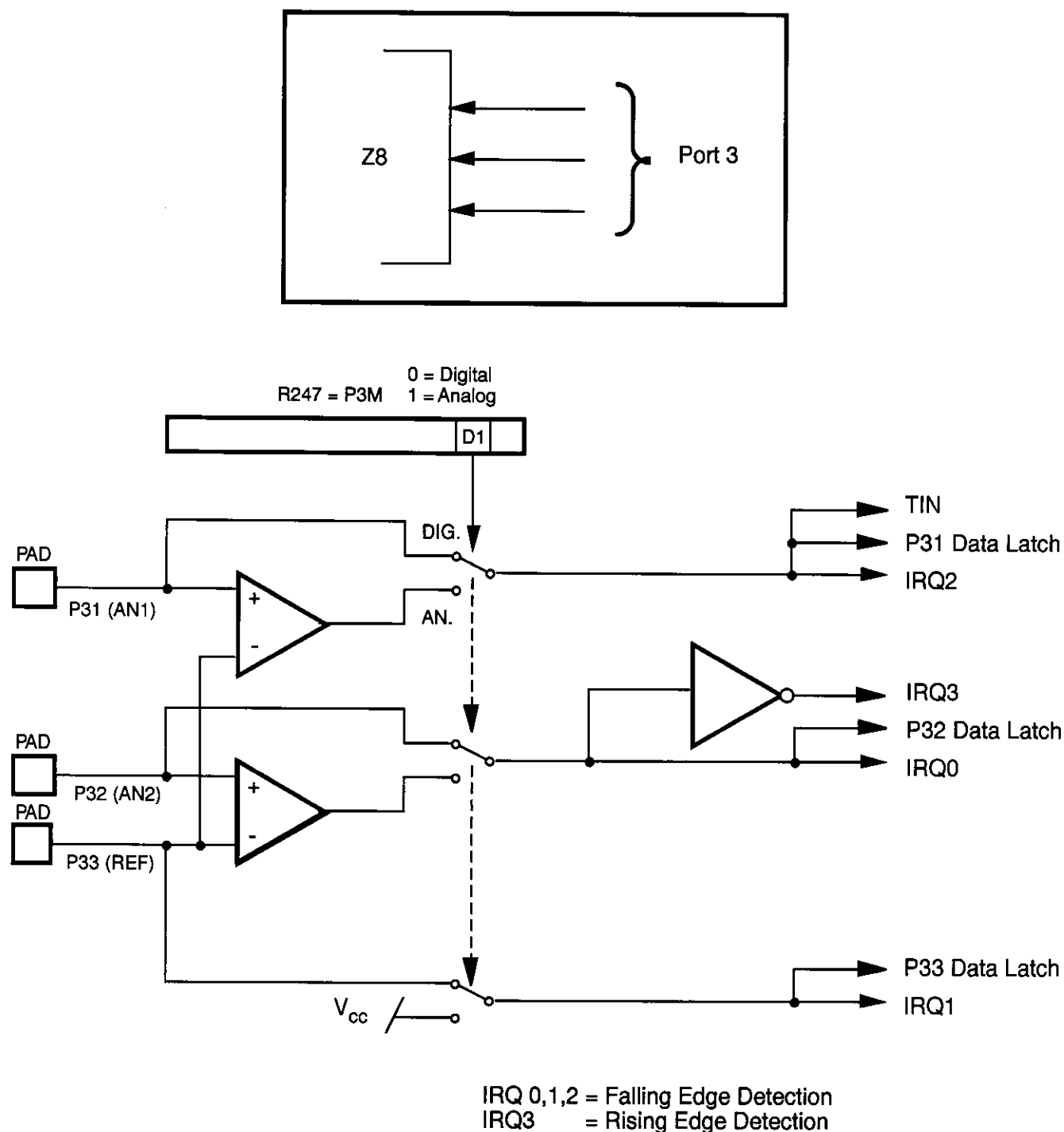

IRQ 0,1,2 = Falling Edge Detection
IRQ3   = Rising Edge Detection

Figure 9. Port 3 Configuration

PRELIMINARY

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.
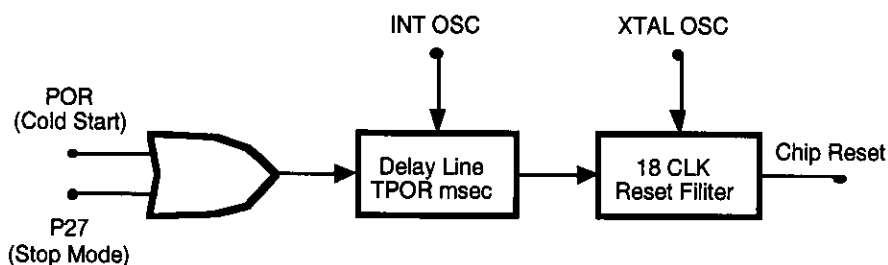

Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

■ Power-bad to power-good status

■ Stop-Mode Recovery

■ WDT time-out

■ WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Program Memory. The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.
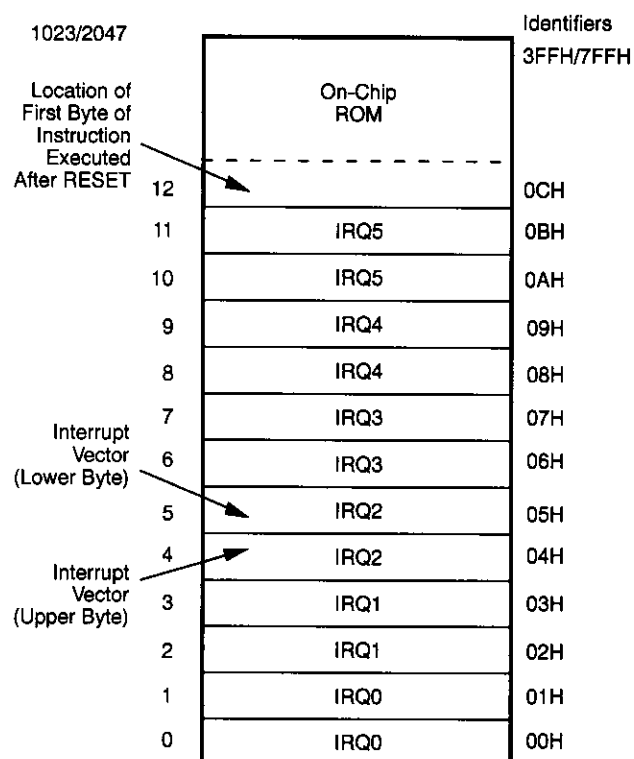
Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

Figure 11. Program Memory Map

Figure 12. Register File

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
$V_{CC} = 5.0V$ @ 25°C

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1µFd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
$V_{CC} = 3.3V$ @ 25°C

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1µFd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

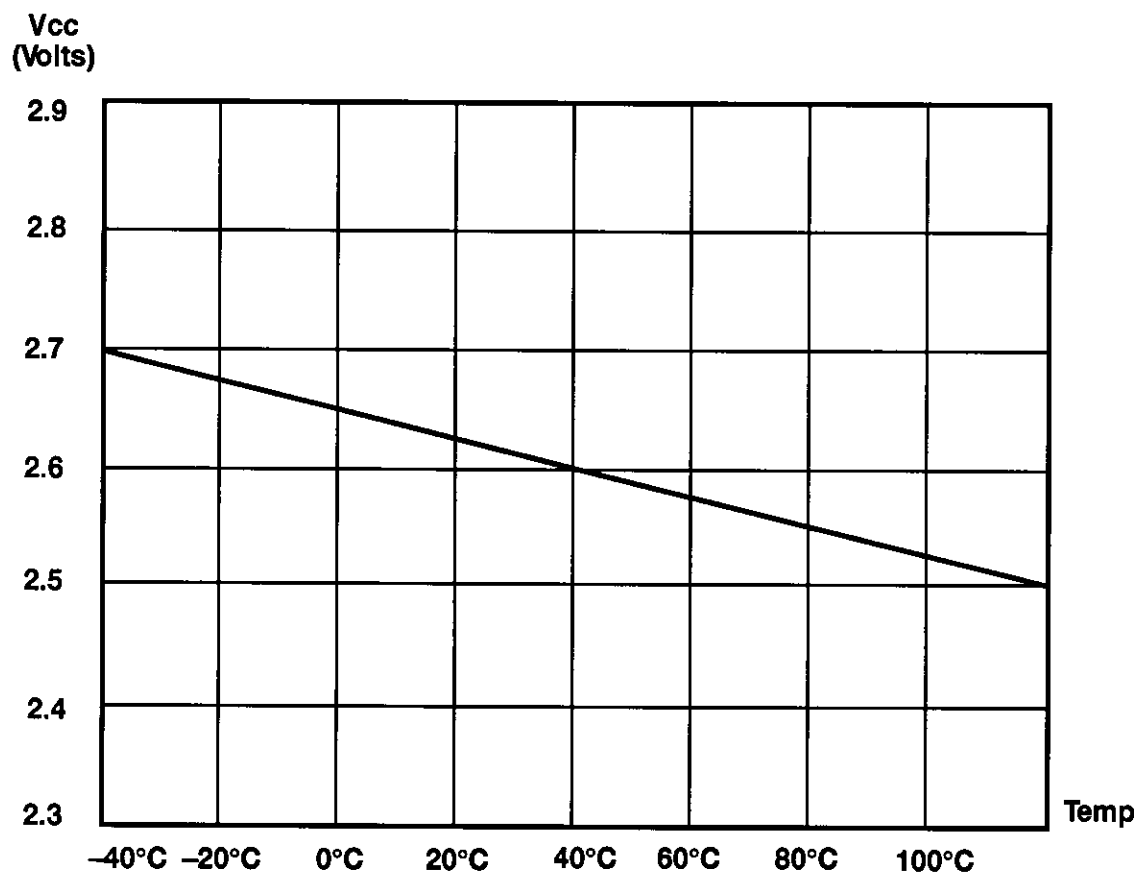## FUNCTIONAL DESCRIPTION (Continued)

**Figure 17. Typical Auto Reset Voltage
(V_{LV}) vs. Temperature**

Low EMI Emission

The Z8 can be programmed to operate in a low EMI Emission (Low Noise) Mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT Mode.

- All drivers slew rates reduced to 10 ns (typical).

- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 ohms (typical).

- Oscillator divide-by-two circuitry eliminated.

In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM Mode. XTAL2 has no function, XTAL1 functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as $\overline{PGM}$.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI **are supported** (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will not automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and $\overline{CE}$ pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP Mode. The V_{PP} requires both a diode and a 100 pF capacitor.

Auto Latch Disable. Auto Latch Disable option bit when programmed will globally disable all Auto Latches.

WDT Enable. The WDT Enable option bit, when programmed, will have the hardware enabled Permanent WDT enabled after exiting reset and can not be stopped in Halt or Stop Mode.

EPROM/Test Mode Disable. The EPROM/Test Mode Disable option bit, when programmed, will disable the EPROM Mode and the Factory Test Mode. Reading, verifying, and programming the Z8 will be disabled. To fully verify that this mode is disabled, the device must be power cycled.

User Modes. Table 7 shows the programming voltage of each mode.

Table 7. OTP Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ	NU	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.0V
PROGRAM	V_H	V_{IH}	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_{IH}	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.4V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
AUTO LATCH DISABLE	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V
WDT ENABLE	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
EPROM/TEST MODE	V_H	V_{IL}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V

Notes:
1. V_H = 12.75V ± 0.25 V_{DC} .
2. V_{IH} = As per specific Z8 DC specification.
3. V_{IL} = As per specific Z8 DC specification.
4. X = Not used, but must be set to V_H or V_{IH} level.
5. NU = Not used, but must be set to either V_{IH} or V_{IL} level.
6. I_{PP} during programming = 40 mA maximum.
7. I_{CC} during programming, verify, or read = 40 mA maximum.
8. * V_{CC} has a tolerance of ±0.25V.
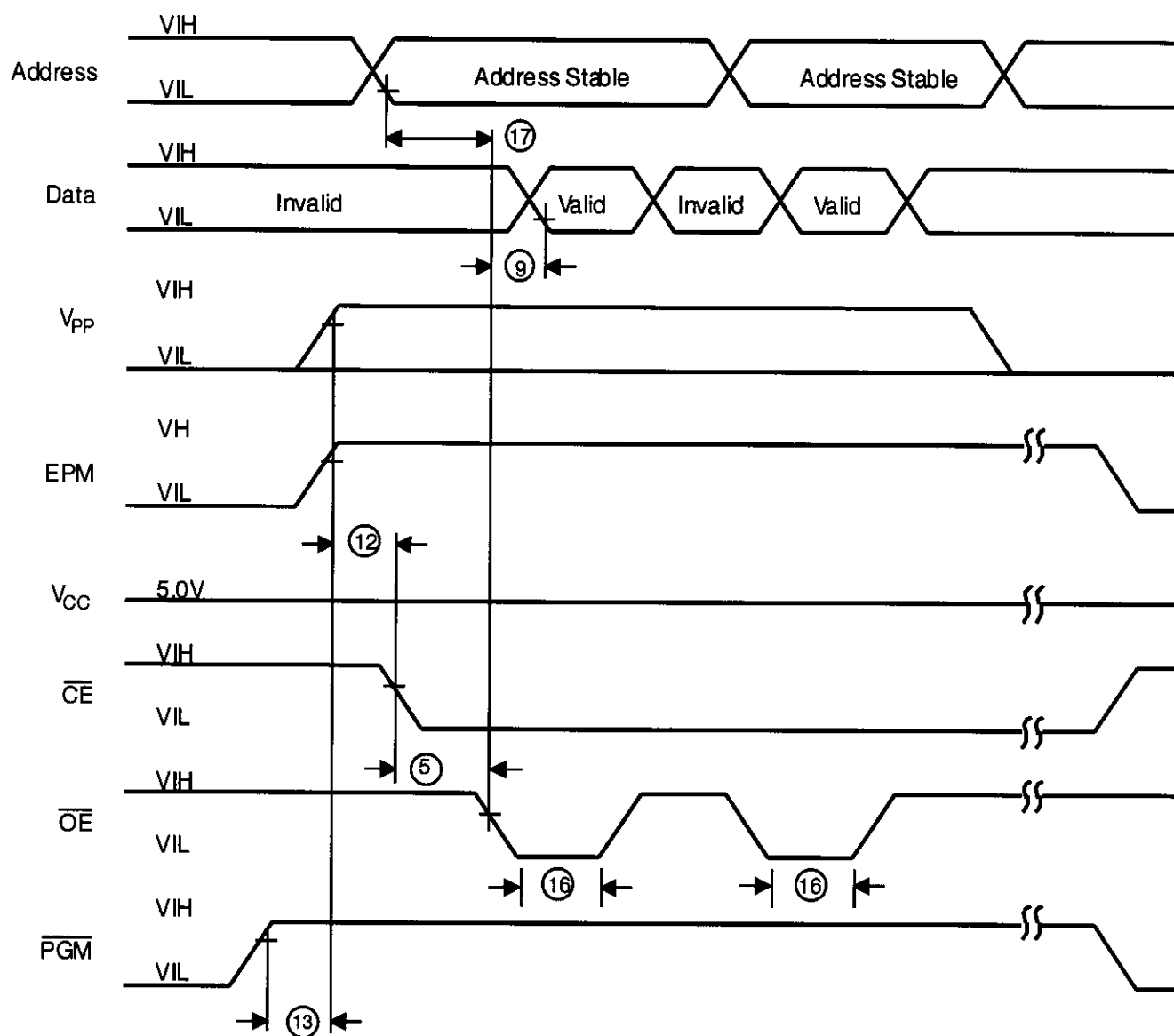
FUNCTIONAL DESCRIPTION (Continued)

**Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)**
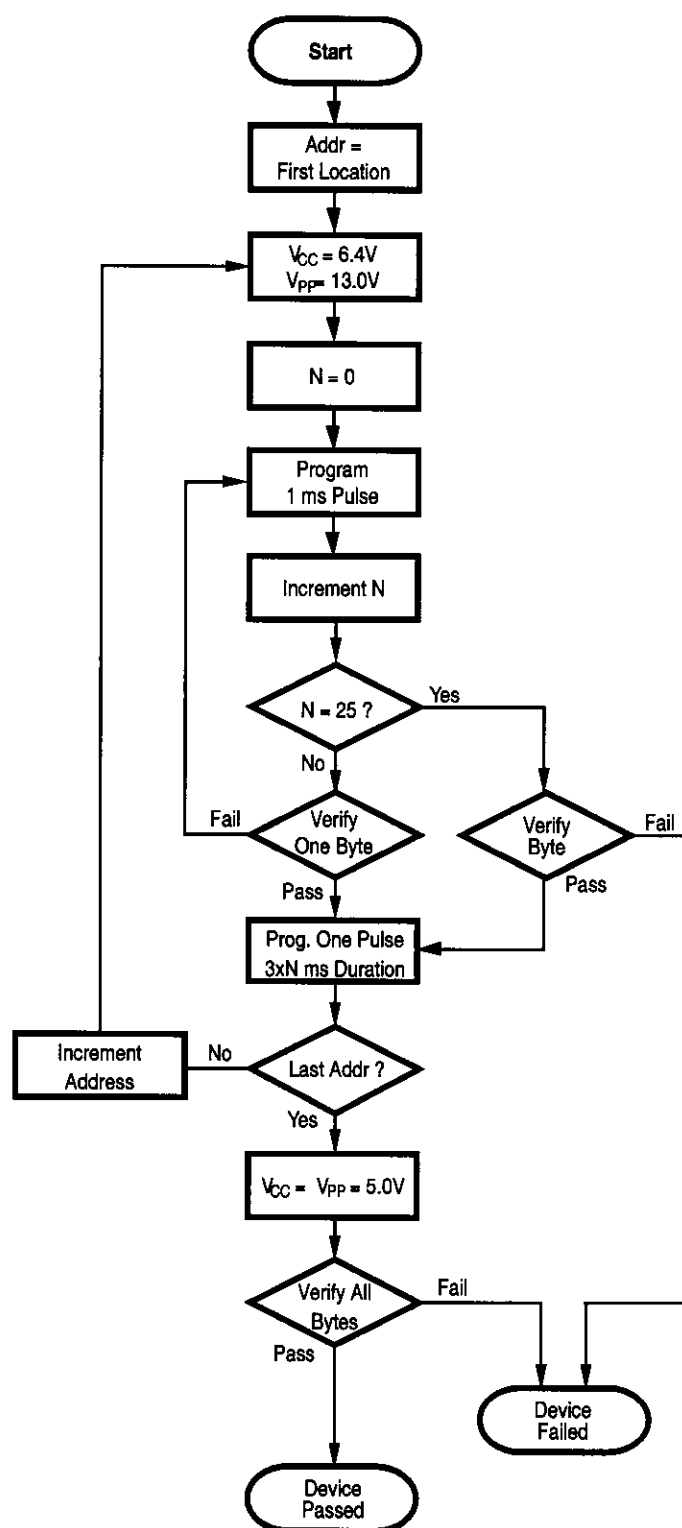
P R E L I M I N A R Y

FUNCTIONAL DESCRIPTION (Continued)

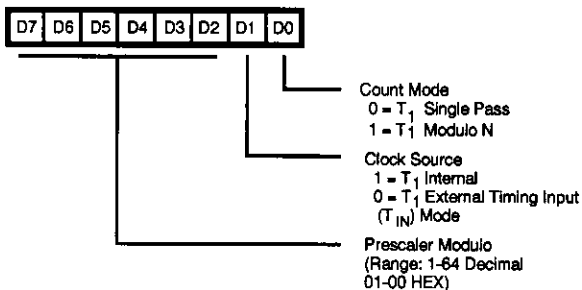**Figure 23. Z86E04/E08 Programming Algorithm**

Z8 CONTROL REGISTERS

R241 TMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

0 No Function
1 Load T0

0 Disable T0 Count
1 Enable T0 Count

0 No Function
1 Load T1

0 Disable T1 Count
1 Enable T1 Count

TIN Modes
00 External Clock Input
01 Gate Input
10 Trigger Input
(Non-retriggerable)
11 Trigger Input
(Retriggerable)

Reserved (Must be 0)
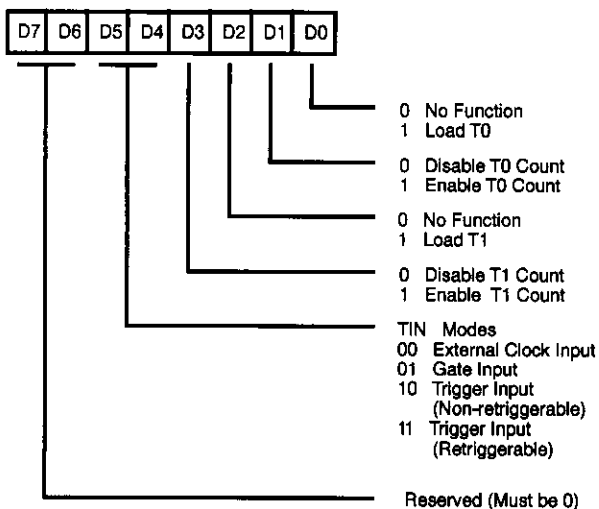
Figure 24. Timer Mode Register (F1$_H$: Read/Write)

R242 T1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

T_1 Initial Value
(When Written)
(Range 1-256 Decimal
01-00 HEX)
T_1 Current Value
(When READ)
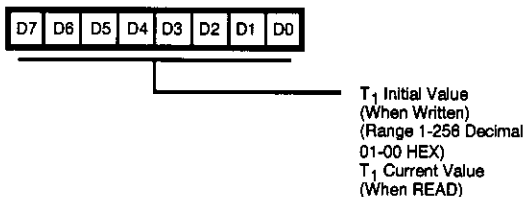
Figure 25. Counter Timer 1 Register (F2$_H$: Read/Write)

R243 PRE1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Count Mode
0 = T_1 Single Pass
1 = T_1 Modulo N

Clock Source
1 = T_1 Internal
0 = T_1 External Timing Input
(T_{IN}) Mode

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

Figure 26. Prescaler 1 Register (F3$_H$: Write Only)

R244 T0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

T_0 Initial Value
(When Written)
(Range: 1-256 Decimal
01-00 HEX)
T_0 Current Value
(When READ)
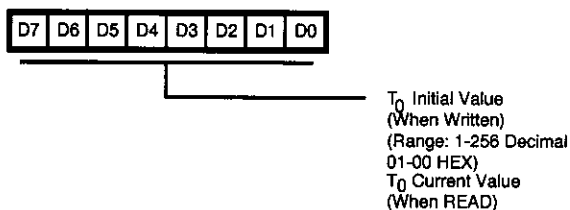
**Figure 27. Counter/Timer 0 Register
(F4$_H$: Read/Write)**

R245 PRE0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Count Mode
0 T0 Single Pass
1 T0 Modulo N

Reserved (Must be 0)

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
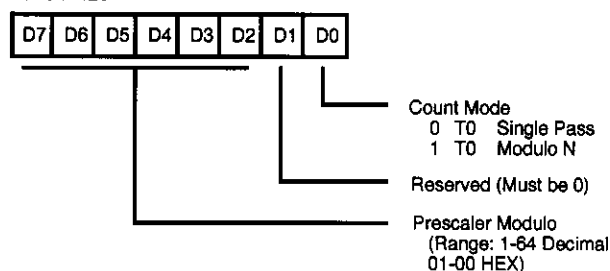
Figure 28. Prescaler 0 Register (F5$_H$: Write Only)

R246 P2M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

$P2_7$ - $P2_0$ I/O Definition
0 Defines Bit as OUTPUT
1 Defines Bit as INPUT
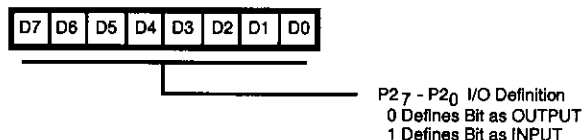
Figure 29. Port 2 Mode Register (F6$_H$: Write Only)

R247 P3M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

0 Port 2 Open-Drain
1 Port 2 Push-pull

Port 3 Inputs
0 Digital Mode
1 Analog Mode

Reserved (Must be 0)
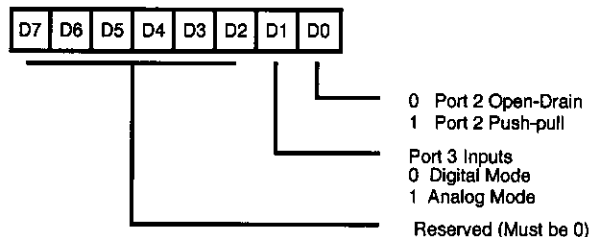
Figure 30. Port 3 Mode Register (F7$_H$: Write Only)

Z8 CONTROL REGISTERS (Continued)

R248 P01M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

P0₂-P0₀ Mode
00 = Output
01 = Input

Reserved (Must be 1.)

Reserved (Must be 0.)
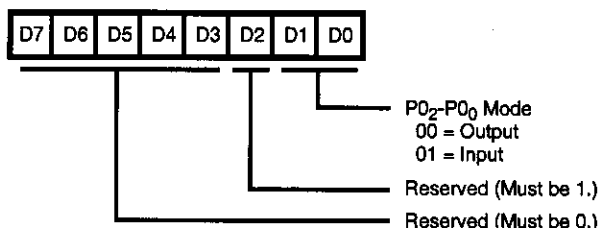
Figure 31. Port 0 and 1 Mode Register
(F8ₕ: Write Only)

R249 IPR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Interrupt Group Priority
Reserved = 000
C > A > B = 001
A > B > C = 010
A > C > B = 011
B > C > A = 100
C > B > A = 101
B > A > C = 110
Reserved = 111

IRQ1, IRQ4 Priority (Group C)
0 = IRQ1 > IRQ4
1 = IRQ4 > IRQ1

IRQ0, IRQ2 Priority (Group B)
0 = IRQ2 > IRQ0
1 = IRQ0 > IRQ2

IRQ3, IRQ5 Priority (Group A)
0 = IRQ5 > IRQ3
1 = IRQ3 > IRQ5

Reserved (Must be 0.)
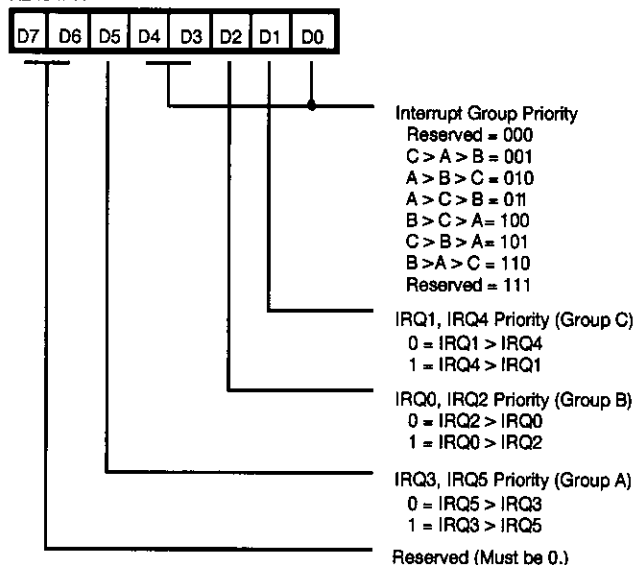
Figure 32. Interrupt Priority Register
(F9ₕ: Write Only)

R250 IRQ

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = P32 Input
IRQ4 = T0
IRQ5 = T1

Reserved (Must be 0)
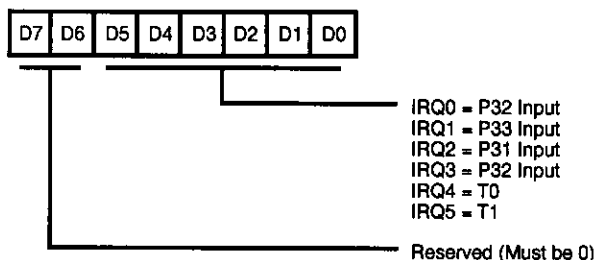
Figure 33. Interrupt Request Register
(FAₕ: Read/Write)

R251 IMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1 Enables IRQ0-IRQ5
(D₀ = IRQ0)

Reserved (Must be 0.)

1 Enables Interrupts
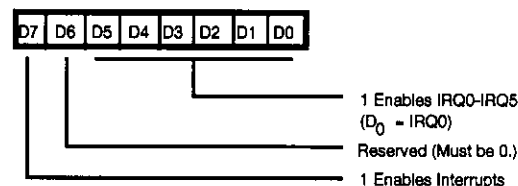
Figure 34. Interrupt Mask Register
(FBₕ: Read/Write)

R252 Flags

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

User Flag F1

User Flag F2

Half Carry Flag

Decimal Adjust Flag

Overflow Flag

Sign Flag

Zero Flag

Carry Flag
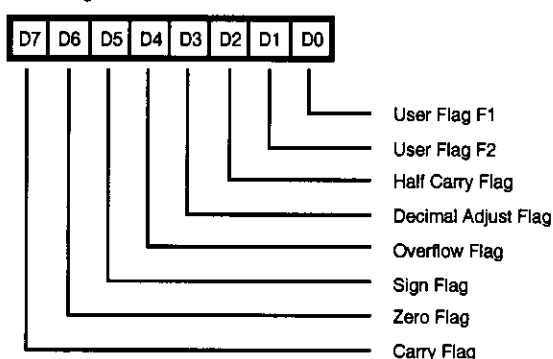
Figure 35. Flag Register
(FCₕ: Read/Write)

R253 RP

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Expanded Register File

Working Register Pointer

Default After Reset = 00H
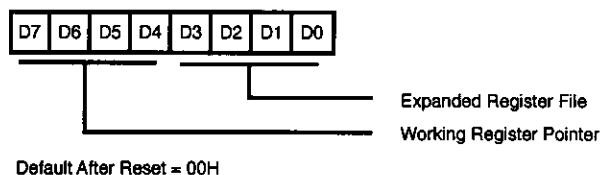
Figure 36. Register Pointer
(FDₕ: Read/Write)

R255 SPL

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stack Pointer Lower
Byte (SP₇ - SP₀)

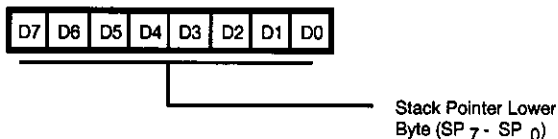**Figure 37. Stack Pointer**
(FFₕ: Read/Write)

ORDERING INFORMATION

Z86E04

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86E0412PSC	Z86E0412SSC
Z86E0412PEC	Z86E0412SEC

Z86E08

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86E0812PSC	Z86E0812SSC
Z86E0812PEC	Z86E0812SEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

Codes

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speeds
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86E04 12 P S C   is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow
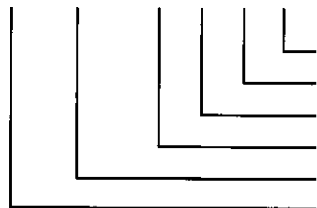
Environmental Flow
Temperature
Package
Speed
Product Number
Zilog Prefix