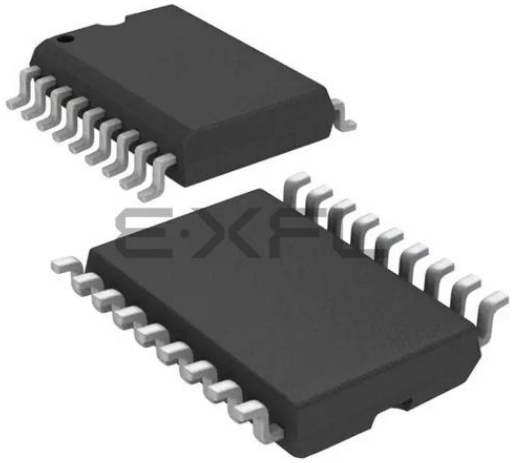

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0412ssg1866

FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1µs @ 12 MHz)
- RAM Bytes (125)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8® MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All Signals with an overline, "‾", are active Low, for example: B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

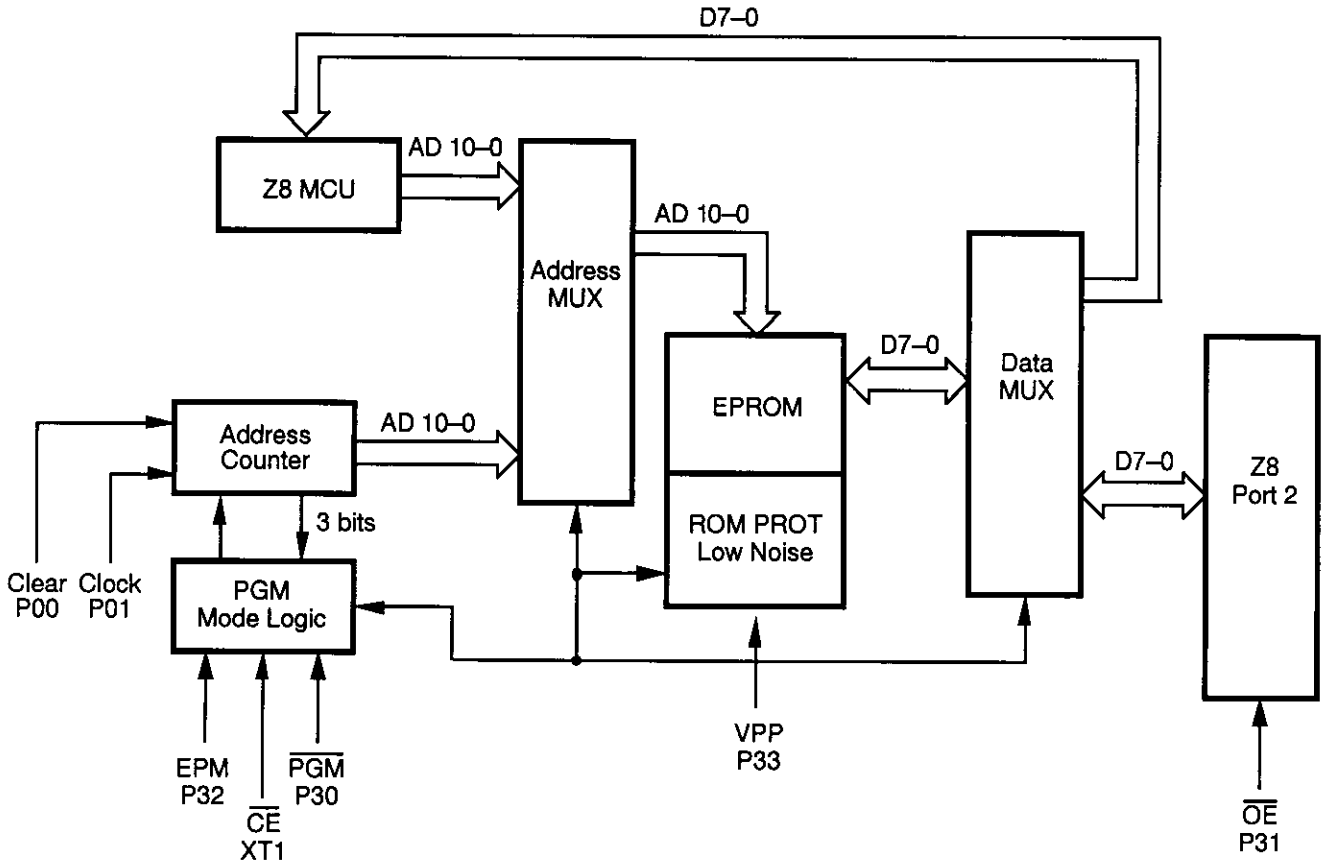

Figure 2. EPROM Programming Mode Block Diagram

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V,V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5 to 5.5V, typical values measured at V_{CC} = 5.0V.
   The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C						
				8 MHz		12 MHz				
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Extended Temperature

				T_A= –40 °C to +105 °C 8 MHz		12 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V		62		41	ns	1
			5.5V		62		41	ns	1
4	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1
11	Tpor	Power-On Reset Time	4.5V	12	100	12	100	ms	1
			5.5V	12	100	12	100	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

				T_A= –40 °C to +105 °C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V		4TpC	4TpC			1
			5.5V		4TpC	4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

PIN FUNCTIONS (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

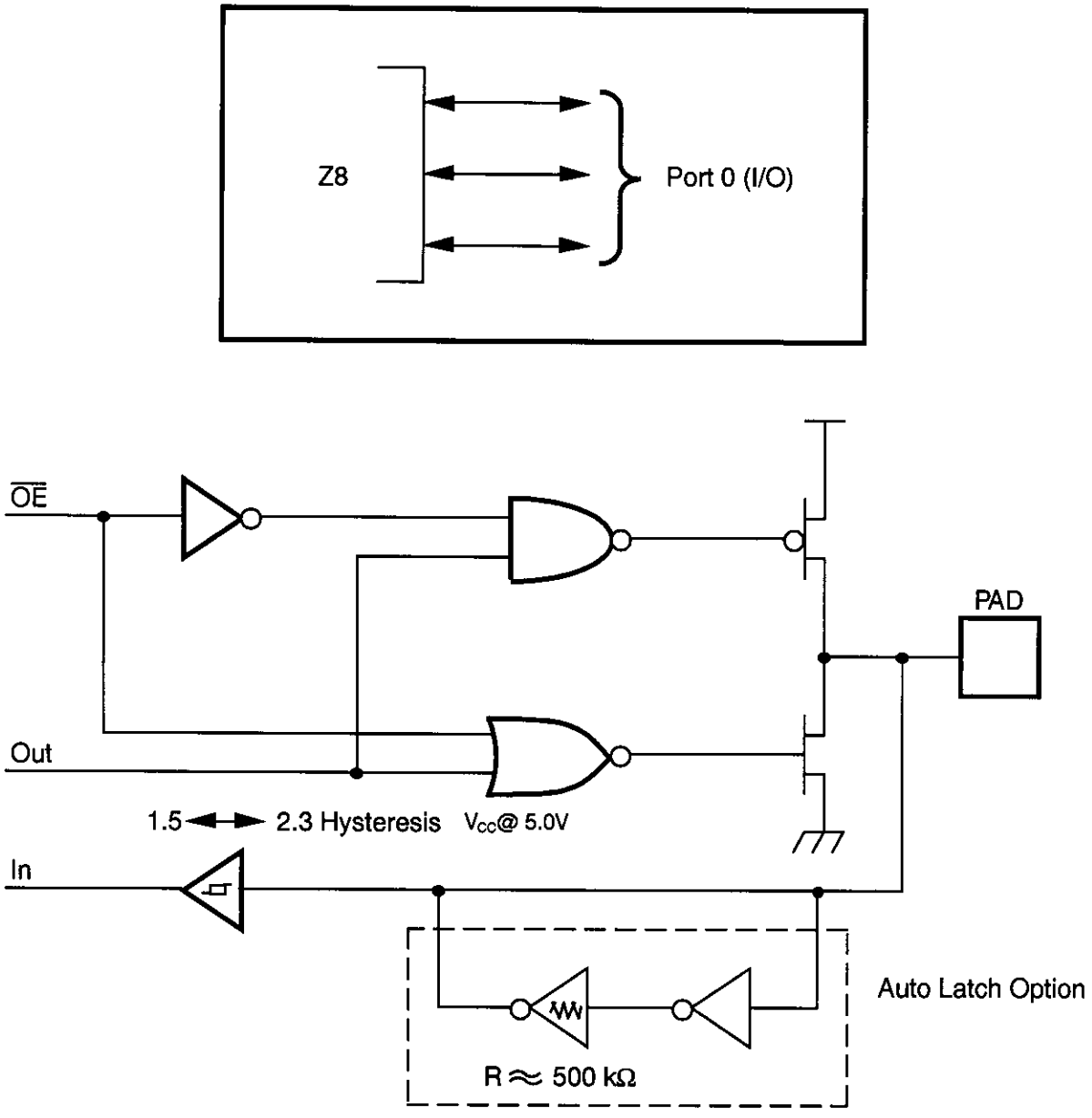

Figure 7. Port 0 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

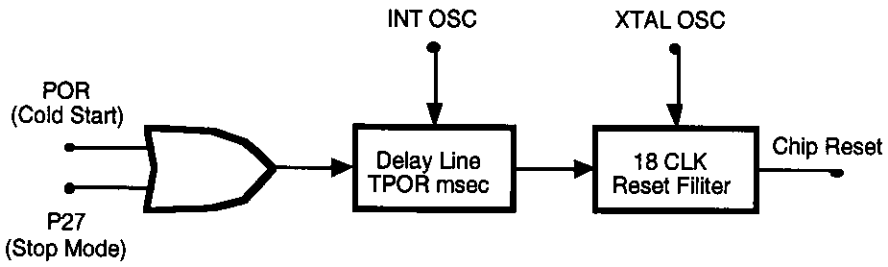

Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

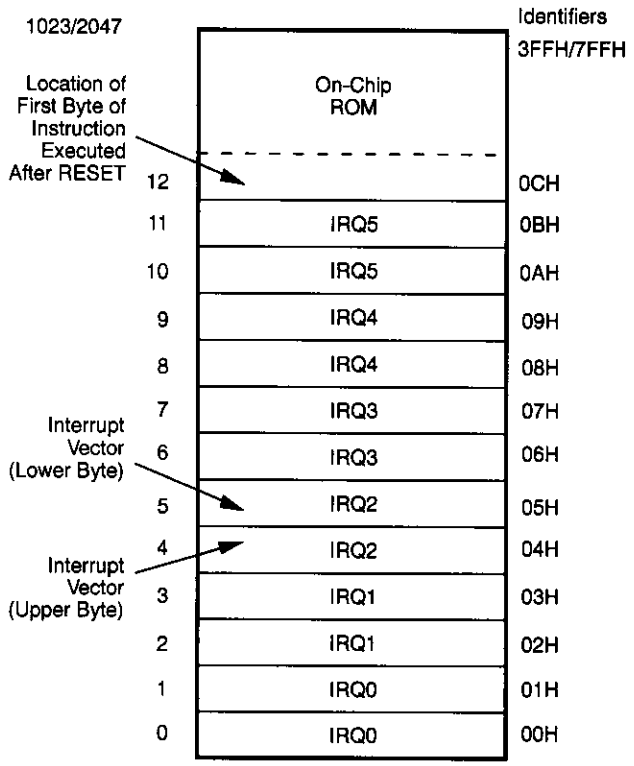

Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

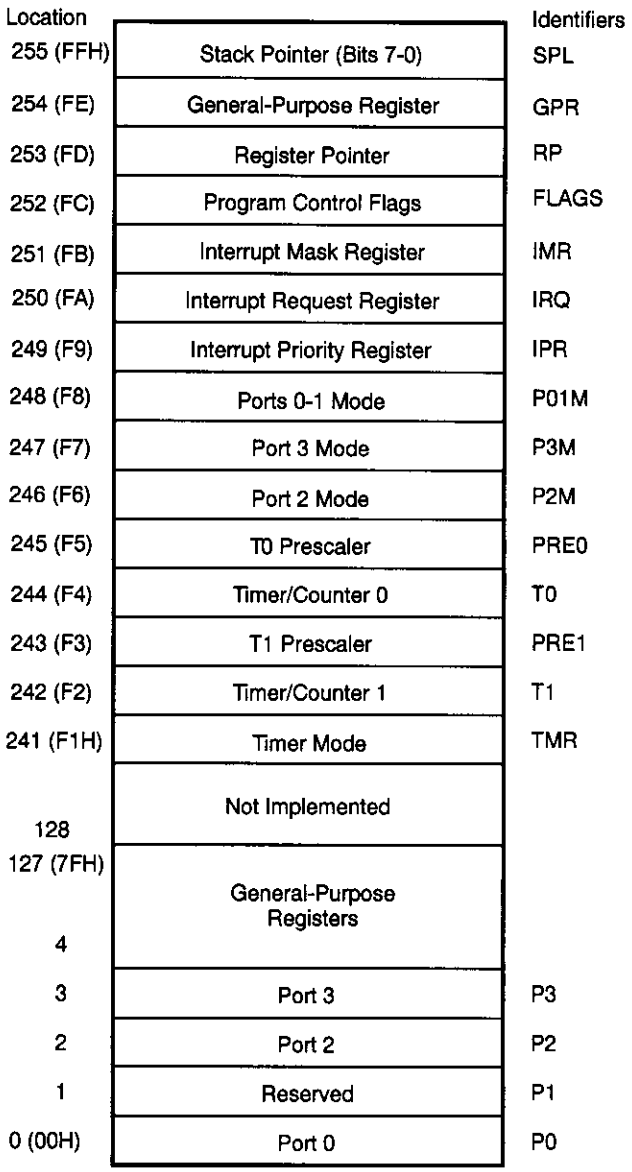

Figure 12. Register File

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

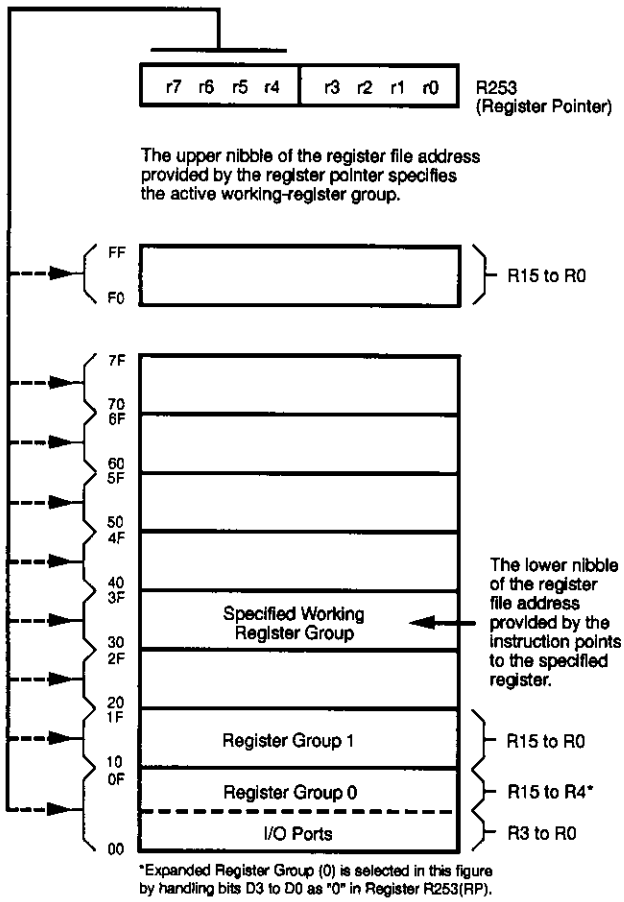

Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
V_{CC} = 5.0V @ 25°C

	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1µFd	
Resistor (R)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
V_{CC} = 3.3V @ 25°C

	Load Capacitor							
Resistor (R)	33 pFd		56 pFd		100 pFd		0.00 1µFd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

FUNCTIONAL DESCRIPTION (Continued)

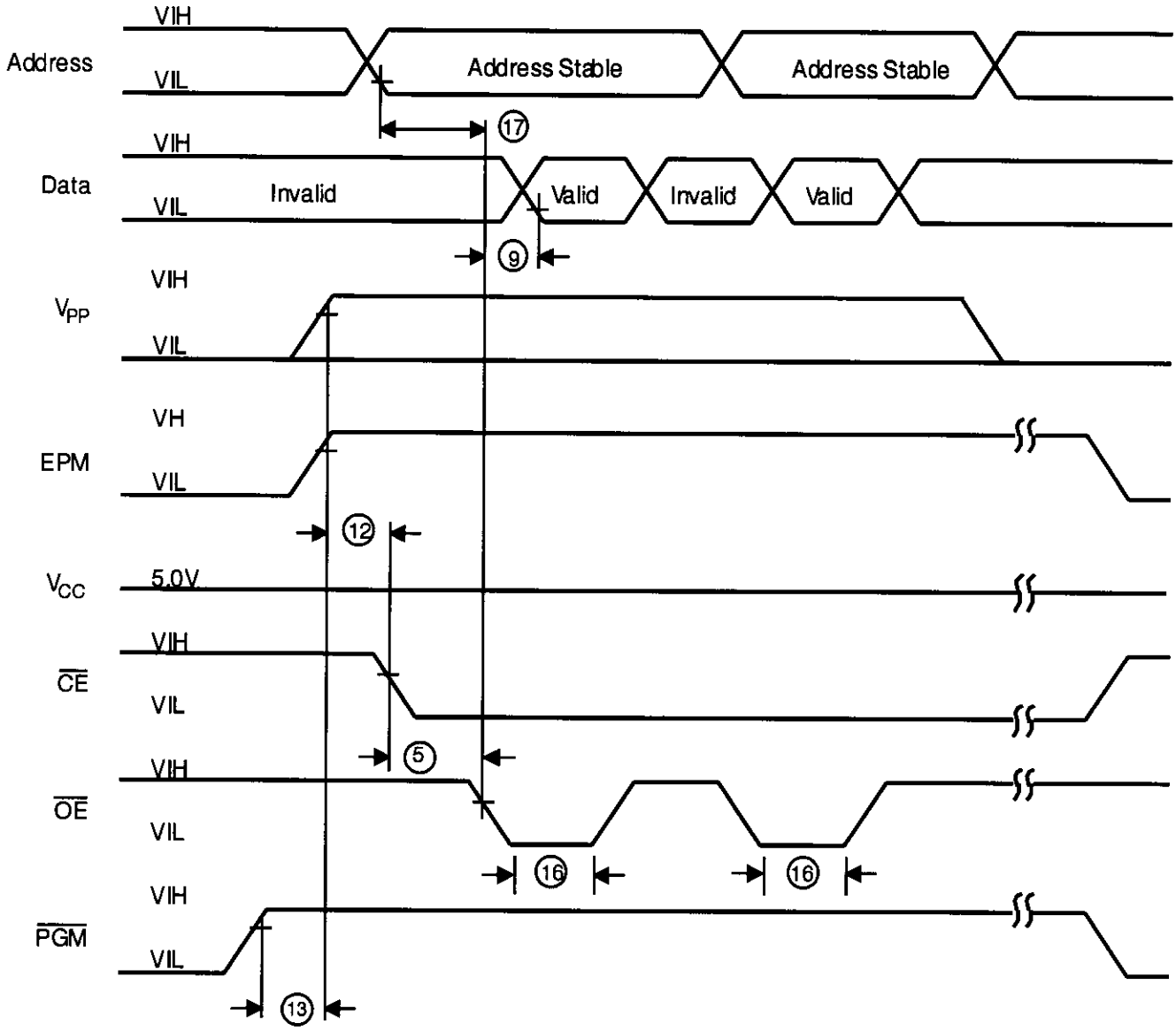

Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)

FUNCTIONAL DESCRIPTION (Continued)

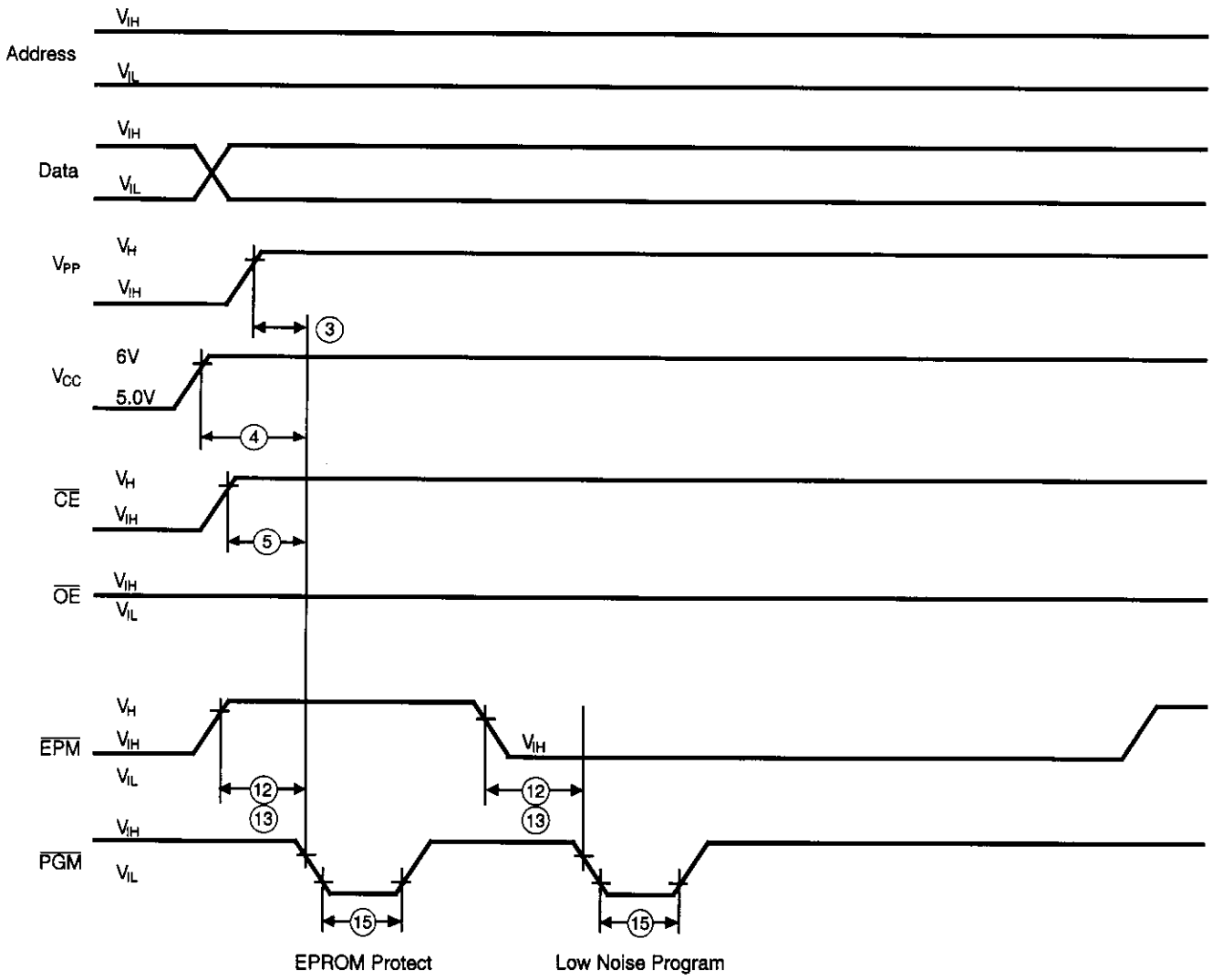

Figure 21. Z86E04/E08 Programming Options Waveform (EPROM Protect and Low Noise Program)

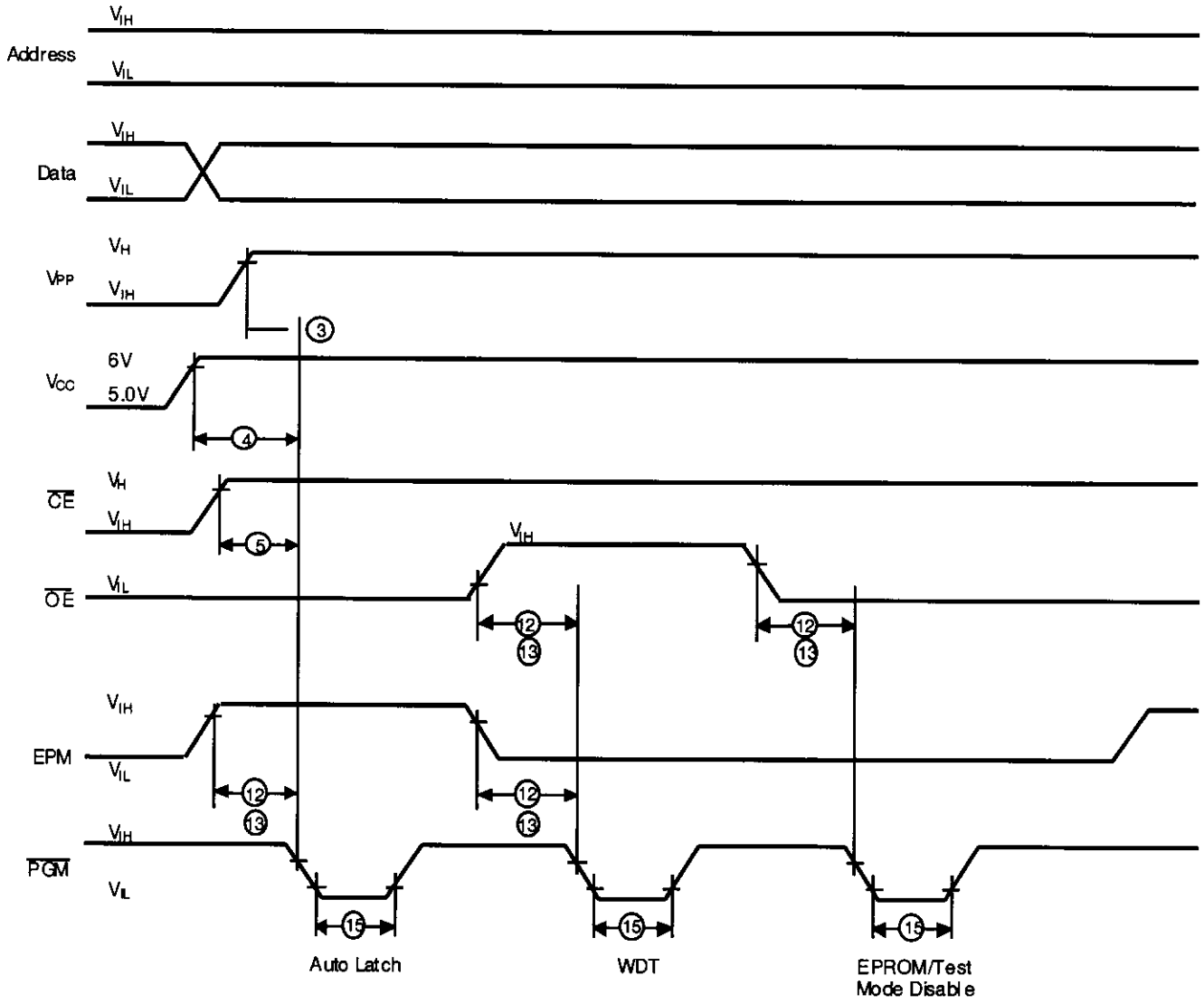

Figure 22. Z86E04/E08 Programming Options Waveform (Auto Latch Disable, Permanent WDT Enable and EPROM/Test Mode Disable)

Z8 CONTROL REGISTERS (Continued)

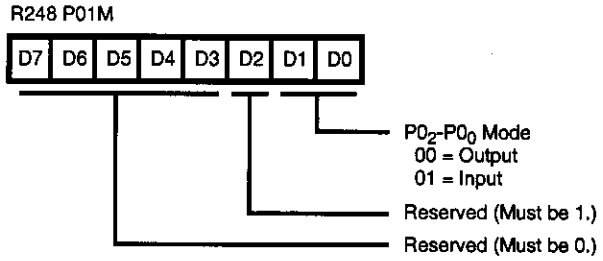

Figure 31. Port 0 and 1 Mode Register ($F8_H$: Write Only)

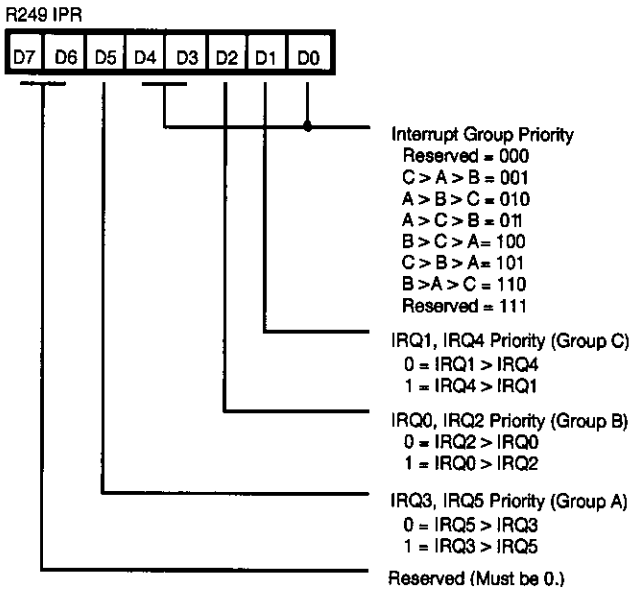

Figure 32. Interrupt Priority Register ($F9_H$: Write Only)

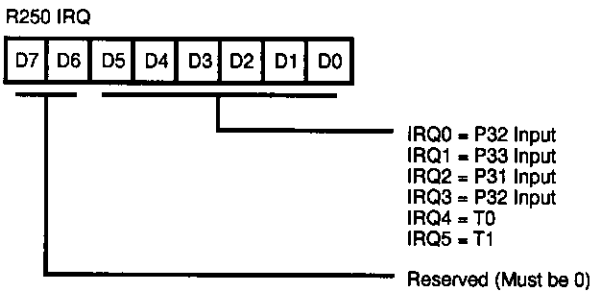

Figure 33. Interrupt Request Register (FA_H: Read/Write)

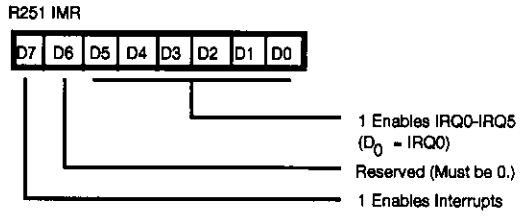

Figure 34. Interrupt Mask Register (FB_H: Read/Write)

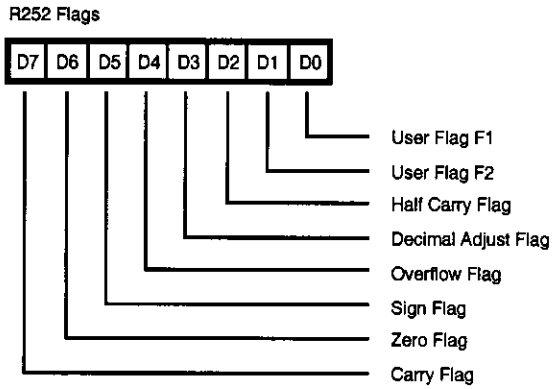

Figure 35. Flag Register (FC_H: Read/Write)

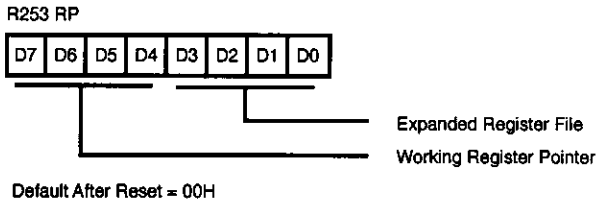

Figure 36. Register Pointer (FD_H: Read/Write)

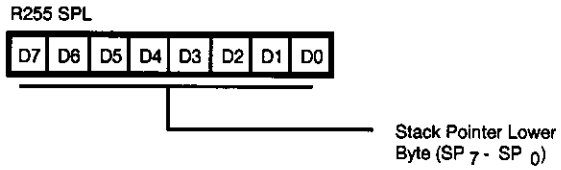

Figure 37. Stack Pointer (FF_H: Read/Write)

ORDERING INFORMATION

Z86E04		Z86E08	
Standard Temperature		Standard Temperature	
18-Pin DIP	18-Pin SOIC	18-Pin DIP	18-Pin SOIC
Z86E0412PSC	Z86E0412SSC	Z86E0812PSC	Z86E0812SSC
Z86E0412PEC	Z86E0412SEC	Z86E0812PEC	Z86E0812SEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

Codes

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC

Preferred Temperature
S = 0°C to +70°C
E = –40°C to +105°C

Speeds
12 =12 MHz

Environmental
C = Plastic Standard

Example:

Z 86E04 12 P S C is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow