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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z86e0412ssg1903">https://www.e-xfl.com/product-detail/zilog/z86e0412ssg1903</a>

## FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts  
(3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1 $\mu$ s @ 12 MHz)
- RAM Bytes (125)

## GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8<sup>®</sup> MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

**Note:** All Signals with an overline, " $\overline{\phantom{x}}$ ", are active Low, for example:  $\overline{B/W}$  (WORD is active Low);  $\overline{B}/W$  (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

# GENERAL DESCRIPTION (Continued)

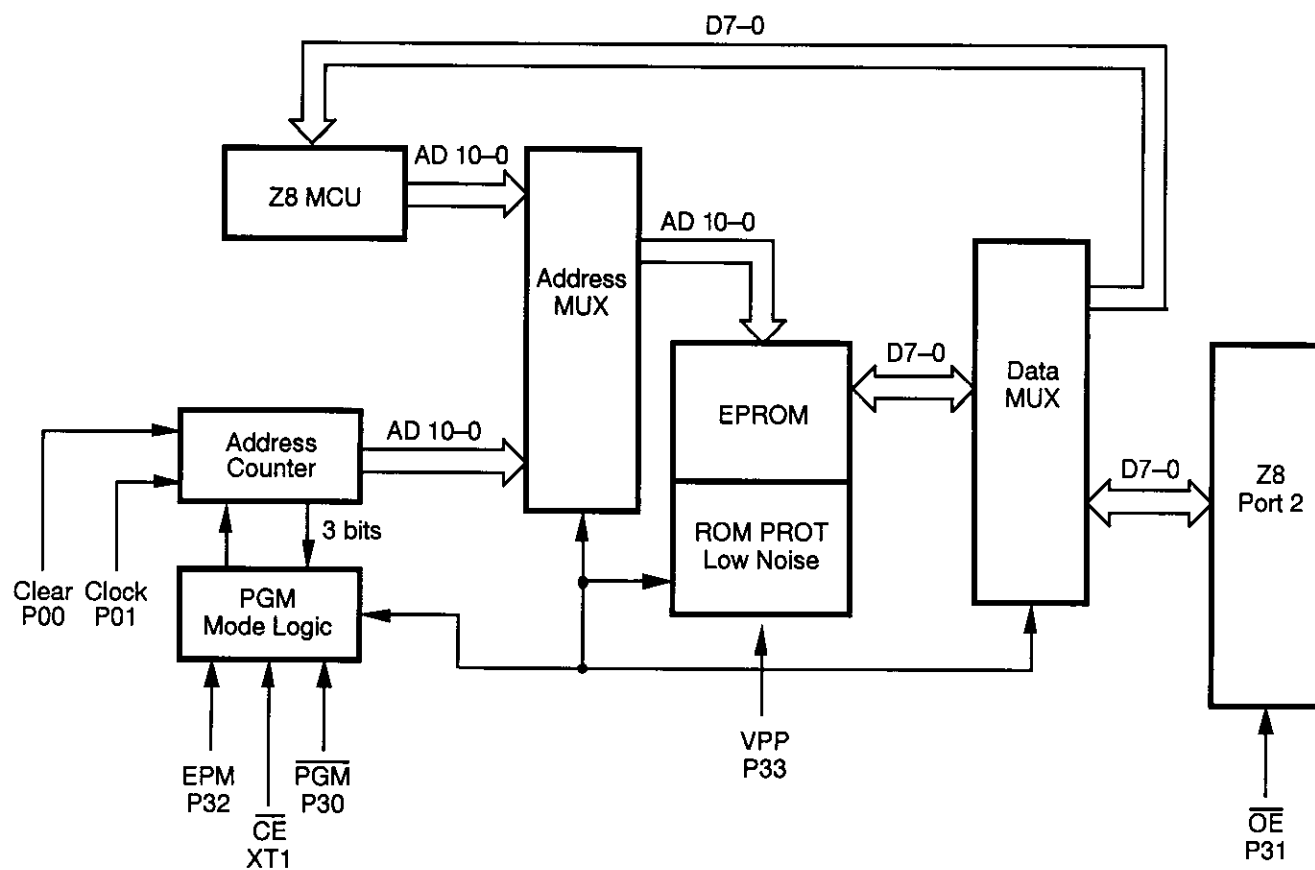


Figure 2. EPROM Programming Mode Block Diagram

## PIN DESCRIPTION

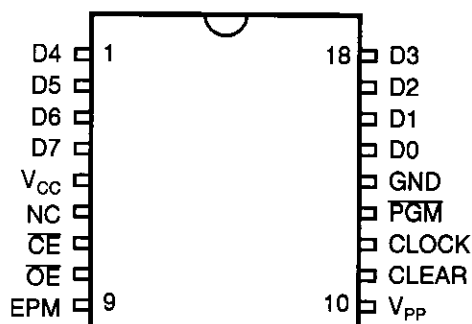


Figure 3. 18-Pin EPROM Mode Configuration

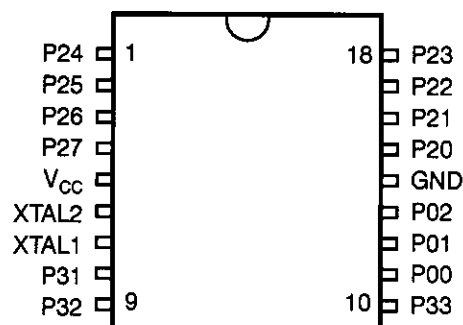


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode			
Pin #	Symbol	Function	Direction
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V <sub>CC</sub>	Power Supply	
6	NC	No Connection	
7	CE	Chip Enable	Input
8	OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V <sub>PP</sub>	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	PGM	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0,1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode			
Pin #	Symbol	Function	Direction
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V <sub>CC</sub>	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

## DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I <sub>CC1</sub>	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 4 MHz	7
I <sub>CC2</sub>	Standby Current	4.5V		10.0	1.0	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	7,8
		5.5V		10.0	1.0	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	7,8
I <sub>ALL</sub>	Auto Latch Low Current	4.5V		32.0	16	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
		5.5V		32.0	16	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
I <sub>ALH</sub>	Auto Latch High Current	4.5V		-16.0	-8.0	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
		5.5V		-16.0	-8.0	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	

## Notes:

- Port 2 and Port 0 only
- V<sub>SS</sub> = 0V = GND
- The device operates down to V<sub>LV</sub> of the specified frequency for V<sub>LV</sub>. The minimum operational V<sub>CC</sub> is determined on the value of the voltage V<sub>LV</sub> at the ambient temperature. The V<sub>LV</sub> increases as the temperature decreases.
- V<sub>CC</sub> = 4.5 to 5.5V, typical values measured at V<sub>CC</sub> = 5.0V.  
The V<sub>CC</sub> voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V<sub>CC</sub> = 5.0V.
- Standard Mode (not Low EMI Mode)
- Z86E08 only
- All outputs unloaded and all inputs are at V<sub>CC</sub> or V<sub>SS</sub> level.
- If analog comparator is selected, then the comparator inputs must be at V<sub>CC</sub> level.

## DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I <sub>CC</sub>	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I <sub>CC1</sub>	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 12 MHz	5,7
I <sub>CC</sub>	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

**AC ELECTRICAL CHARACTERISTICS**

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

Standard Temperature

15		$T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$							
No	Symbol	Parameter	$V_{CC}$	8 MHz		12 MHz		Units	Notes
				Min	Max	Min	Max		
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC, Tfc	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

**Notes:**

1. Timing Reference uses 0.7  $V_{CC}$  for a logic 1 and 0.2  $V_{CC}$  for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

**AC ELECTRICAL CHARACTERISTICS**

Low Noise Mode, Standard Temperature

No	Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0 °C to +70 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

**Notes:**

1. Timing Reference uses 0.7 V<sub>CC</sub> for a logic 1 and 0.2 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).



# AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

No	Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = −40 °C to +105 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V	25		25		ns	1
			5.5V	25		25		ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V	100		100		ns	1
			5.5V	100		100		ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

## Notes:

1. Timing Reference uses 0.7 V<sub>CC</sub> for a logic 1 and 0.2 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

## PIN FUNCTIONS (Continued)

**XTAL1, XTAL2** *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

**Port 0, P02–P00.** Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

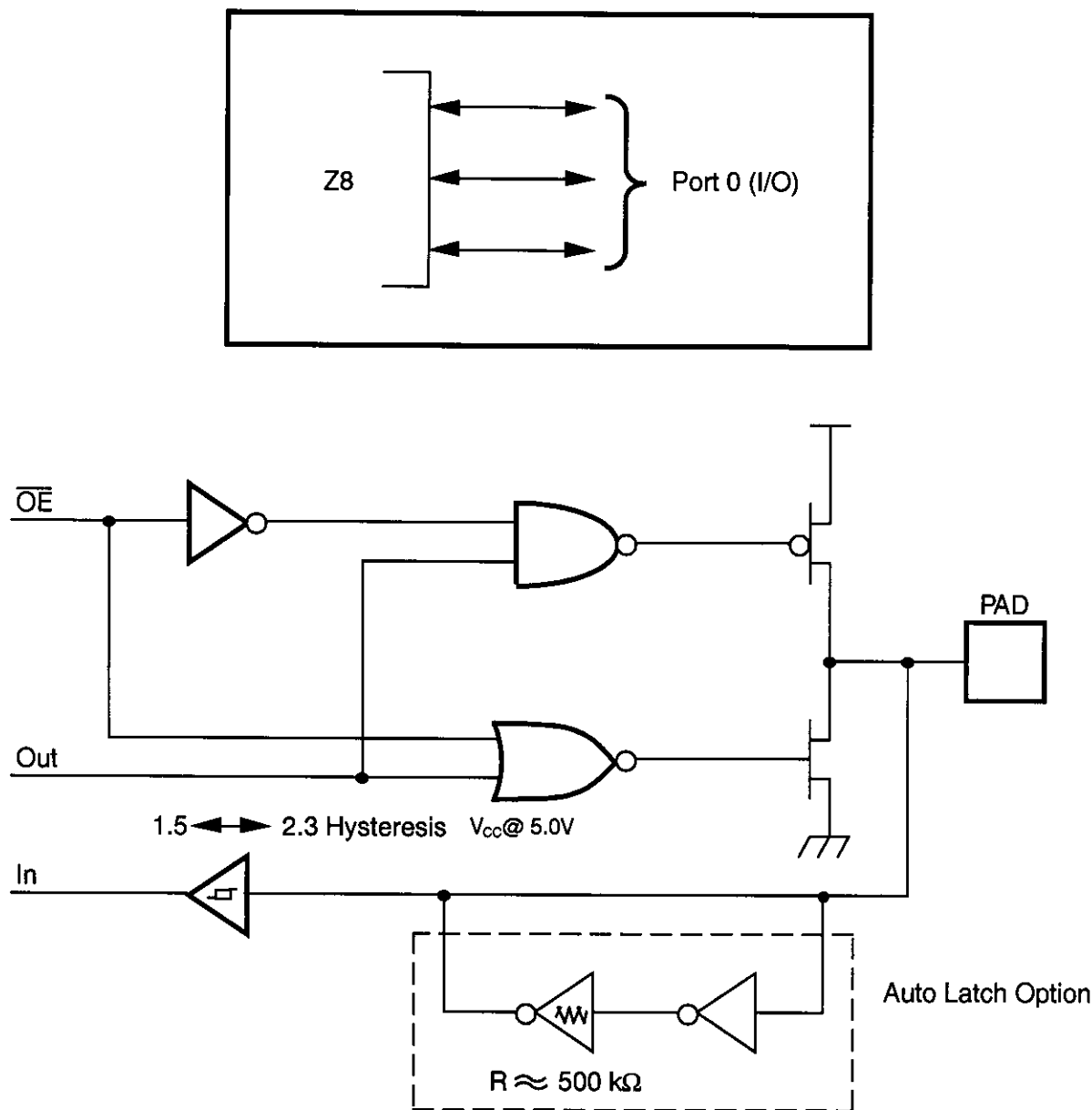
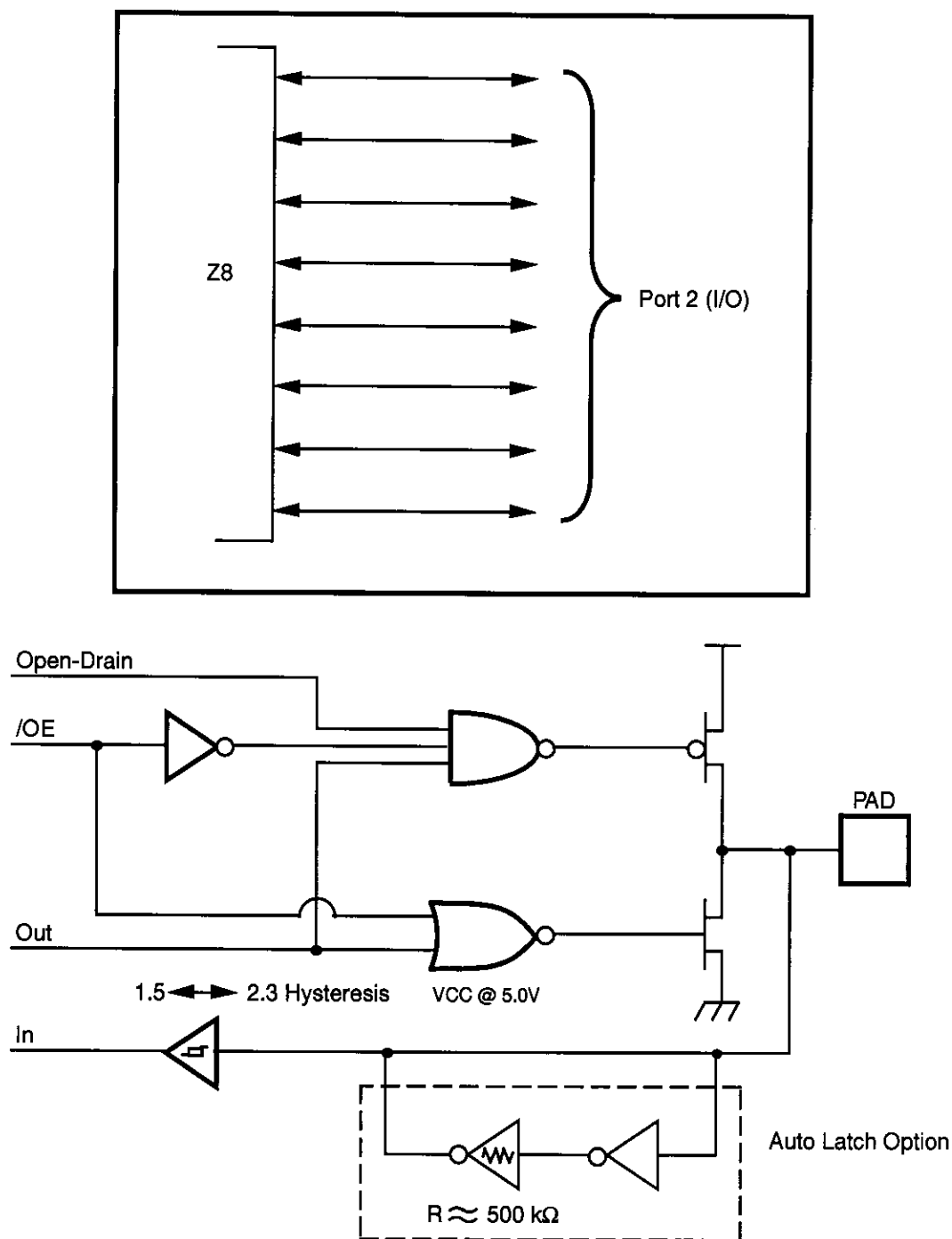


Figure 7. Port 0 Configuration

**Port 2, P27–P20.** Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software

control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).



**Figure 8. Port 2 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the  $V_{CC}$  is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or  $T_{IN}$  through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

**RESET.** This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for  $T_{POR}$  ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

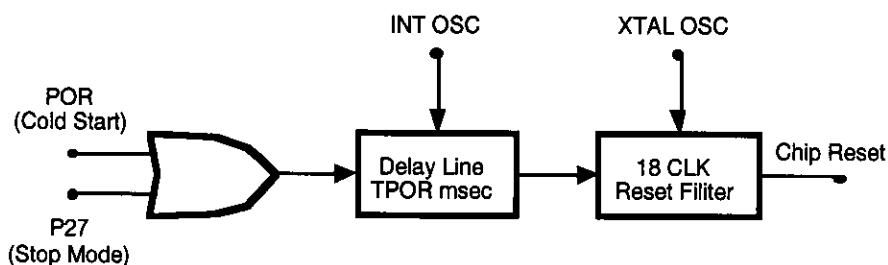


Figure 10. Internal Reset Configuration

**Power-On Reset (POR).** A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows  $V_{CC}$  and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

**Watch-Dog Timer Reset.** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

**Program Memory.** The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

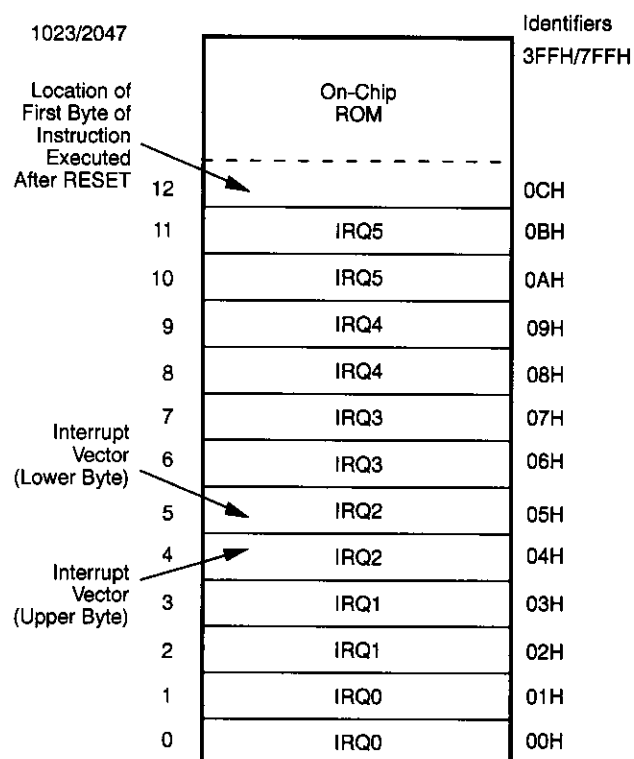


Figure 11. Program Memory Map

**Register File.** The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

Location	Identifiers
255 (FFH)	Stack Pointer (Bits 7-0) SPL
254 (FE)	General-Purpose Register GPR
253 (FD)	Register Pointer RP
252 (FC)	Program Control Flags FLAGS
251 (FB)	Interrupt Mask Register IMR
250 (FA)	Interrupt Request Register IRQ
249 (F9)	Interrupt Priority Register IPR
248 (F8)	Ports 0-1 Mode P01M
247 (F7)	Port 3 Mode P3M
246 (F6)	Port 2 Mode P2M
245 (F5)	T0 Prescaler PRE0
244 (F4)	Timer/Counter 0 T0
243 (F3)	T1 Prescaler PRE1
242 (F2)	Timer/Counter 1 T1
241 (F1H)	Timer Mode TMR
128	Not Implemented
127 (7FH)	General-Purpose Registers
4	
3	Port 3 P3
2	Port 2 P2
1	Reserved P1
0 (00H)	Port 0 P0

Figure 12. Register File

## FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

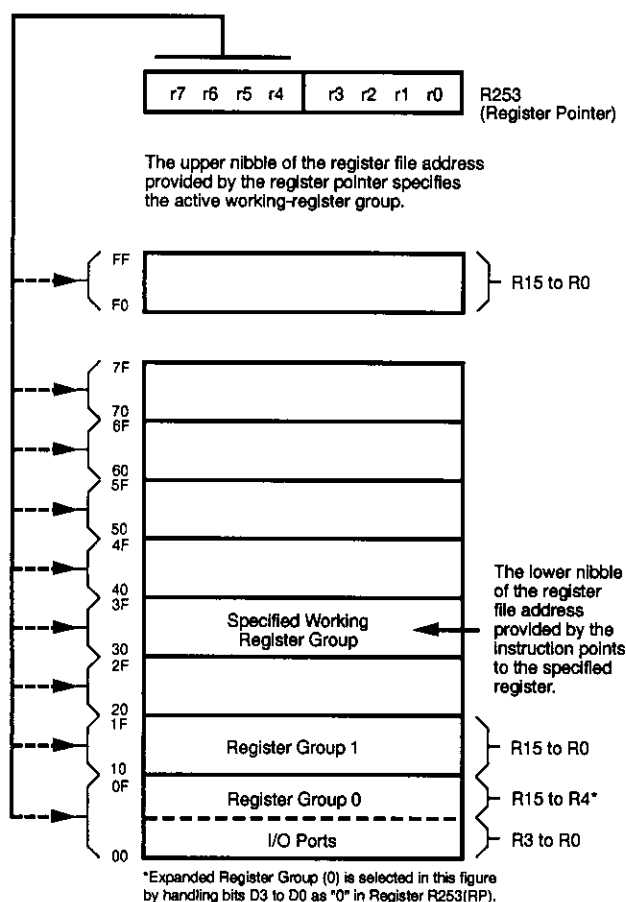


Figure 13. Register Pointer

**Stack Pointer.** The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

**General-Purpose Registers (GPR).** These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the  $V_{CC}$  voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

**Counter/Timer.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

**Note:** User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

**Notes:**

F = Falling edge triggered

R = Rising edge triggered

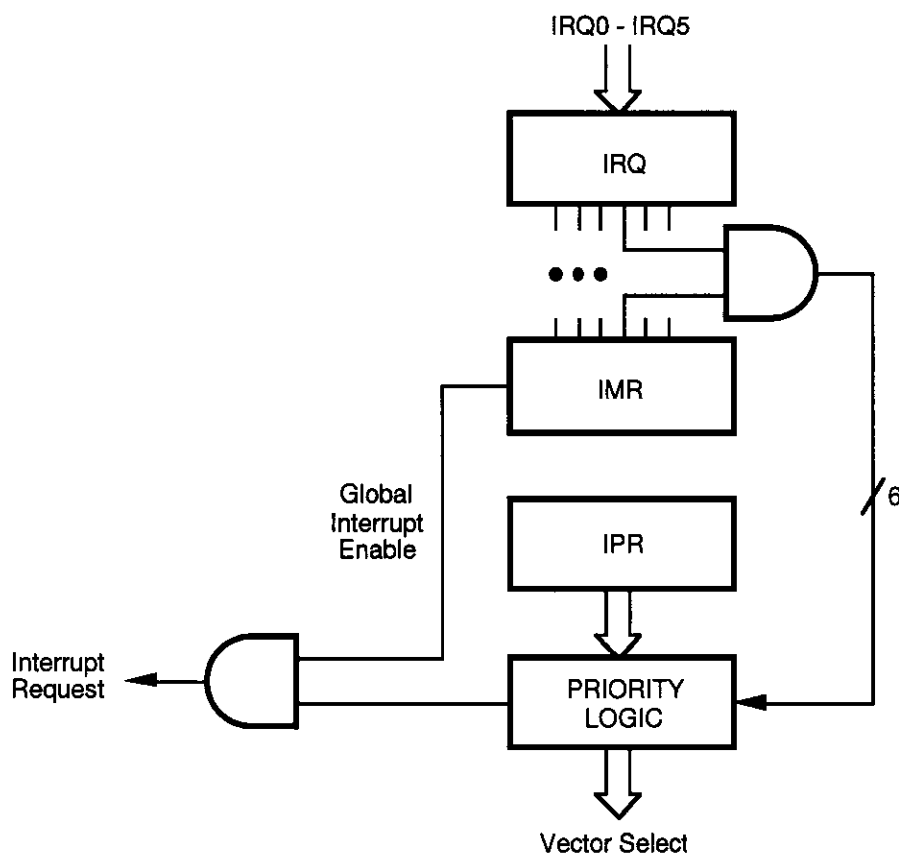


Figure 15. Interrupt Block Diagram

# FUNCTIONAL DESCRIPTION (Continued)

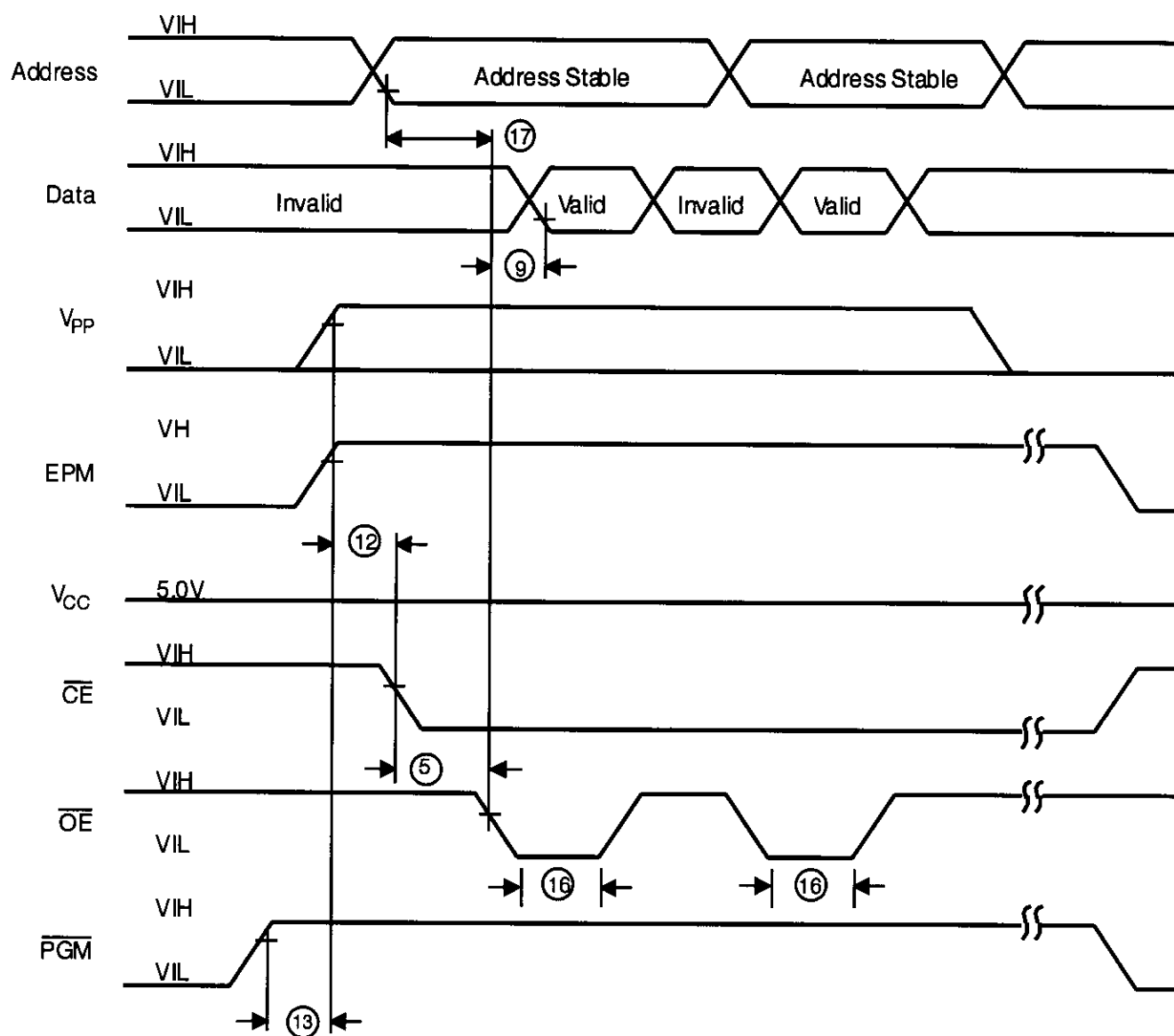


Figure 19. Z86E04/E08 Programming Waveform  
(EPROM Read)



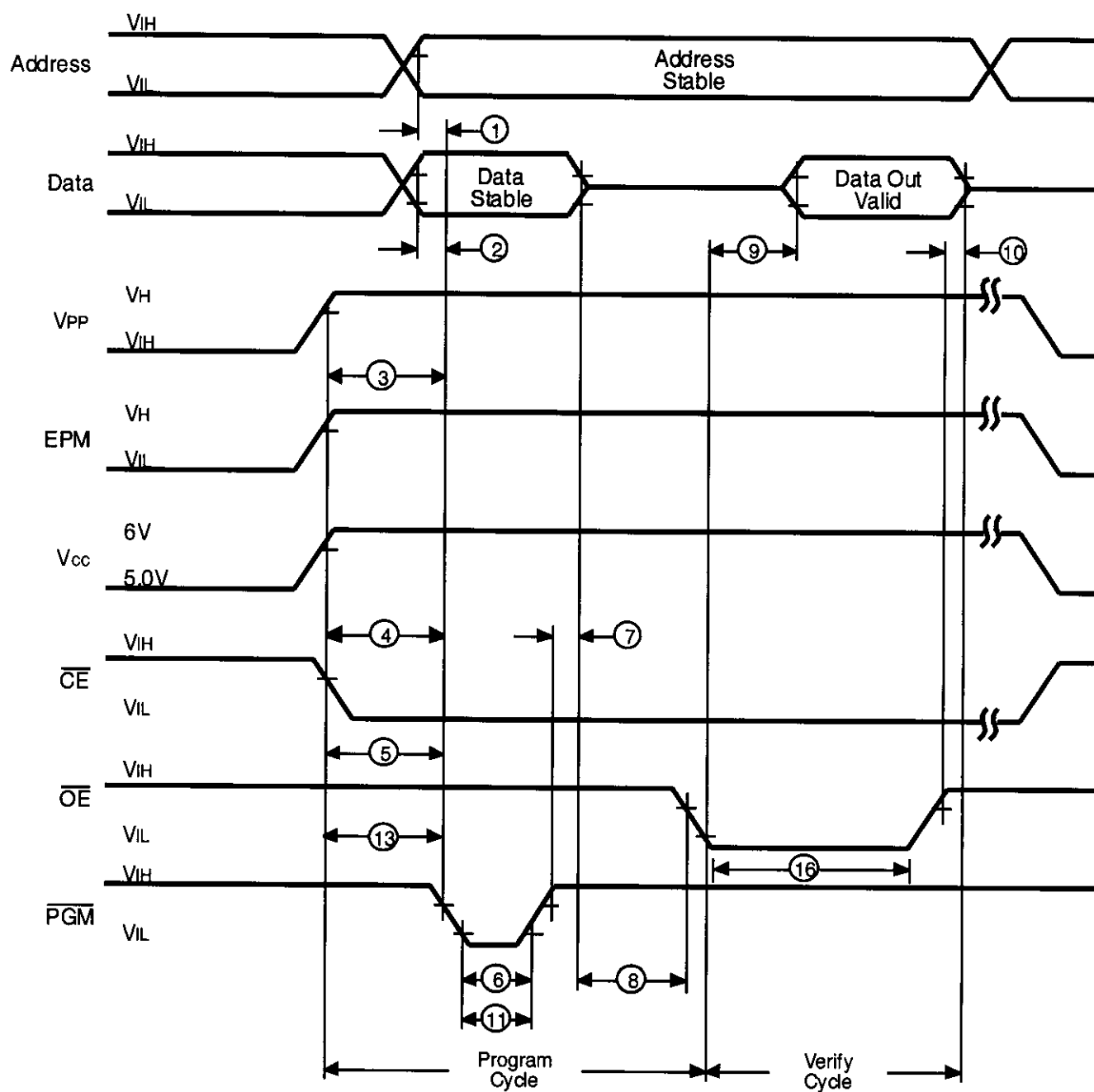


Figure 20. Z86E04/E08 Programming Waveform  
(Program and Verify)

# FUNCTIONAL DESCRIPTION (Continued)

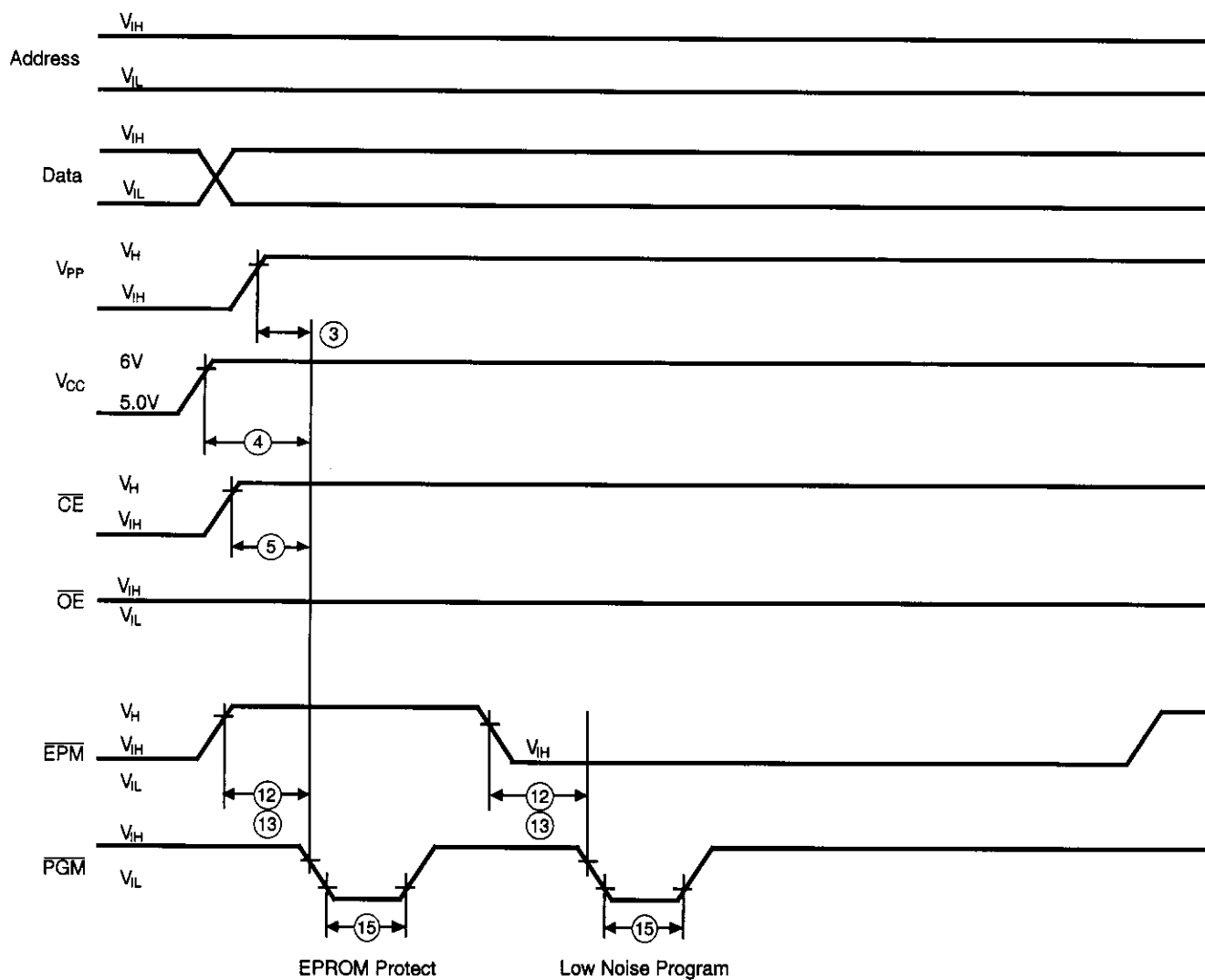
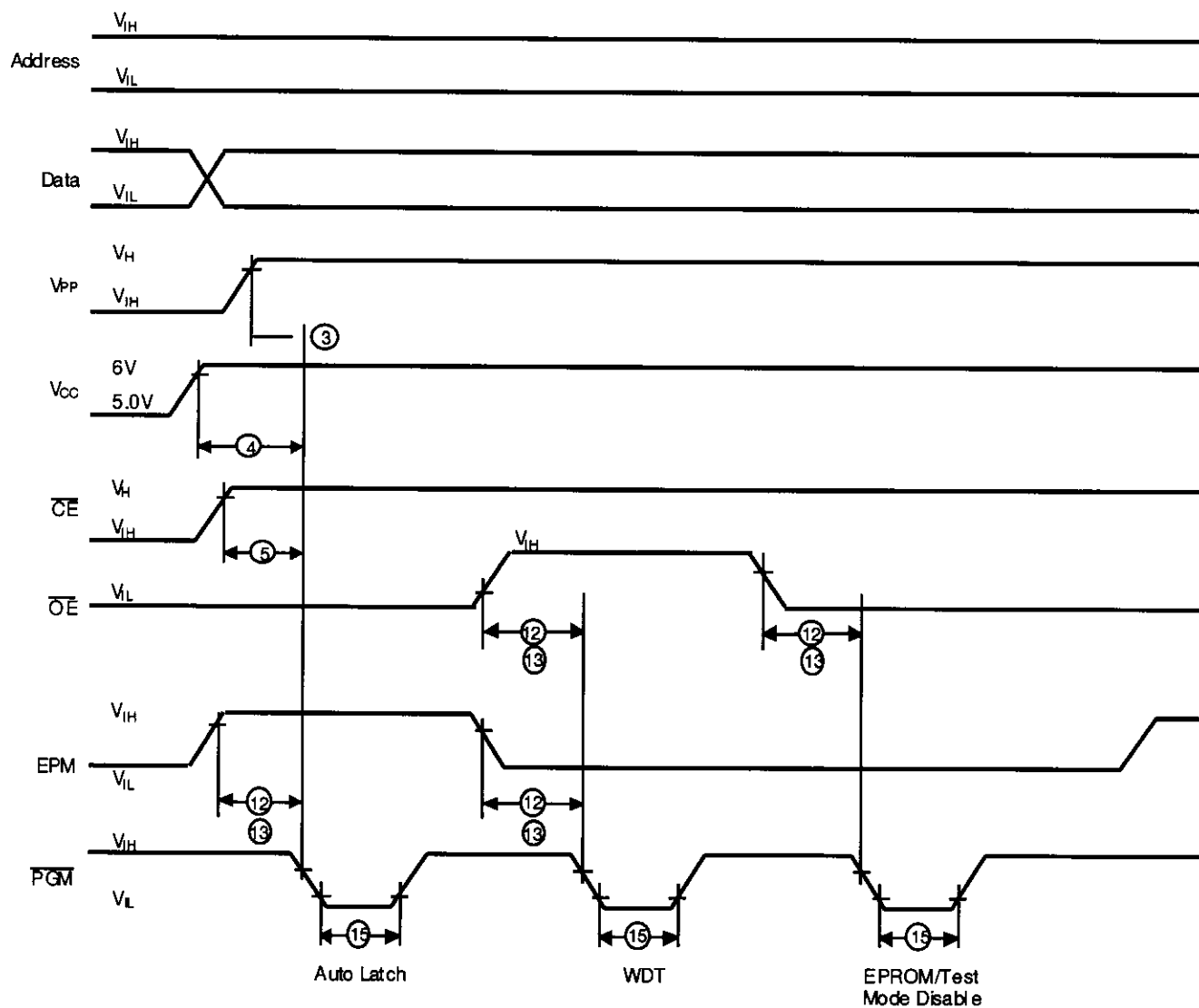


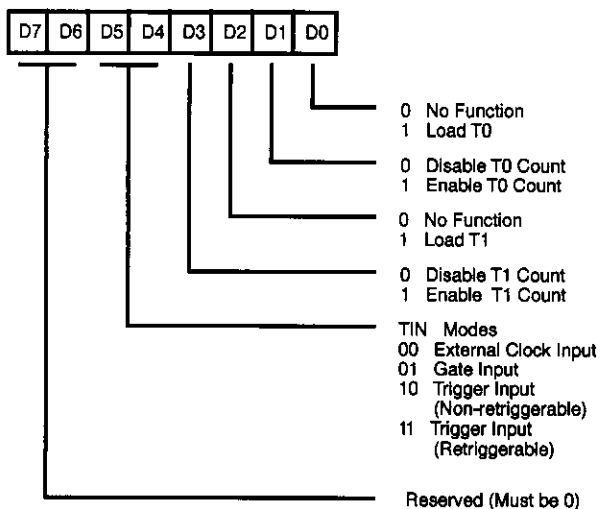
Figure 21. Z86E04/E08 Programming Options Waveform  
(EPROM Protect and Low Noise Program)



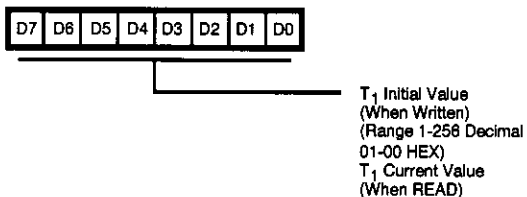
**Figure 22. Z86E04/E08 Programming Options Waveform  
(Auto Latch Disable, Permanent WDT Enable and  
EPROM/Test Mode Disable)**

## Z8 CONTROL REGISTERS

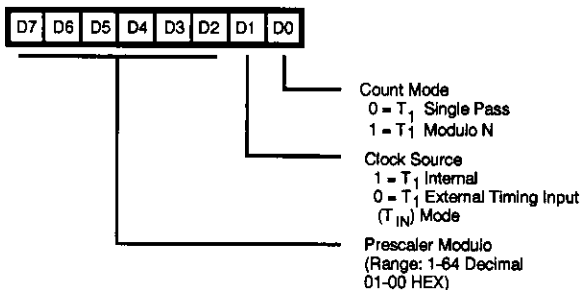
R241 TMR

Figure 24. Timer Mode Register (F1<sub>H</sub>: Read/Write)

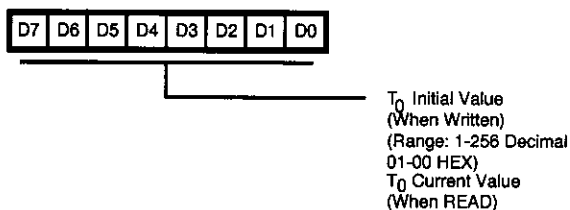
R242 T1

Figure 25. Counter Timer 1 Register (F2<sub>H</sub>: Read/Write)

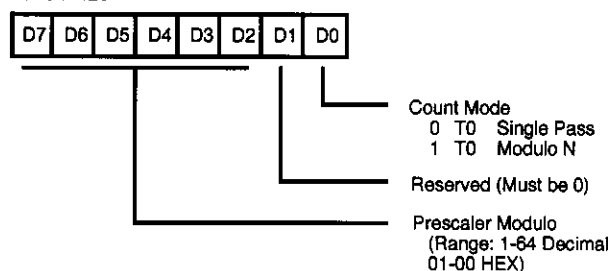
R243 PRE1

Figure 26. Prescaler 1 Register (F3<sub>H</sub>: Write Only)

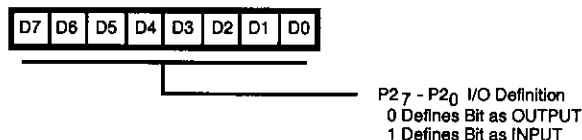
R244 T0

Figure 27. Counter/Timer 0 Register (F4<sub>H</sub>: Read/Write)

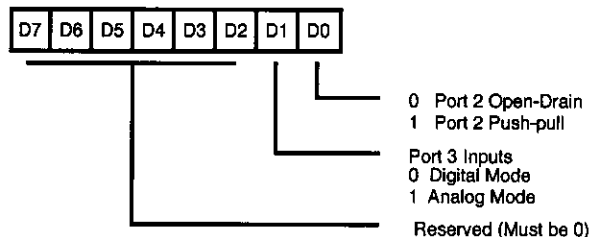
R245 PRE0

Figure 28. Prescaler 0 Register (F5<sub>H</sub>: Write Only)

R246 P2M

Figure 29. Port 2 Mode Register (F6<sub>H</sub>: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7<sub>H</sub>: Write Only)

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