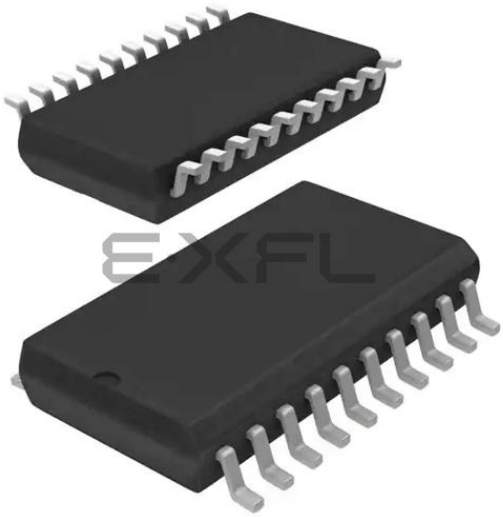

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812hec1903

PIN DESCRIPTION

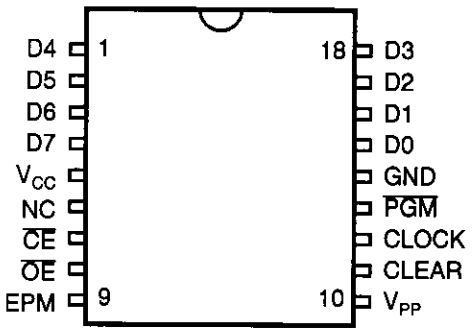


Figure 3. 18-Pin EPROM Mode Configuration

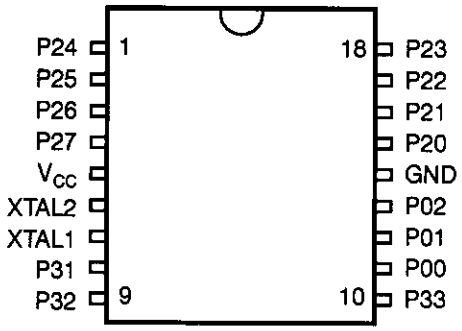


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	NC	No Connection	
7	$\overline{CE}$	Chip Enable	Input
8	$\overline{OE}$	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	$\overline{PGM}$	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0,1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

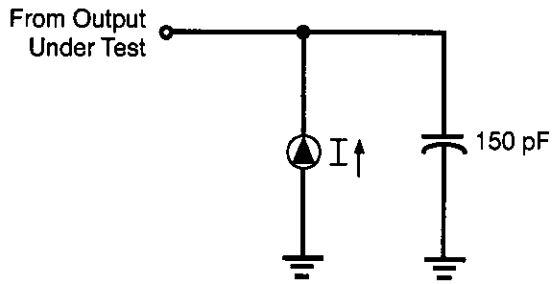


Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Standard Temperature

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{INMAX}	Max Input Voltage	4.5V		12		V	I_{In}<250 µA	1
		5.5V		12		V	I_{In}<250 µA	1
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		4.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	4.5V		0.8	0.1	V	I_{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	4.5V		0.8	0.8	V	I_{OL} = +12 mA,	5
		5.5V		0.8	0.8	V	I_{OL} = +12 mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		2.2	3.0	2.8	V	@ 6 MHz Max. Int. CLK Freq.	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS

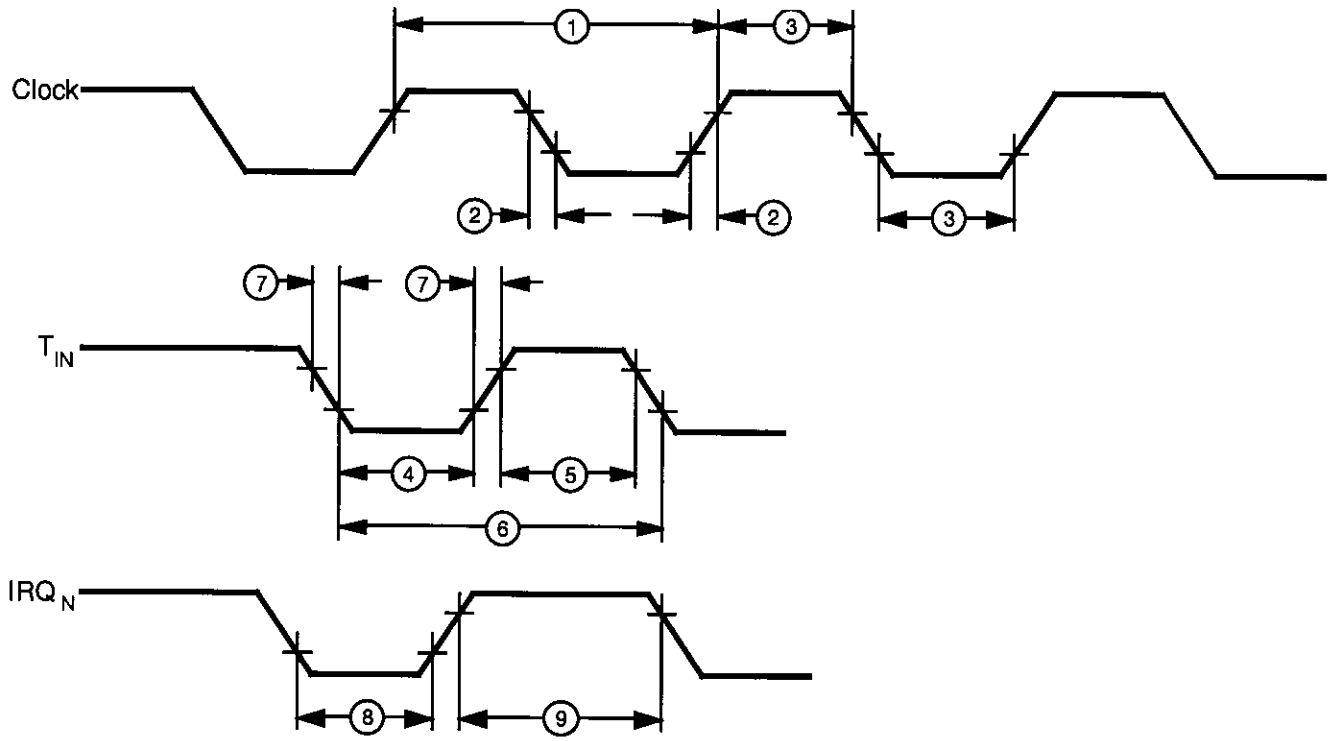


Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C						
				8 MHz		12 MHz				
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode, Standard Temperature

				T_A= 0 °C to +70 °C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

				T_A= –40 °C to +105 °C					
				1 MHz		4 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V		4TpC	4TpC			1
			5.5V		4TpC	4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

V_{CC} *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

$\overline{CE}$ *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

$\overline{PGM}$ *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the V_{PP}, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

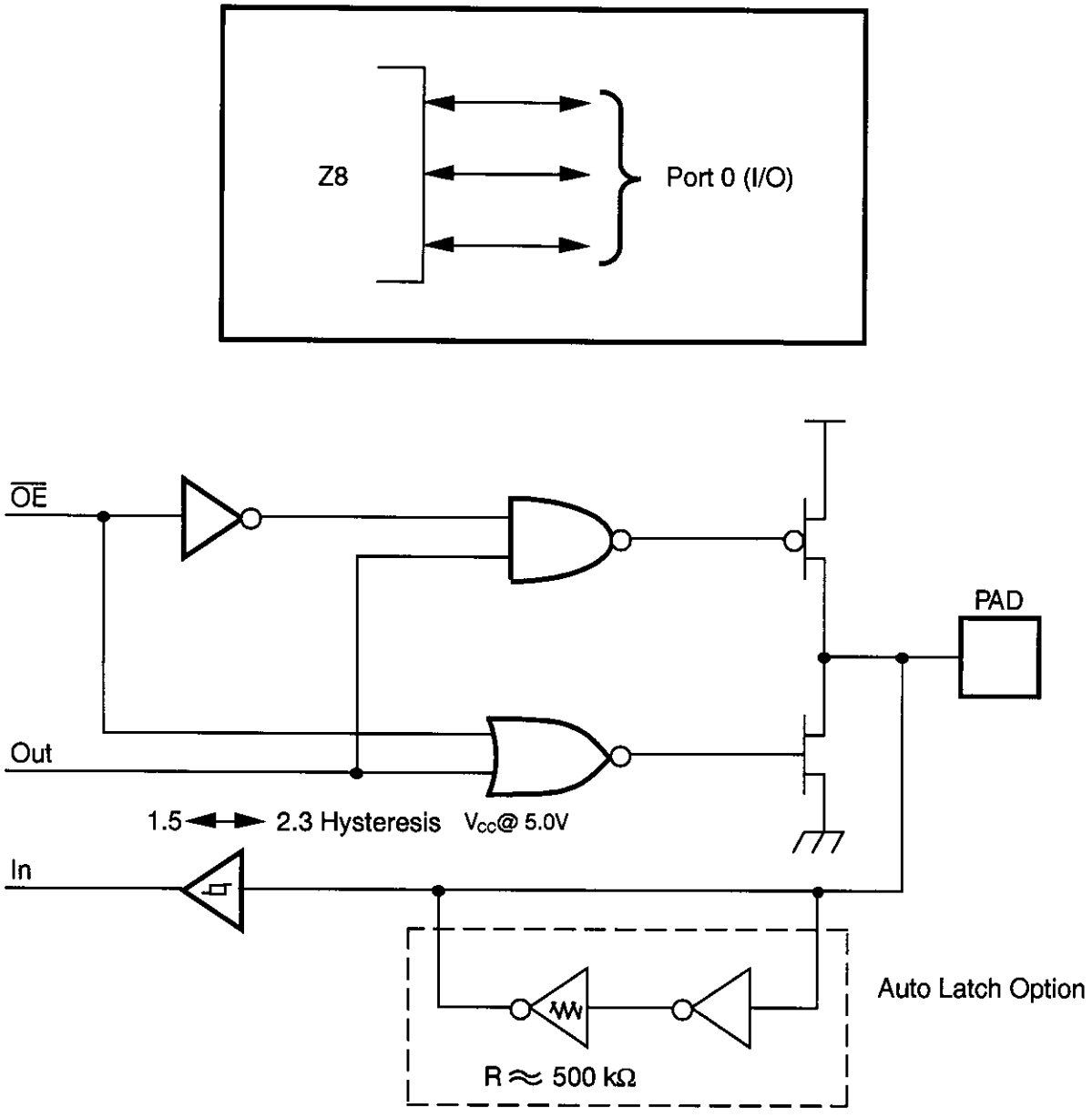


Figure 7. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).

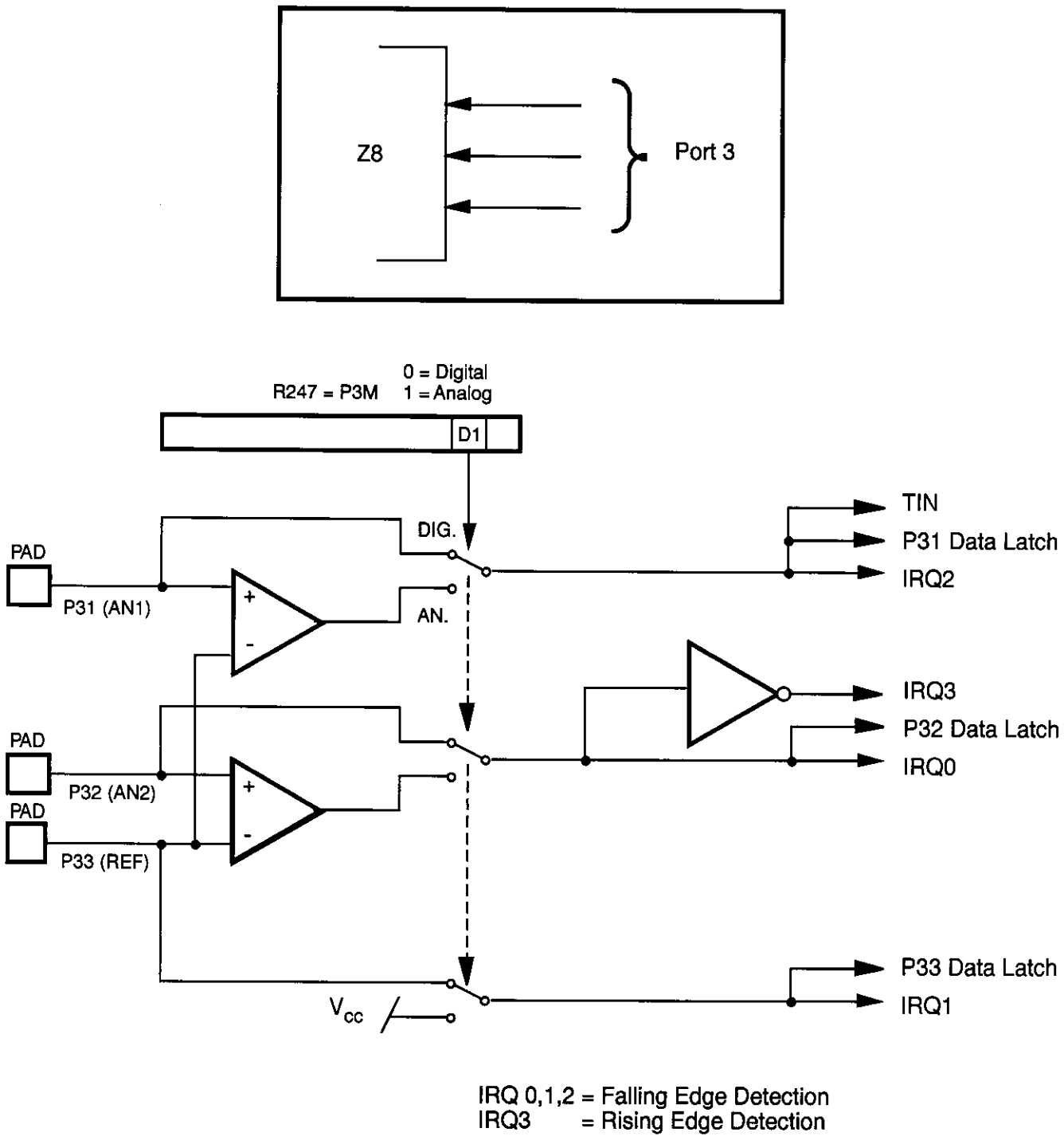


Figure 9. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

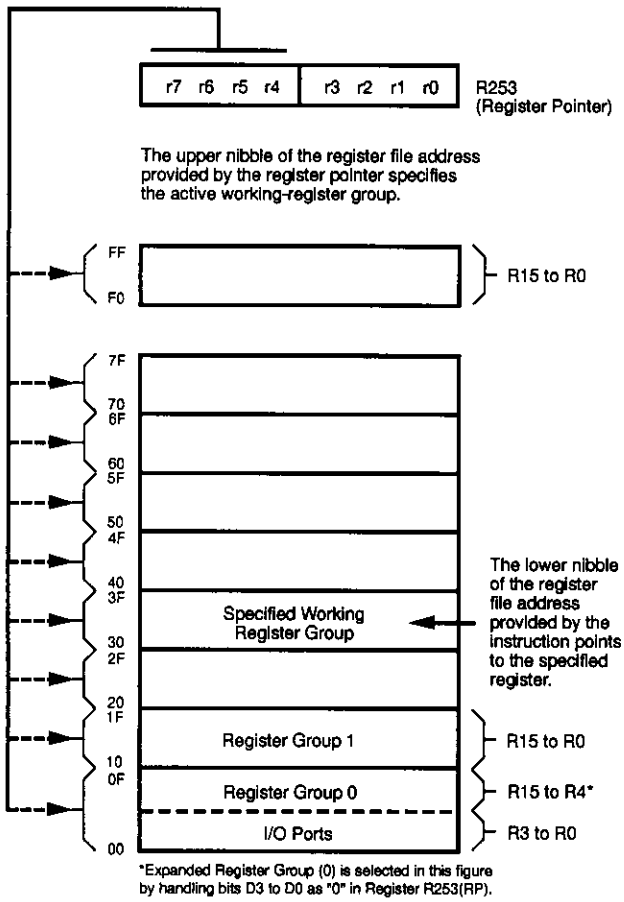


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

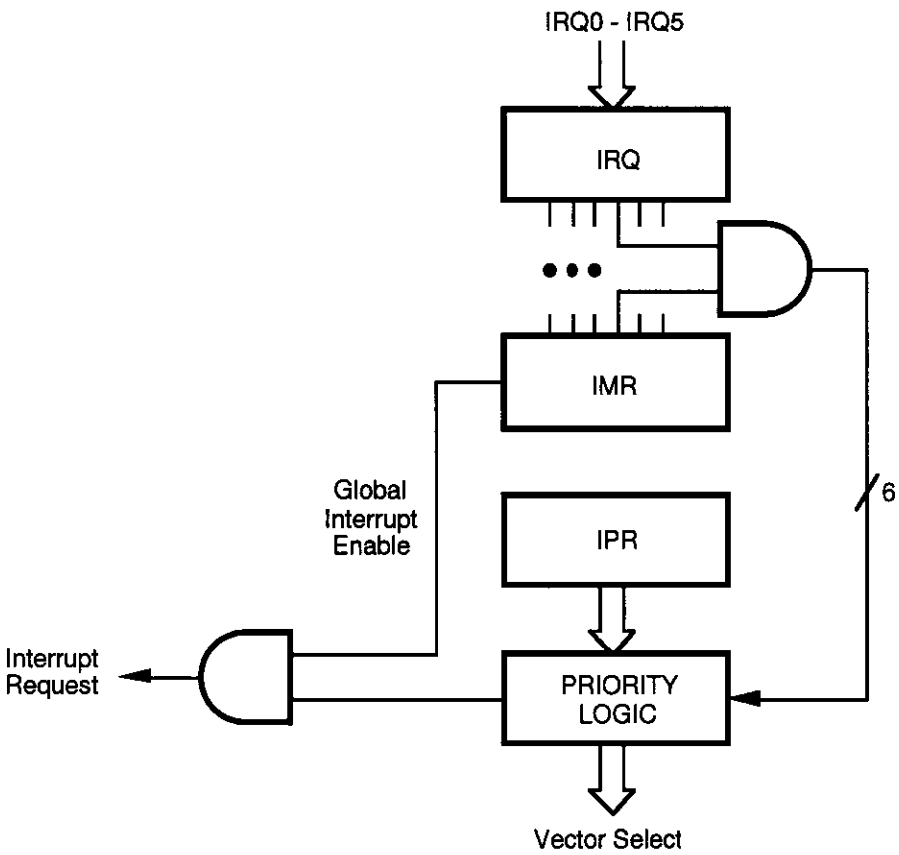


Figure 15. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

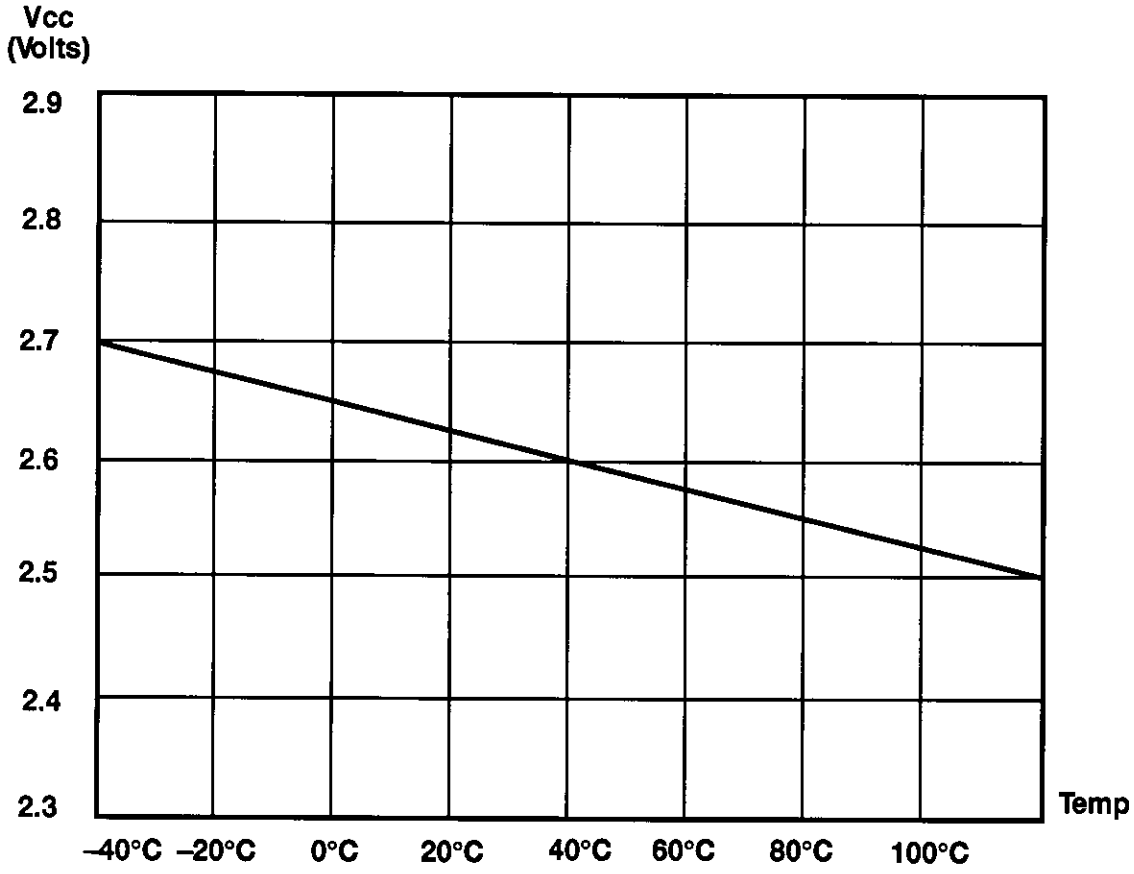
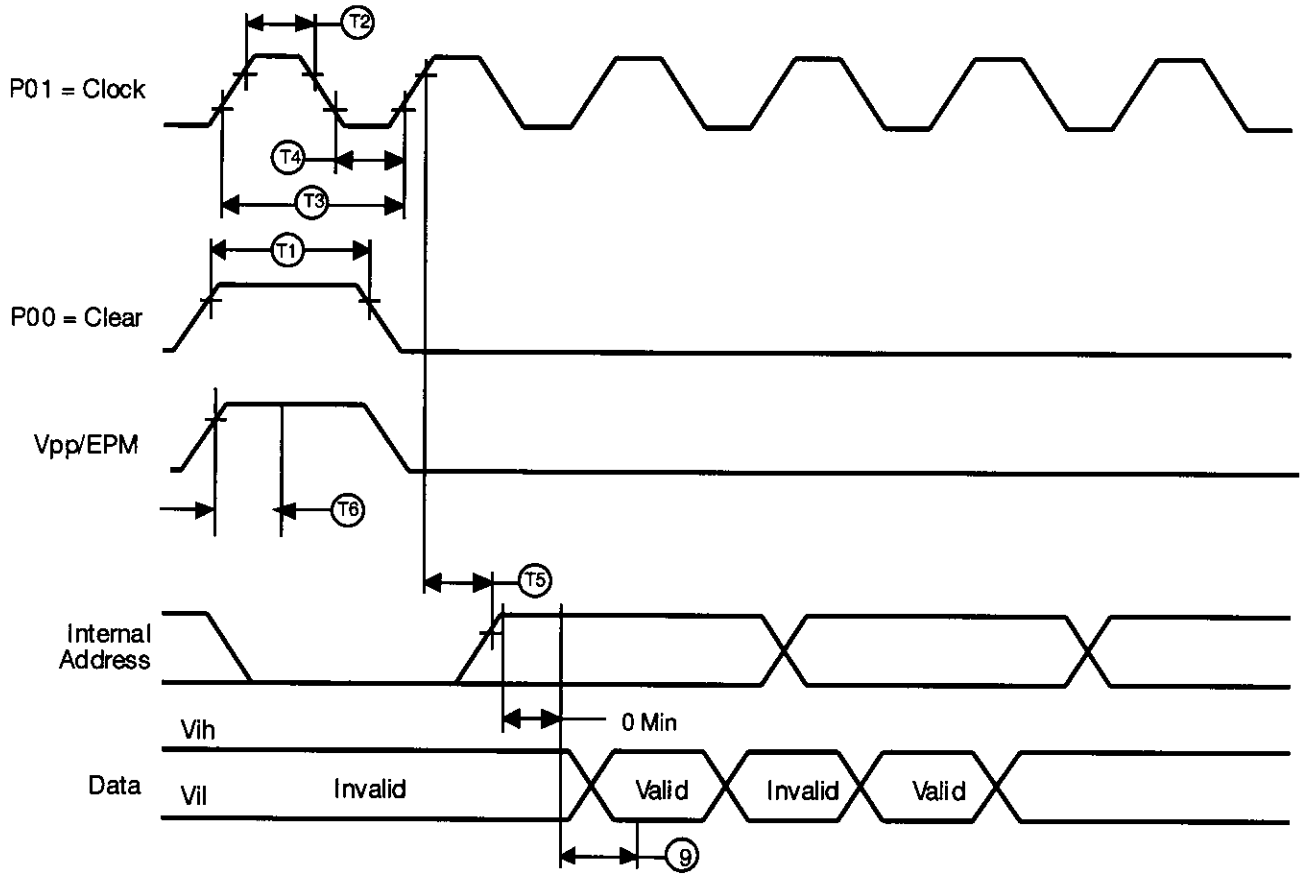


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 µs Min

Figure 18. Z86E04/E08 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

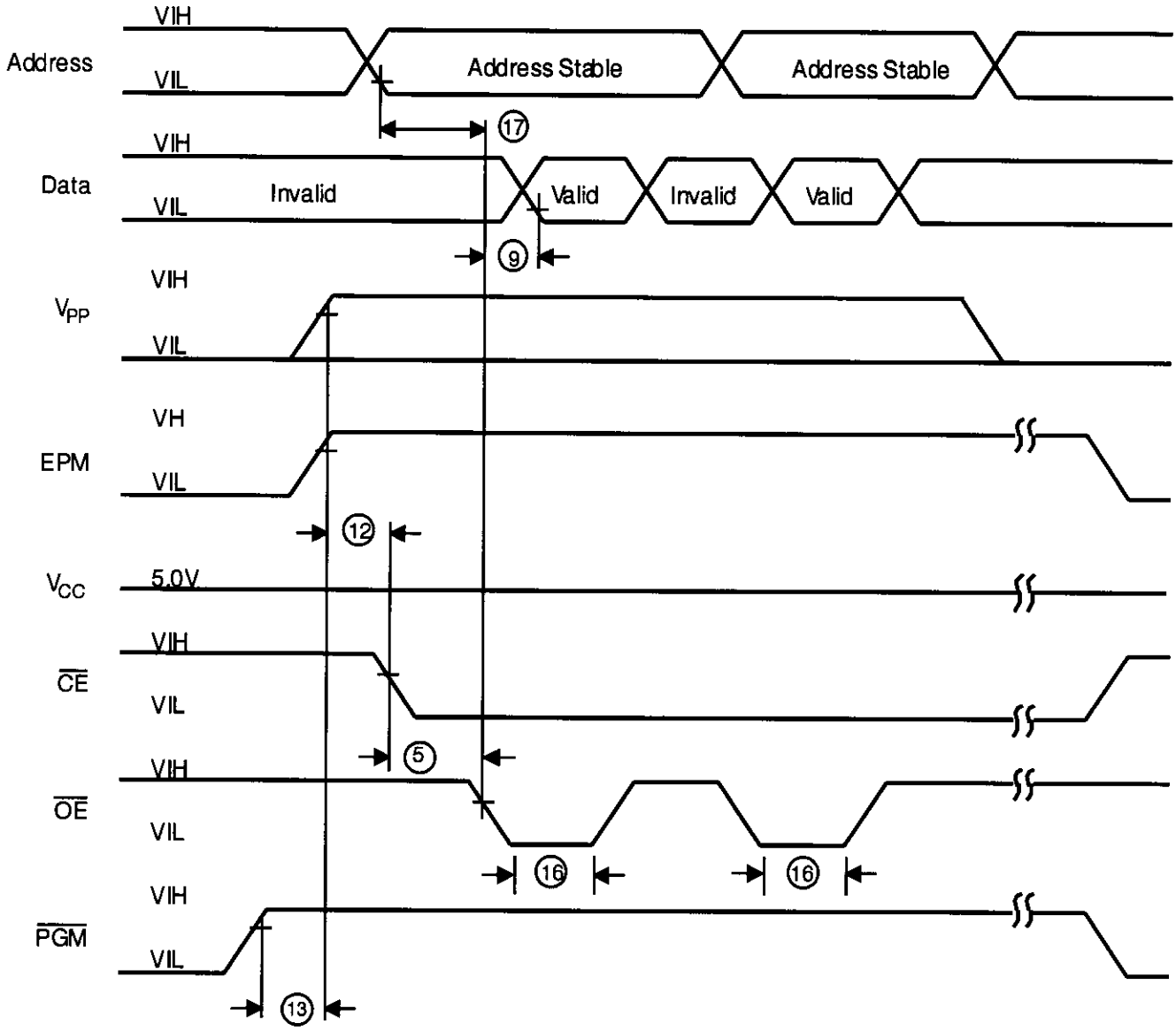


Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)

FUNCTIONAL DESCRIPTION (Continued)

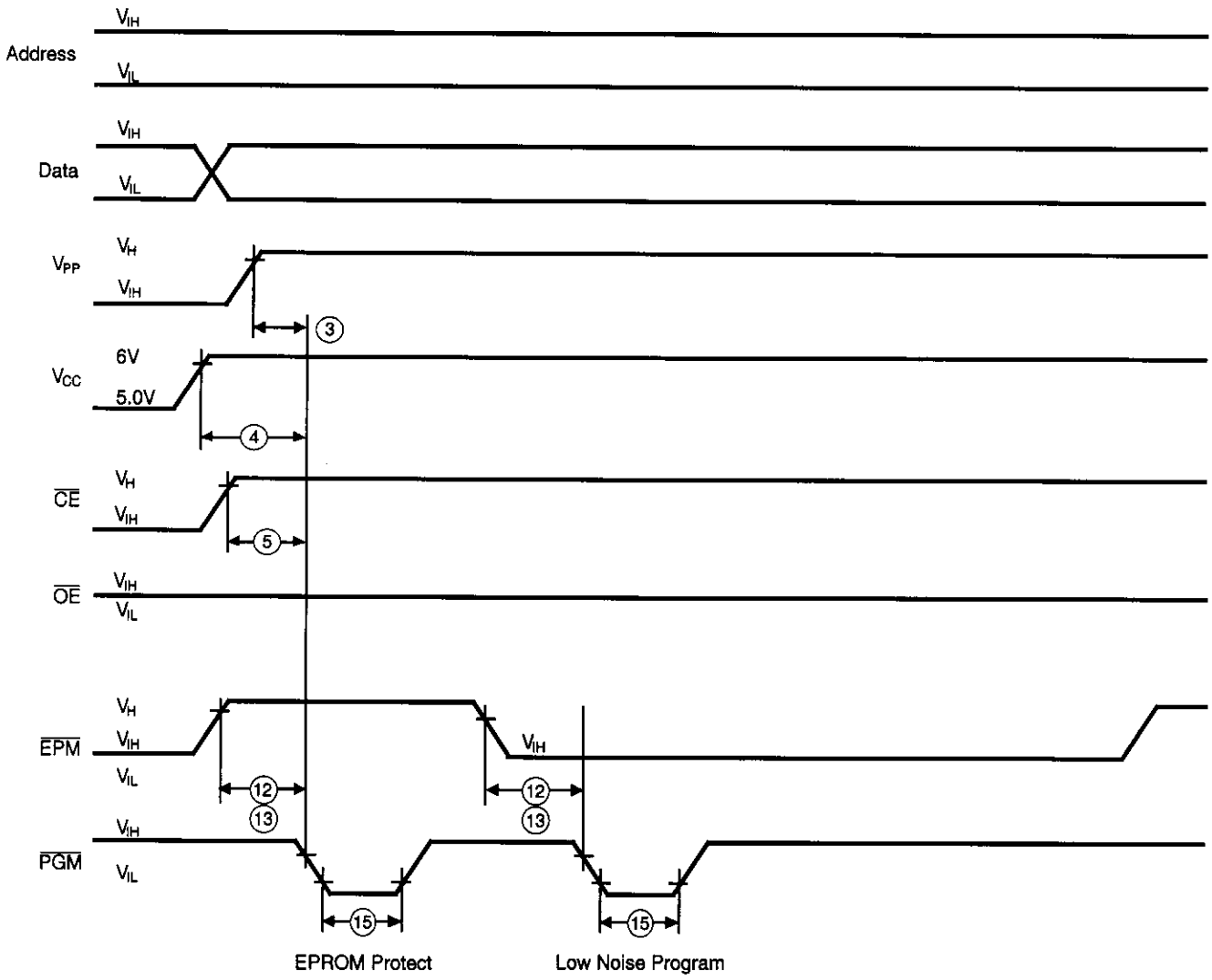


Figure 21. Z86E04/E08 Programming Options Waveform (EPROM Protect and Low Noise Program)

Z8 CONTROL REGISTERS

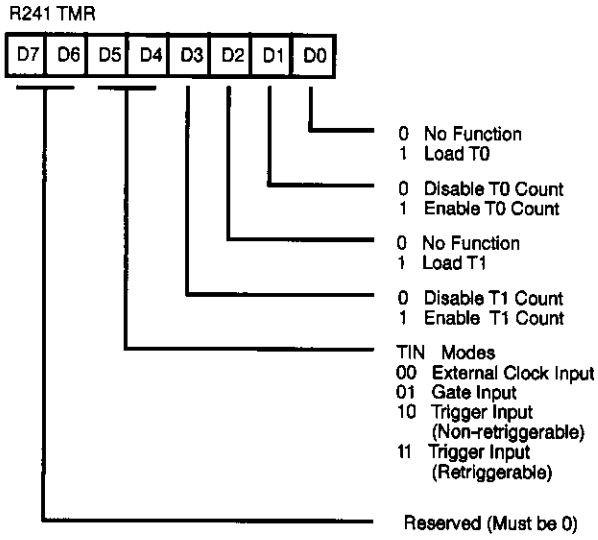


Figure 24. Timer Mode Register ($F1_H$: Read/Write)

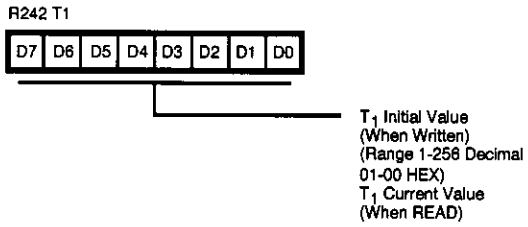


Figure 25. Counter Timer 1 Register ($F2_H$: Read/Write)

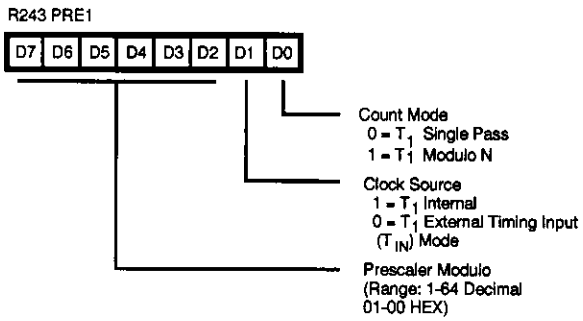


Figure 26. Prescaler 1 Register ($F3_H$: Write Only)

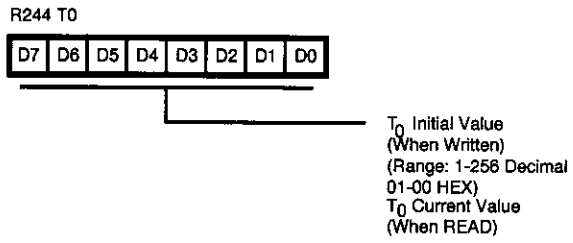


Figure 27. Counter/Timer 0 Register ($F4_H$: Read/Write)

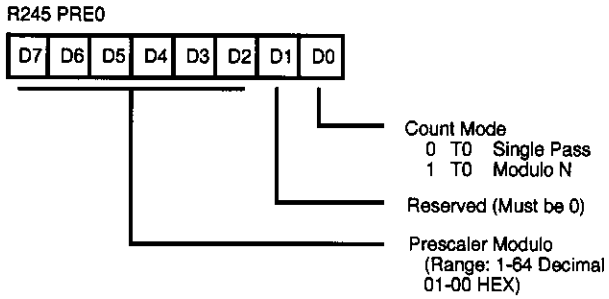


Figure 28. Prescaler 0 Register ($F5_H$: Write Only)

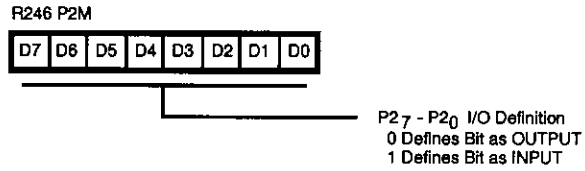


Figure 29. Port 2 Mode Register ($F6_H$: Write Only)

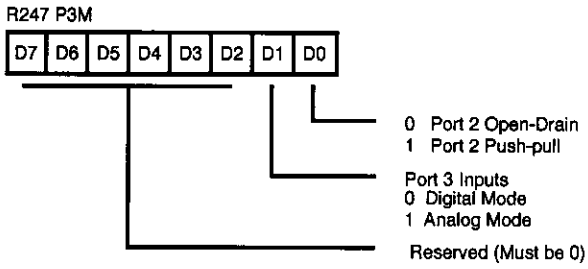


Figure 30. Port 3 Mode Register ($F7_H$: Write Only)