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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812hsc1866tr

FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
 - Low Noise
 - ROM Protect
 - Auto Latch
 - Watch-Dog Timer (WDT)
 - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1 μ s @ 12 MHz)
- RAM Bytes (125)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8[®] MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All Signals with an overline, " $\overline{}$ ", are active Low, for example: $\overline{B/W}$ (WORD is active Low); $\overline{B}/W$ (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

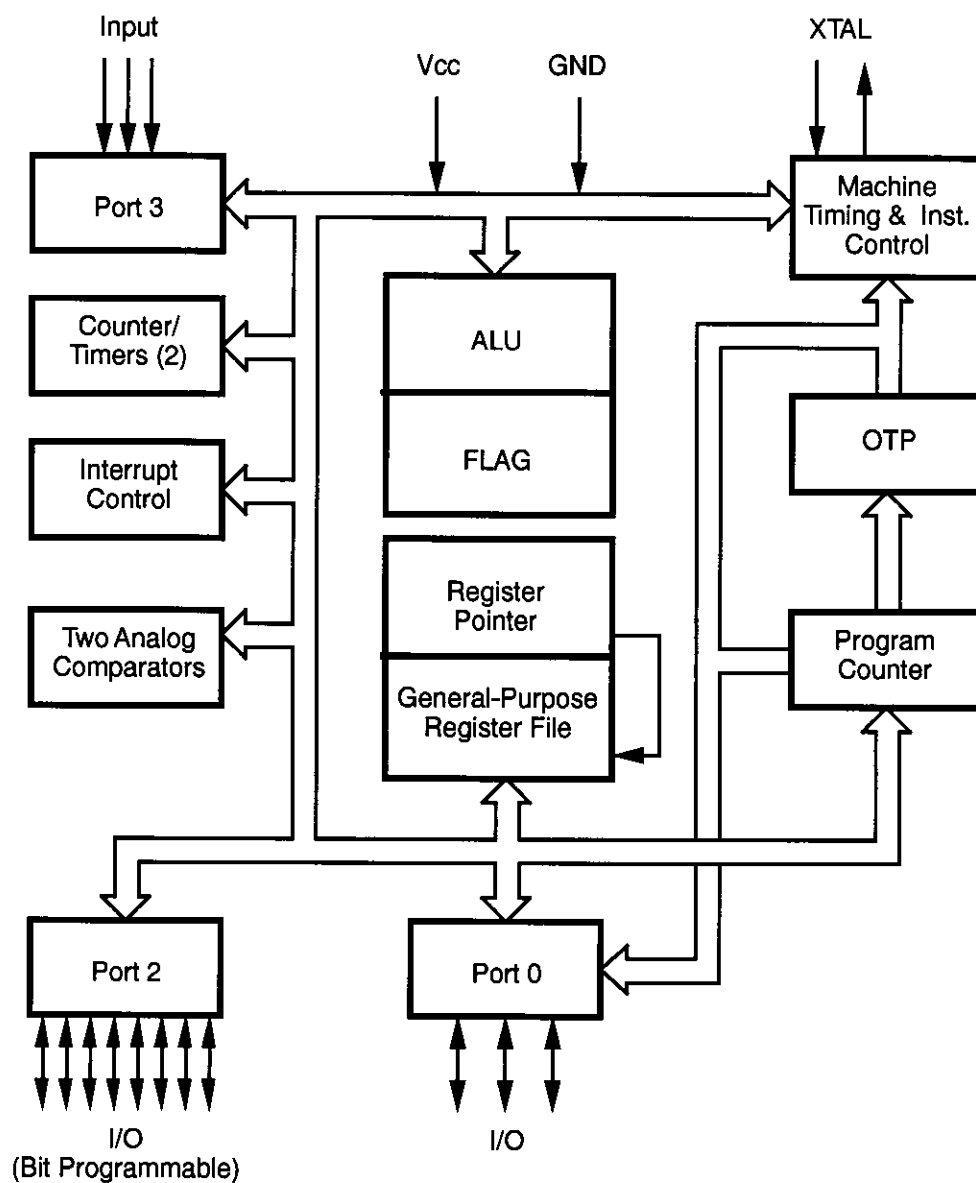


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power

dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	-40	+105	C	
Storage Temperature	-65	+150	C	
Voltage on any Pin with Respect to V_{SS}	-0.7	+12	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	-0.3	+7	V	
Voltage on Pins 7, 8, 9, 10 with Respect to V_{SS}	-0.6	$V_{DD}+1$	V	2
Total Power Dissipation		1.65	W	
Maximum Allowable Current out of V_{SS}		300	mA	
Maximum Allowable Current into V_{DD}		220	mA	
Maximum Allowable Current into an Input Pin	-600	+600	μA	3
Maximum Allowable Current into an Open-Drain Pin	-600	+600	μA	4
Maximum Allowable Output Current Sunked by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Total Maximum Output Current Sunked by a Port		60	mA	
Total Maximum Output Current Sourced by a Port		45	mA	

Notes:

1. This applies to all pins except where otherwise noted. Maximum current into pin must be $\pm 600 \mu\text{A}$.
2. There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

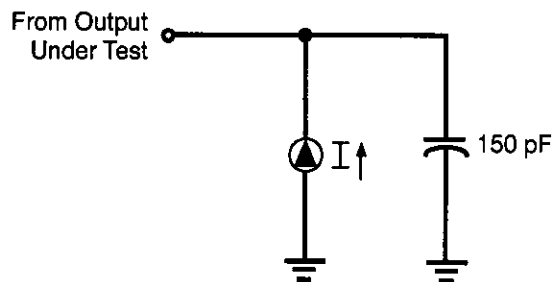


Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I _{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz	5,7
I _{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz	7
I _{CC2}	Standby Current	4.5V		20	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7,8
		5.5V		20	1.0	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	7,8
I _{ALL}	Auto Latch Low Current	4.5V		40	16	μA	0V < V _{IN} < V _{CC}	
		5.5V		40	16	μA	0V < V _{IN} < V _{CC}	
I _{ALH}	Auto Latch High Current	4.5V		-20.0	-8.0	μA	0V < V _{IN} < V _{CC}	
		5.5V		-20.0	-8.0	μA	0V < V _{IN} < V _{CC}	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS

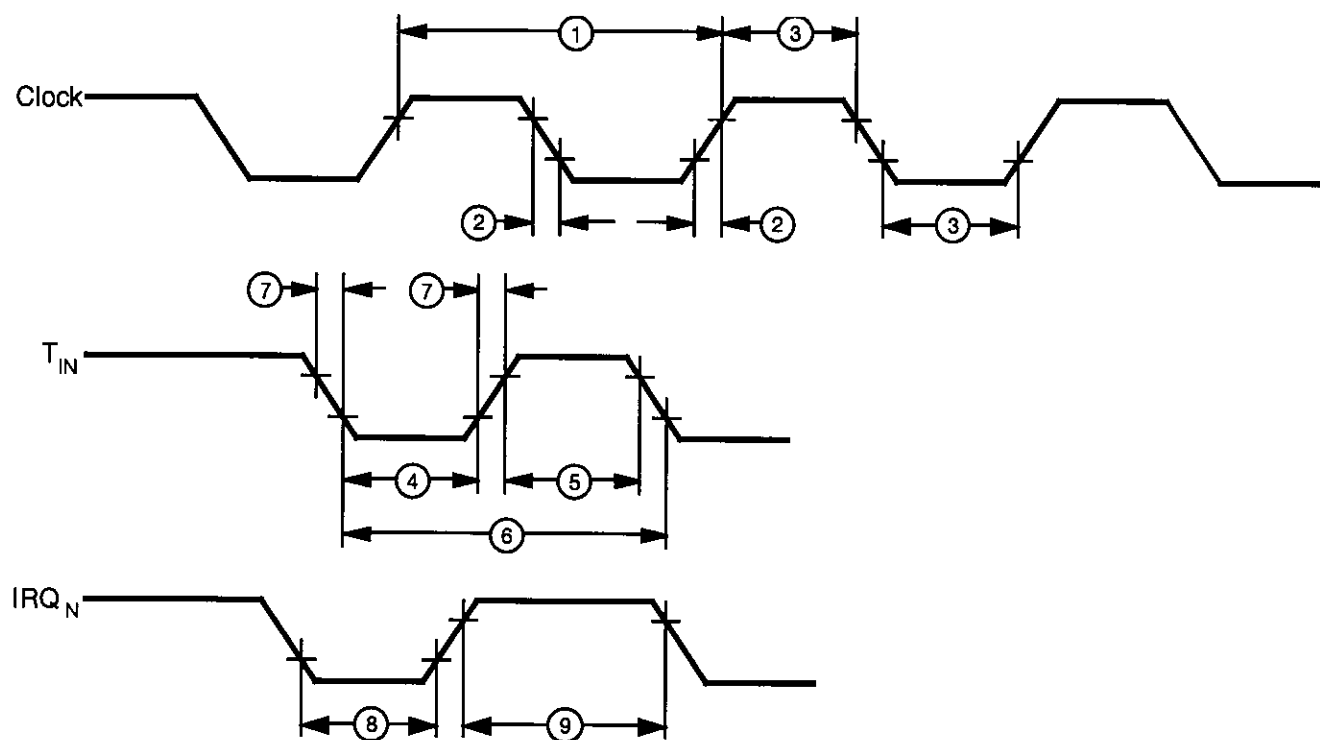


Figure 6. AC Electrical Timing Diagram

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

$\overline{CE}$ Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear Clear (active High). This pin resets the internal address counter at the High Level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one with one clock cycle.

PGM Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V_{PP}, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

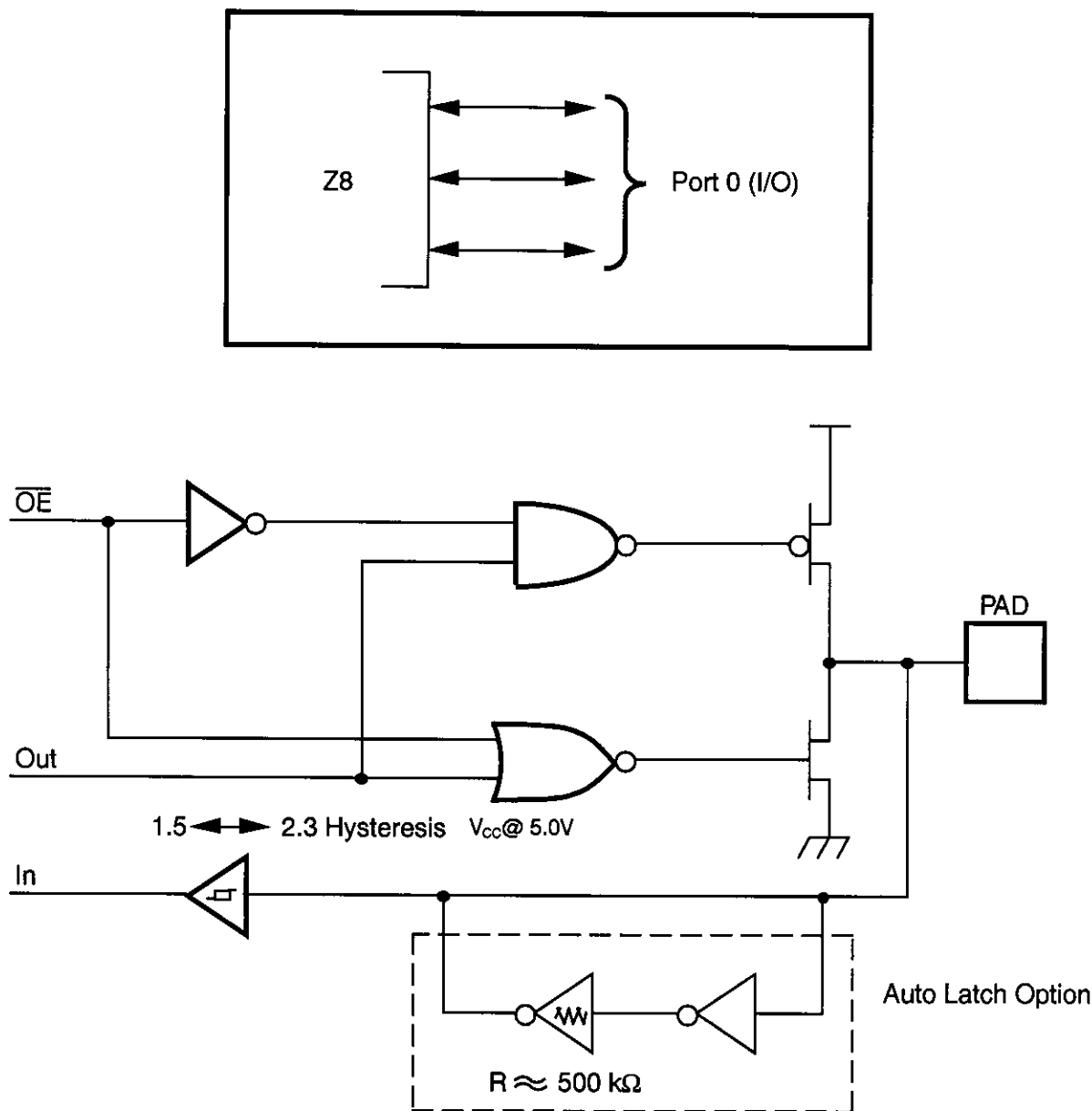


Figure 7. Port 0 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

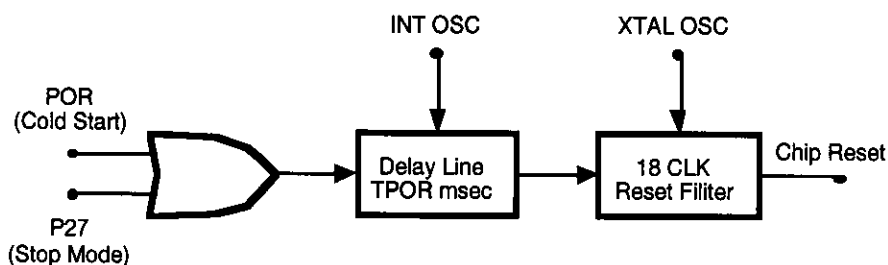


Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

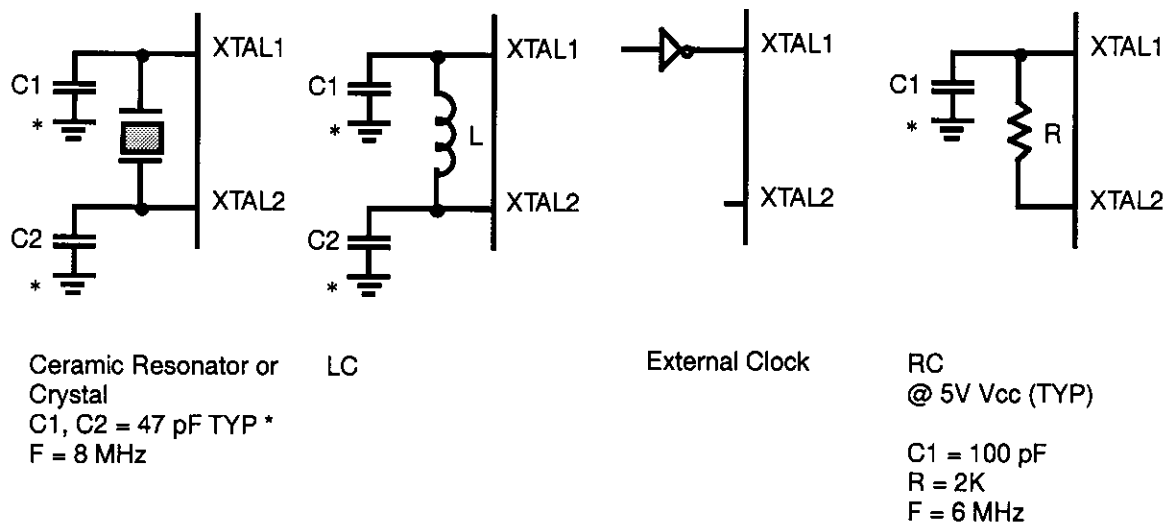
Table 3. Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



* Typical value including pin parasitics

Figure 16. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
 $V_{CC} = 5.0V @ 25^{\circ}C$

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 μ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
 $V_{CC} = 3.3V @ 25^{\circ}C$

Resistor (R)	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1 μ Fd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μ A. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT} ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR} , plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV} .

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

FUNCTIONAL DESCRIPTION (Continued)

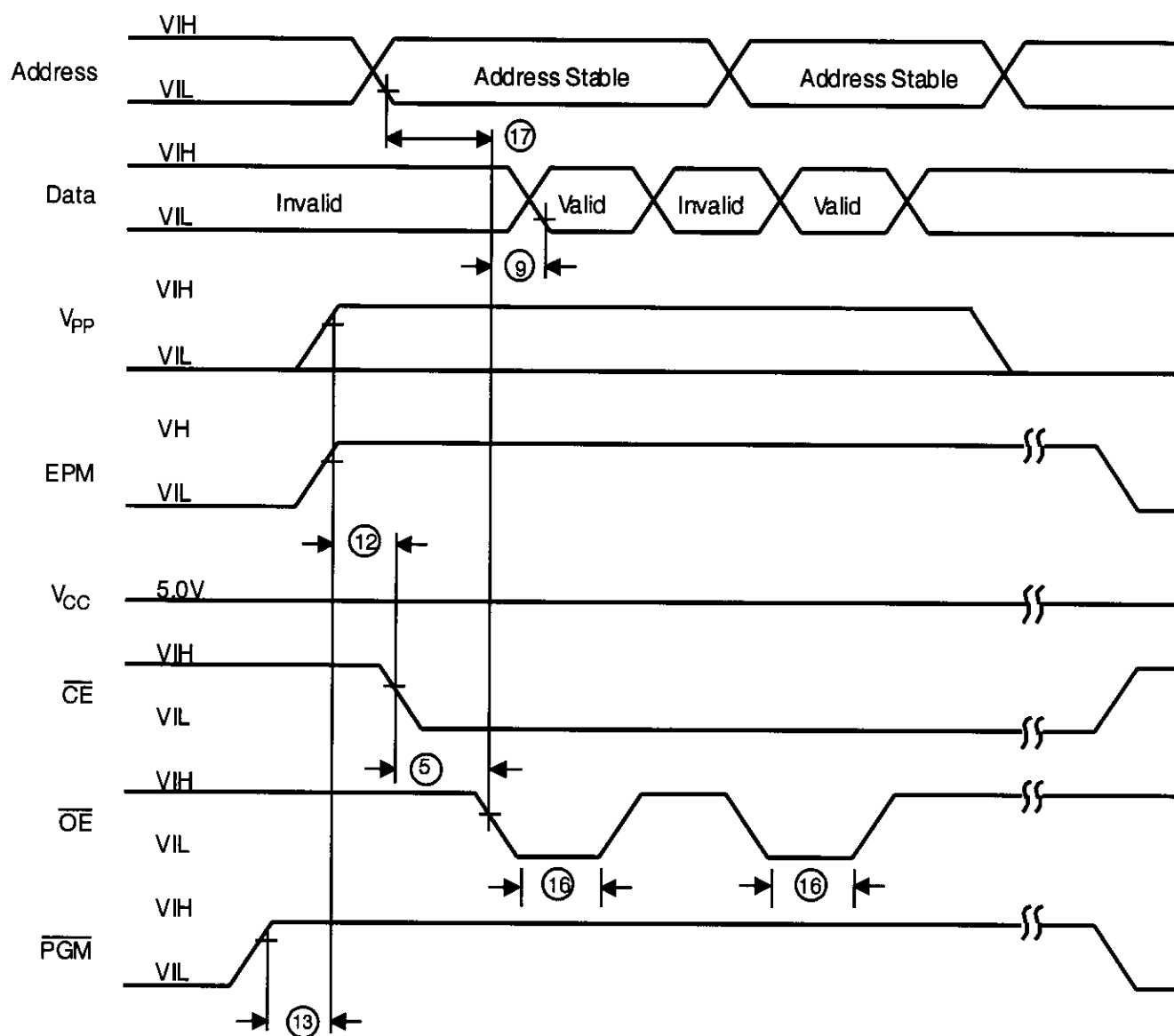


Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)

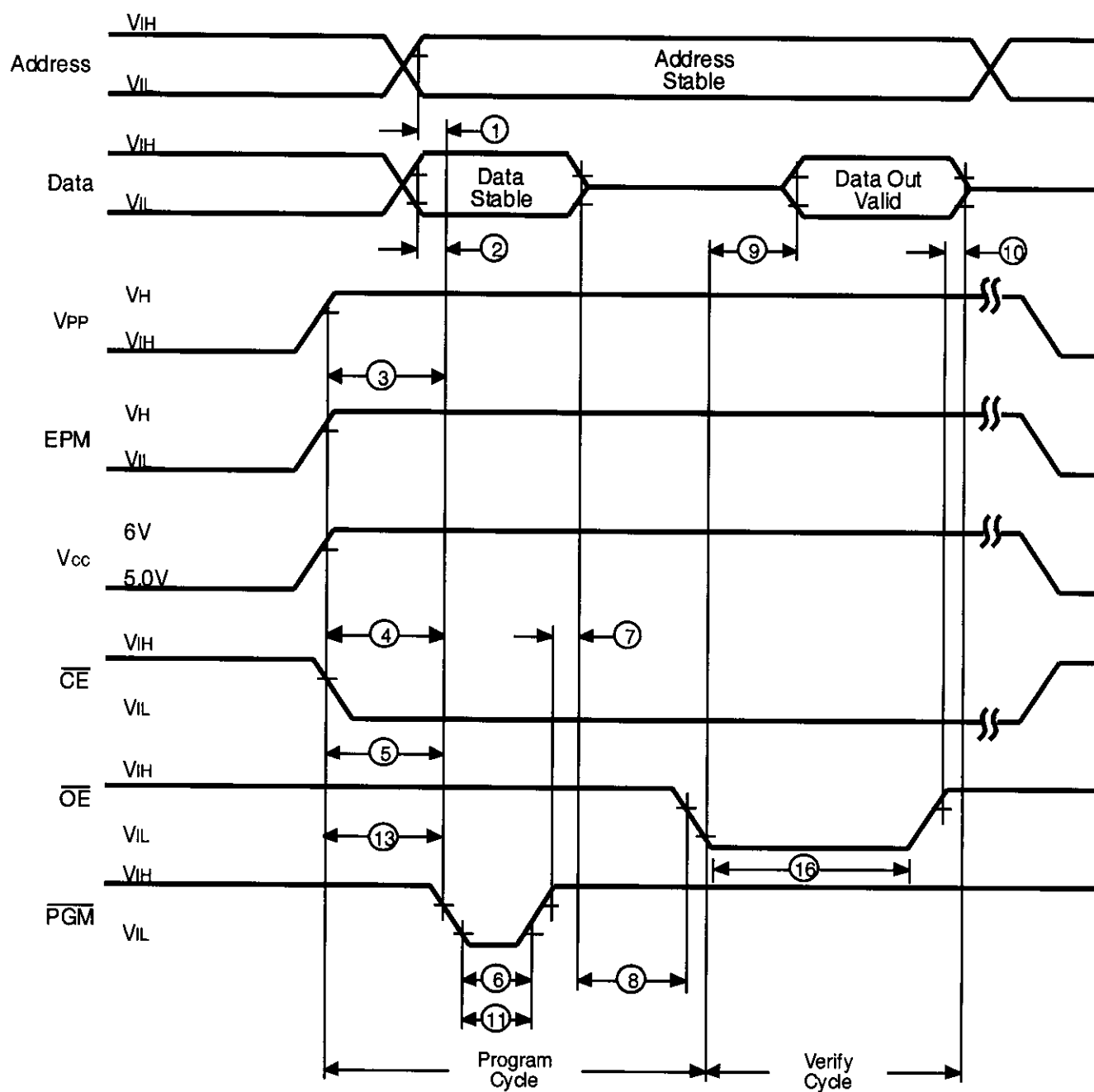


Figure 20. Z86E04/E08 Programming Waveform
(Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

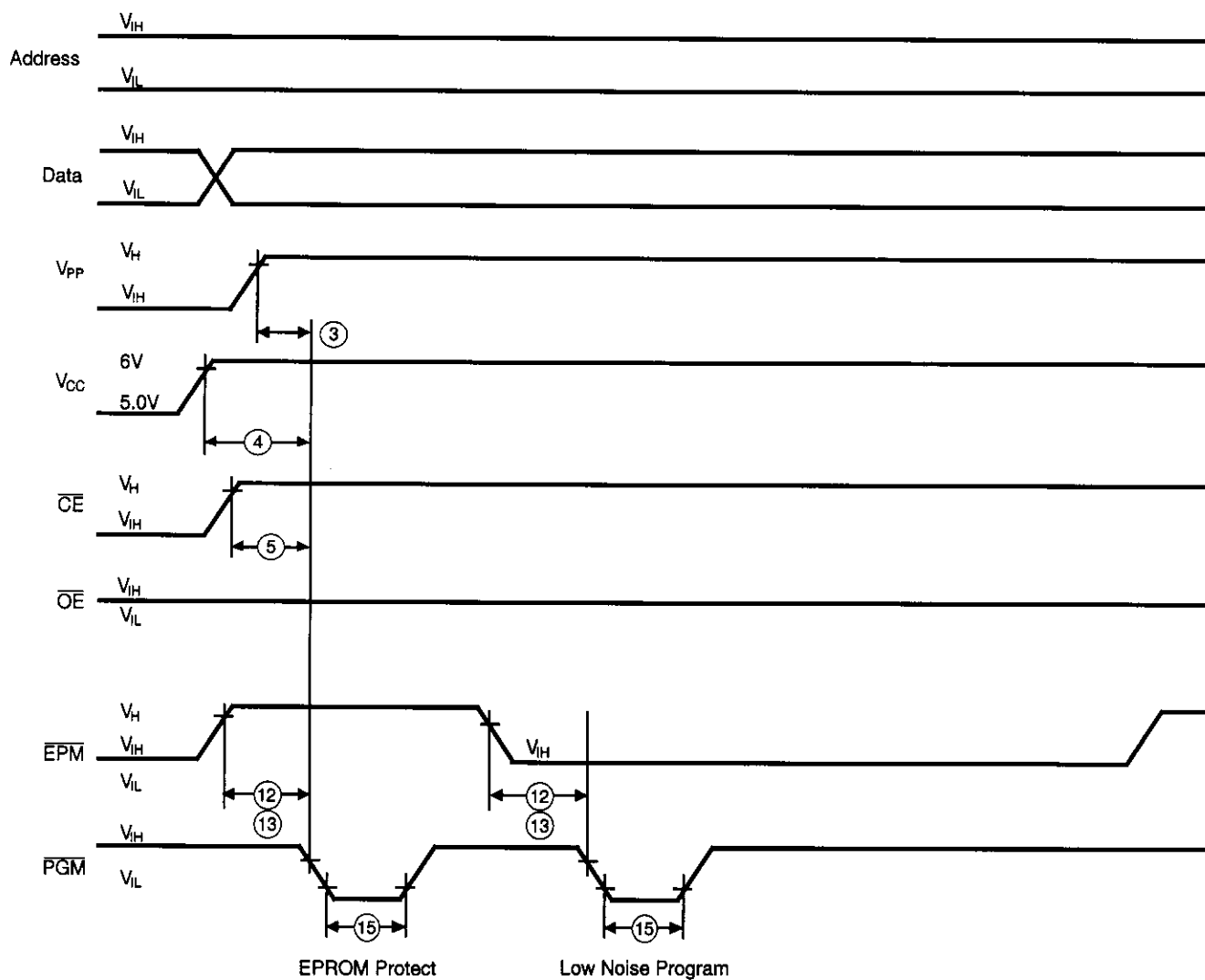
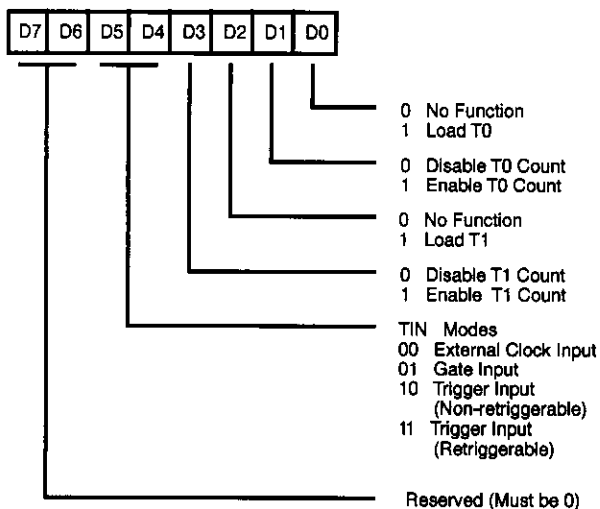


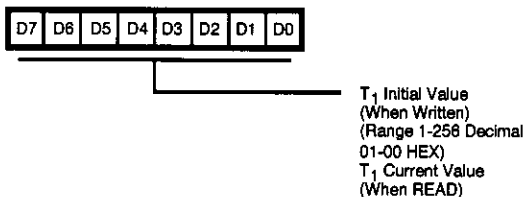
Figure 21. Z86E04/E08 Programming Options Waveform
(EPROM Protect and Low Noise Program)

Z8 CONTROL REGISTERS

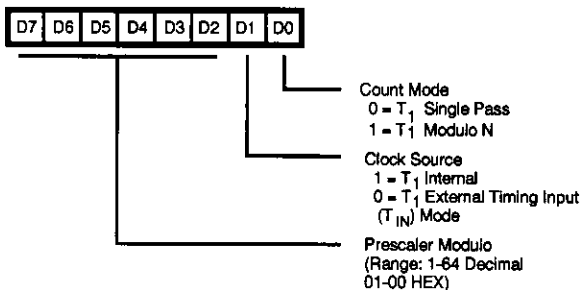
R241 TMR

Figure 24. Timer Mode Register (F1_H: Read/Write)

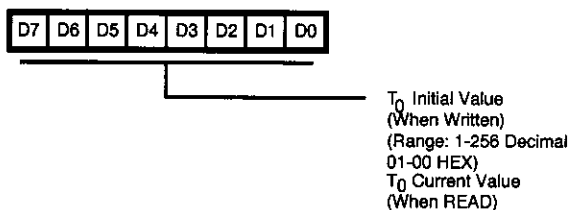
R242 T1

Figure 25. Counter Timer 1 Register (F2_H: Read/Write)

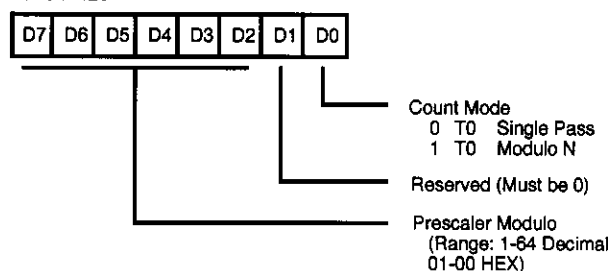
R243 PRE1

Figure 26. Prescaler 1 Register (F3_H: Write Only)

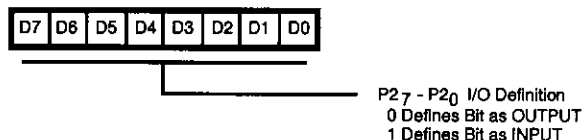
R244 T0

Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

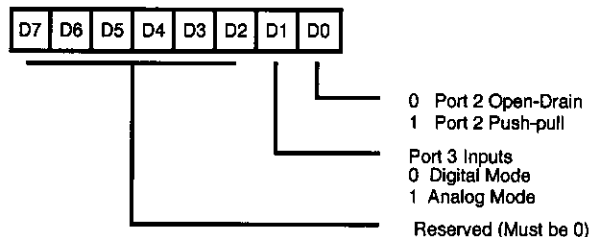
R245 PRE0

Figure 28. Prescaler 0 Register (F5_H: Write Only)

R246 P2M

Figure 29. Port 2 Mode Register (F6_H: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7_H: Write Only)

Z8 CONTROL REGISTERS (Continued)

R248 P01M

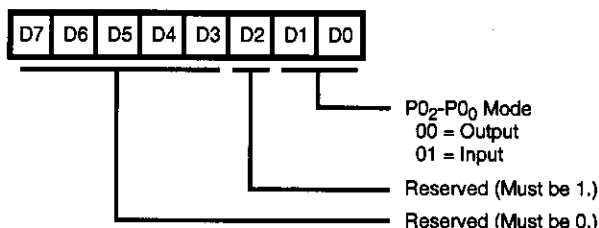


Figure 31. Port 0 and 1 Mode Register
(F8_H: Write Only)

R249 IPR

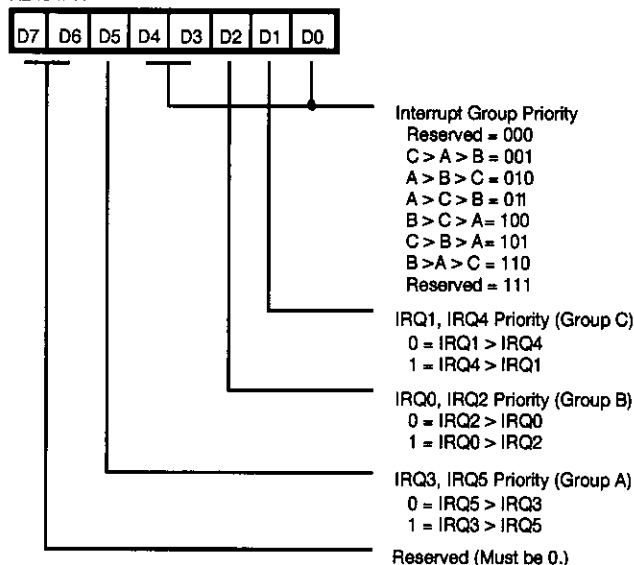


Figure 32. Interrupt Priority Register
(F9_H: Write Only)

R250 IRQ

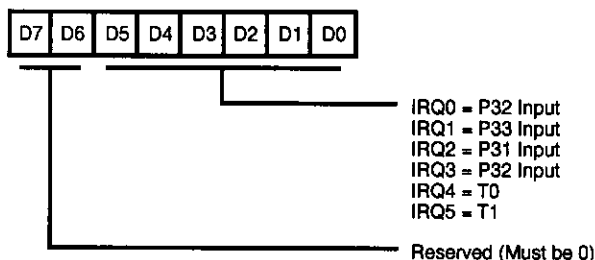


Figure 33. Interrupt Request Register
(FA_H: Read/Write)

R251 IMR

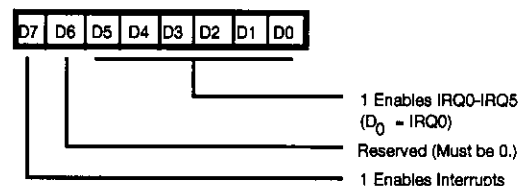


Figure 34. Interrupt Mask Register
(FB_H: Read/Write)

R252 Flags

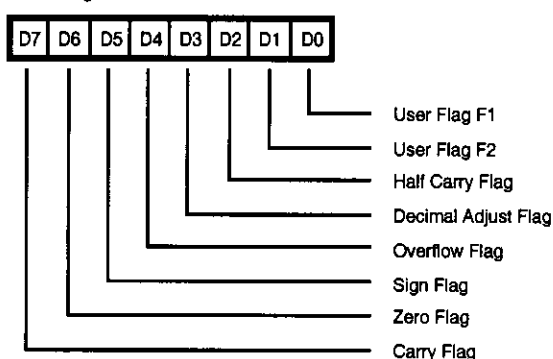


Figure 35. Flag Register
(FC_H: Read/Write)

R253 RP

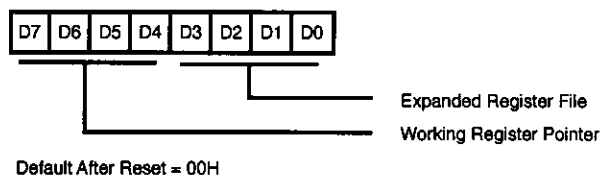


Figure 36. Register Pointer
(FD_H: Read/Write)

R255 SPL

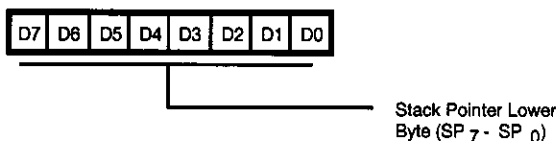
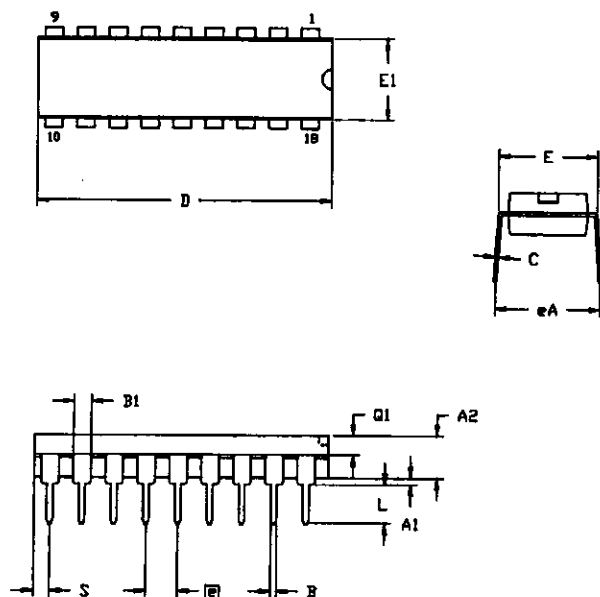


Figure 37. Stack Pointer
(FF_H: Read/Write)

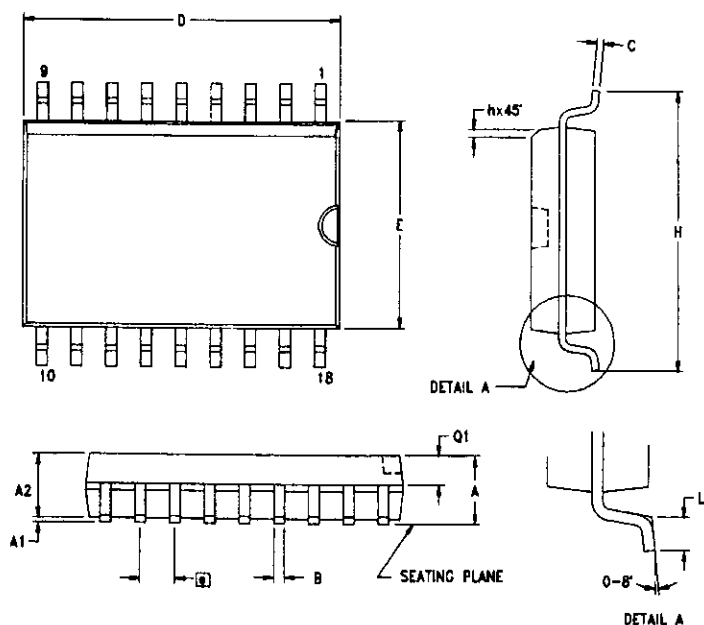
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram