# Zilog - Z86E0812HSC1903TR Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 125 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86e0812hsc1903tr |

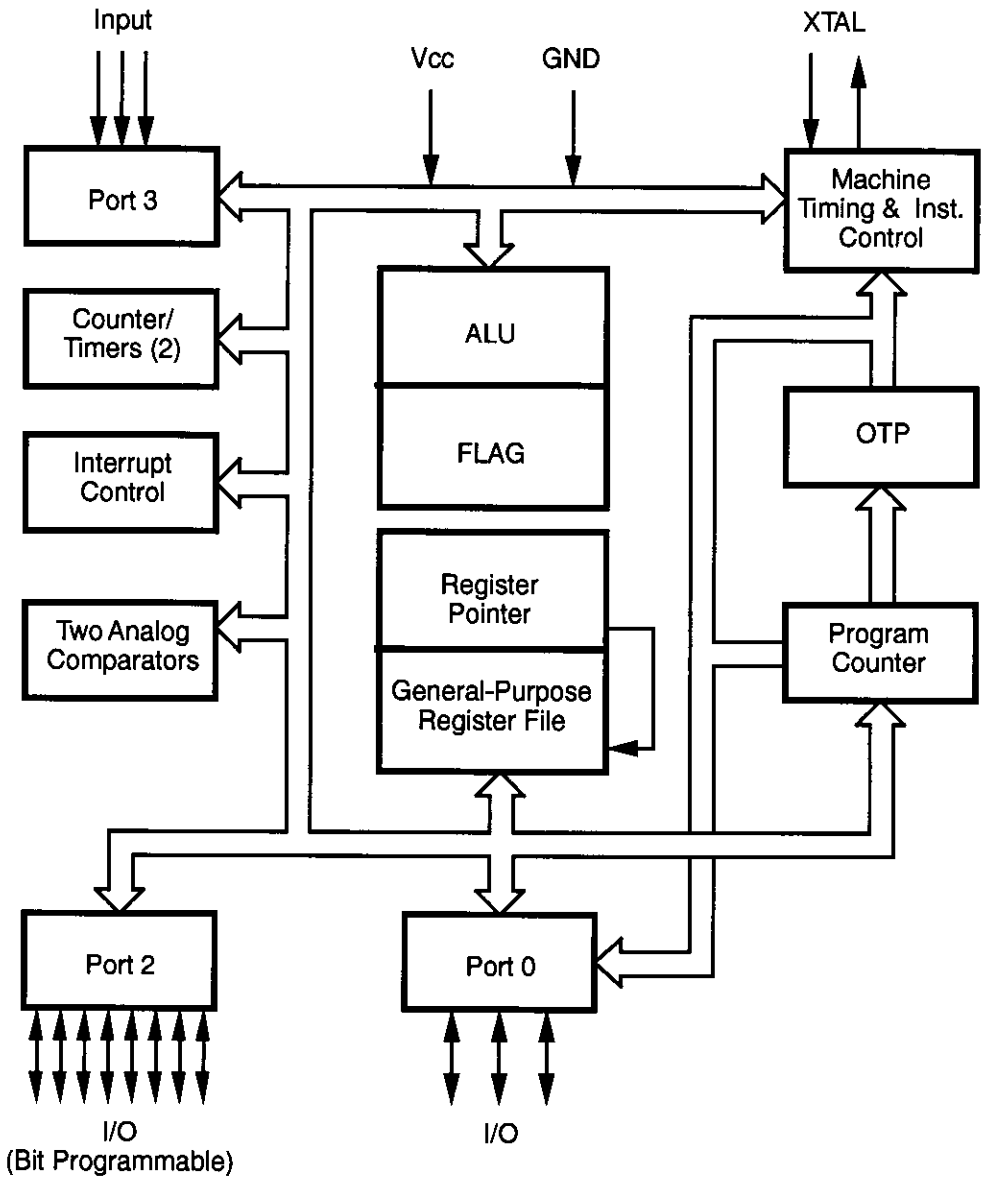



**Figure 1. Functional Block Diagram**

## GENERAL DESCRIPTION (Continued)

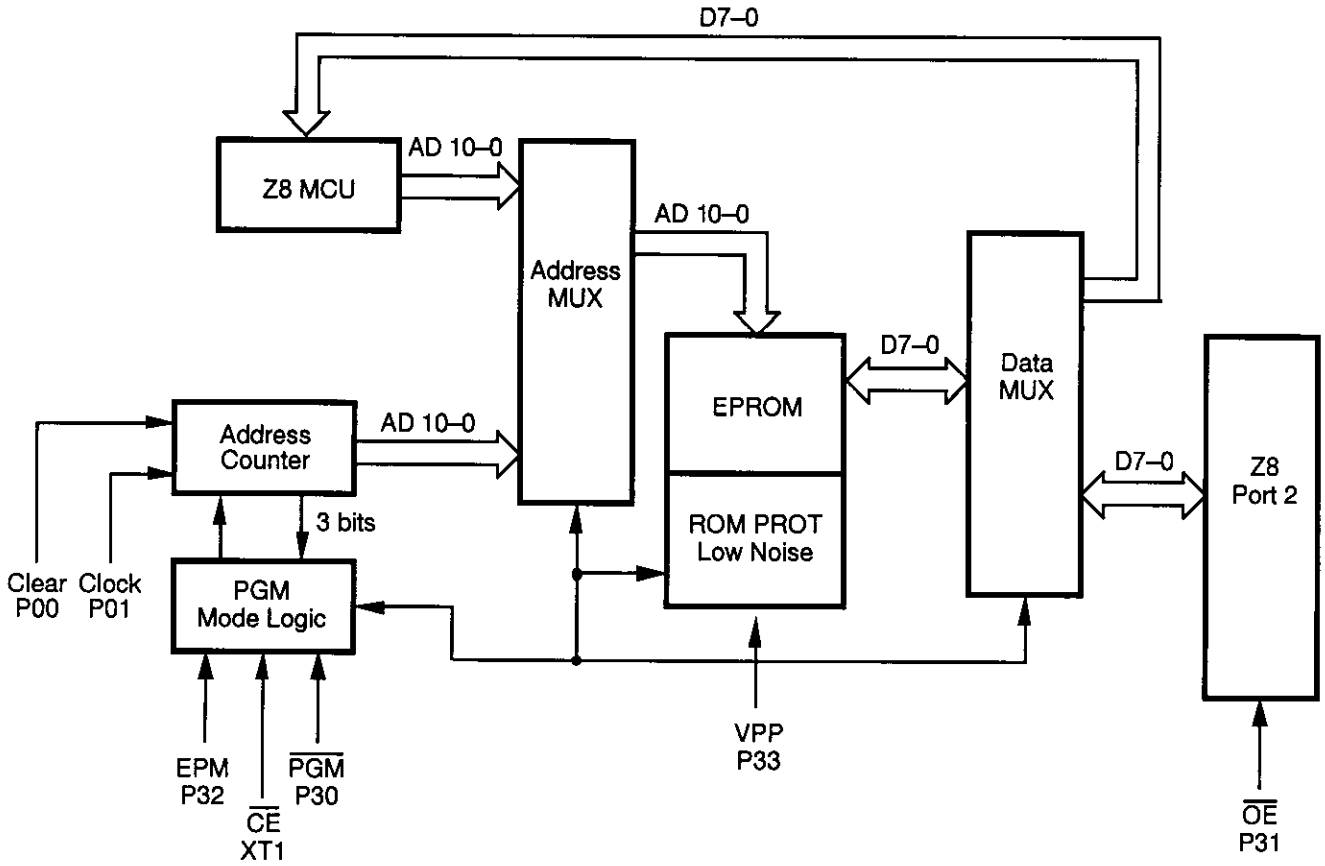



**Figure 2. EPROM Programming Mode Block Diagram**

## PIN DESCRIPTION

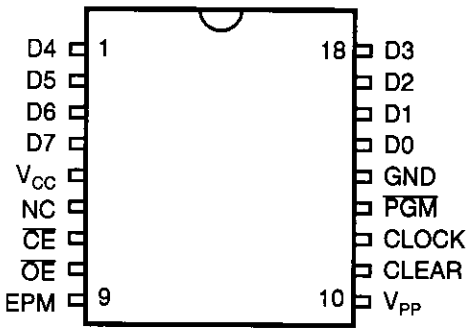



**Figure 3. 18-Pin EPROM Mode Configuration**

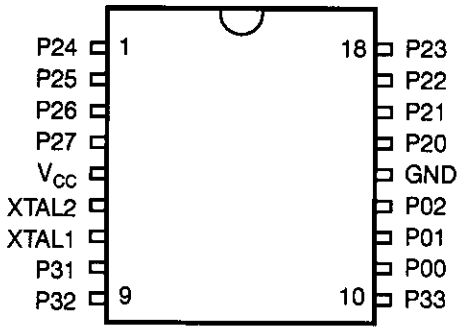



**Figure 4. 18-Pin DIP/SOIC Mode Configuration**

**Table 1. 18-Pin DIP Pin Identification**

| EPROM Programming Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | D4–D7 | Data 4, 5, 6, 7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | NC | No Connection | |
| 7 | $\overline{CE}$ | Chip Enable | Input |
| 8 | $\overline{OE}$ | Output Enable | Input |
| 9 | EPM | EPROM Prog Mode | Input |
| 10 | $V_{PP}$ | Prog Voltage | Input |
| 11 | Clear | Clear Clock | Input |
| 12 | Clock | Address | Input |
| 13 | $\overline{PGM}$ | Prog Mode | Input |
| 14 | GND | Ground | |
| 15–18 | D0–D3 | Data 0,1, 2, 3 | In/Output |

**Table 2. 18-Pin DIP/SOIC Pin Identification**

| Standard Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | P24–P27 | Port 2, Pins 4,5,6,7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Osc. Clock | Output |
| 7 | XTAL1 | Crystal Osc. Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11–13 | P00–P02 | Port 0, Pins 0,1,2 | In/Output |
| 14 | GND | Ground | |
| 15–18 | P20–P23 | Port 2, Pins 0,1,2,3 | In/Output |

## DC ELECTRICAL CHARACTERISTICS

Standard Temperature

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{INMAX}$ | Max Input Voltage | 4.5V | | 12 | | V | $I_{In}$<250 µA | 1 |
| | | 5.5V | | 12 | | V | $I_{In}$<250 µA | 1 |
| $V_{CH}$ | Clock Input High Voltage | 4.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 4.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 4.5V | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| $V_{OL1}$ | Output Low Voltage | 4.5V | | 0.8 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 4.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| $V_{OL2}$ | Output Low Voltage | 4.5V | | 0.8 | 0.8 | V | $I_{OL}$ = +12 mA, | 5 |
| | | 5.5V | | 0.8 | 0.8 | V | $I_{OL}$ = +12 mA, | 5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 4.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | 2.2 | 3.0 | 2.8 | V | @ 6 MHz Max. Int. CLK Freq. | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 4.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 4.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$–1.0 | | V | | |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 4.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 4.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 5.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| $I_{CC2}$ | Standby Current | 4.5V | | 10.0 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| | | 5.5V | | 10.0 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V,$V_{CC}$ WDT is not Running | 7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | | 32.0 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | 32.0 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | | –16.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | –16.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |

**Notes:**

1. Port 2 and Port 0 only
2. $V_{SS}$ = 0V = GND
3. The device operates down to $V_{LV}$ of the specified frequency for $V_{LV}$. The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{LV}$ at the ambient temperature. The $V_{LV}$ increases as the temperature decreases.
4. $V_{CC}$ = 4.5 to 5.5V, typical values measured at $V_{CC}$ = 5.0V.
   The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at $V_{CC}$ = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at $V_{CC}$ or $V_{SS}$ level.
8. If analog comparator is selected, then the comparator inputs must be at $V_{CC}$ level.

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = –40°C to +105°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 4.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 4.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 5.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| $I_{CC2}$ | Standby Current | 4.5V | | 20 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| | | 5.5V | | 20 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | | –20.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | –20.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |

**Notes:**

1. Port 2 and Port 0 only
2. $V_{SS}$ = 0V = GND
3. The device operates down to $V_{LV}$ of the specified frequency for $V_{LV}$. The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{LV}$ at the ambient temperature. The $V_{LV}$ increases as the temperature decreases.
4. $V_{CC}$ = 4.5V to 5.5V, typical values measured at $V_{CC}$ = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at $V_{CC}$ or $V_{SS}$ level.
8. If analog comparator is selected, then the comparator inputs must be at $V_{CC}$ level.

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

| 15 | | | | $T_A$= 0 °C to +70 °C | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 8 MHz | | 12 MHz | | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 4.5V | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 62 | | 41 | | ns | 1 |
| | | | 5.5V | 62 | | 41 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 8TpC | 8TpC | | | 1 |
| | | | 5.5V | | 8TpC | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | | 5TpC | 5TpC | | | 1,2 |
| | | | 5.5V | | 5TpC | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 12 | | 12 | | ms | 1 |
| | | | 5.5V | 12 | | 12 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 4.5V | 20 | 80 | 20 | 80 | ms | 1 |
| | | | 5.5V | 20 | 80 | 20 | 80 | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Extended Temperature

| | | | | $T_A$= –40 °C to +105 °C 8 MHz | | 12 MHz | | | |
|---|---|---|---|---|---|---|---|---|---|
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 4.5V | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | | 62 | | 41 | ns | 1 |
| | | | 5.5V | | 62 | | 41 | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | 8TpC | | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 5TpC | | 5TpC | | | 1,2 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 10 | | 10 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 4.5V | 12 | 100 | 12 | 100 | ms | 1 |
| | | | 5.5V | 12 | 100 | 12 | 100 | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

# LOW NOISE VERSION

## Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

# PIN FUNCTIONS

## OTP Programming Mode

**D7–D0** *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

**$V_{CC}$** *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

**$\overline{CE}$** *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

**$\overline{OE}$** *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

**EPM** *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

**$V_{PP}$** *Program Voltage.* This pin supplies the program voltage.

**Clear** *Clear* (active High). This pin resets the internal address counter at the High Level.

**Clock** *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

**$\overline{PGM}$** *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

## Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above $V_{CC}$ occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the $V_{PP}$, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to $V_{CC}$.
- Adding a capacitor to the affected pin.

**Note:** Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

## PIN FUNCTIONS (Continued)

**XTAL1, XTAL2** *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

**Port 0, P02–P00.** Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

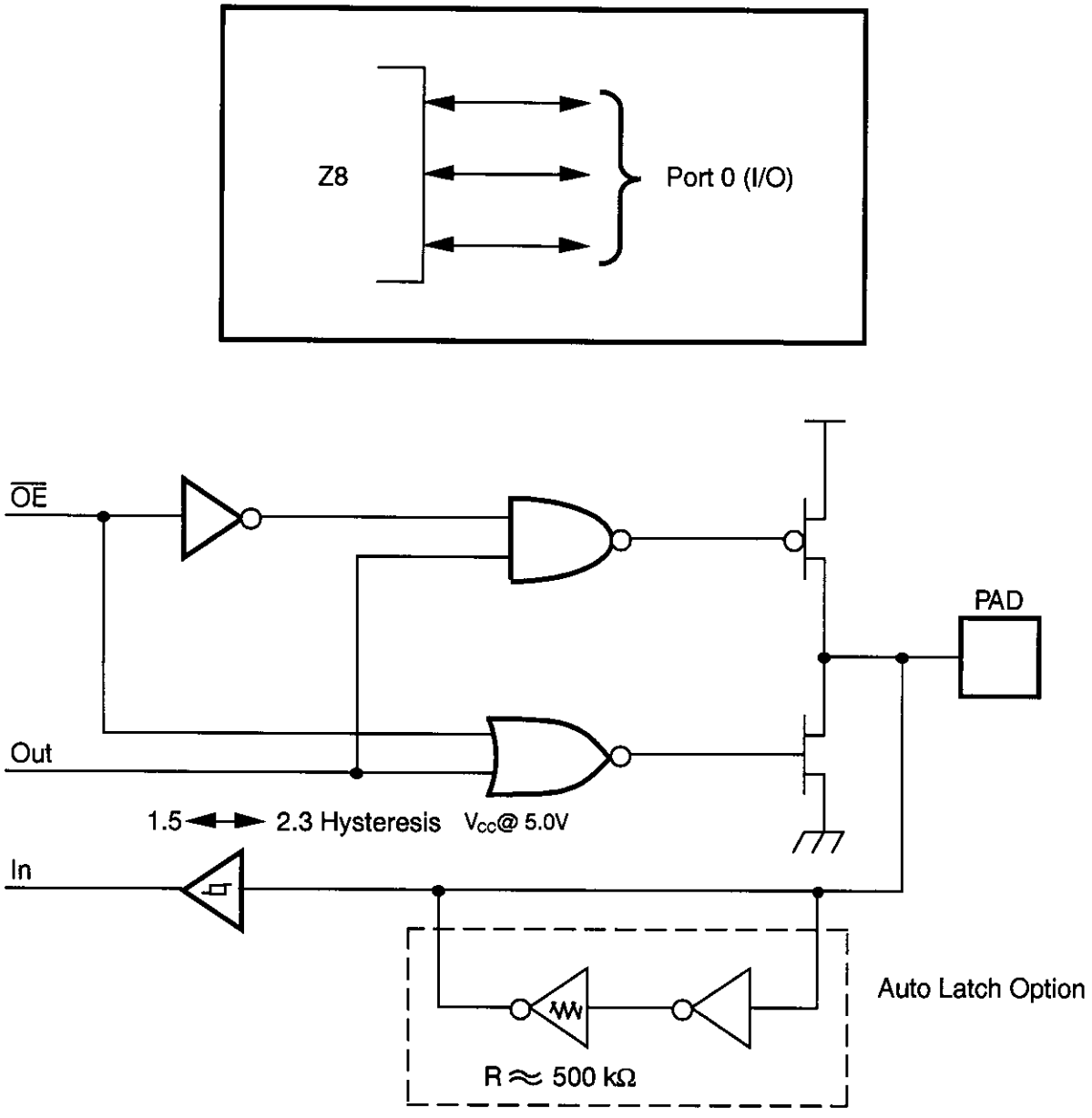
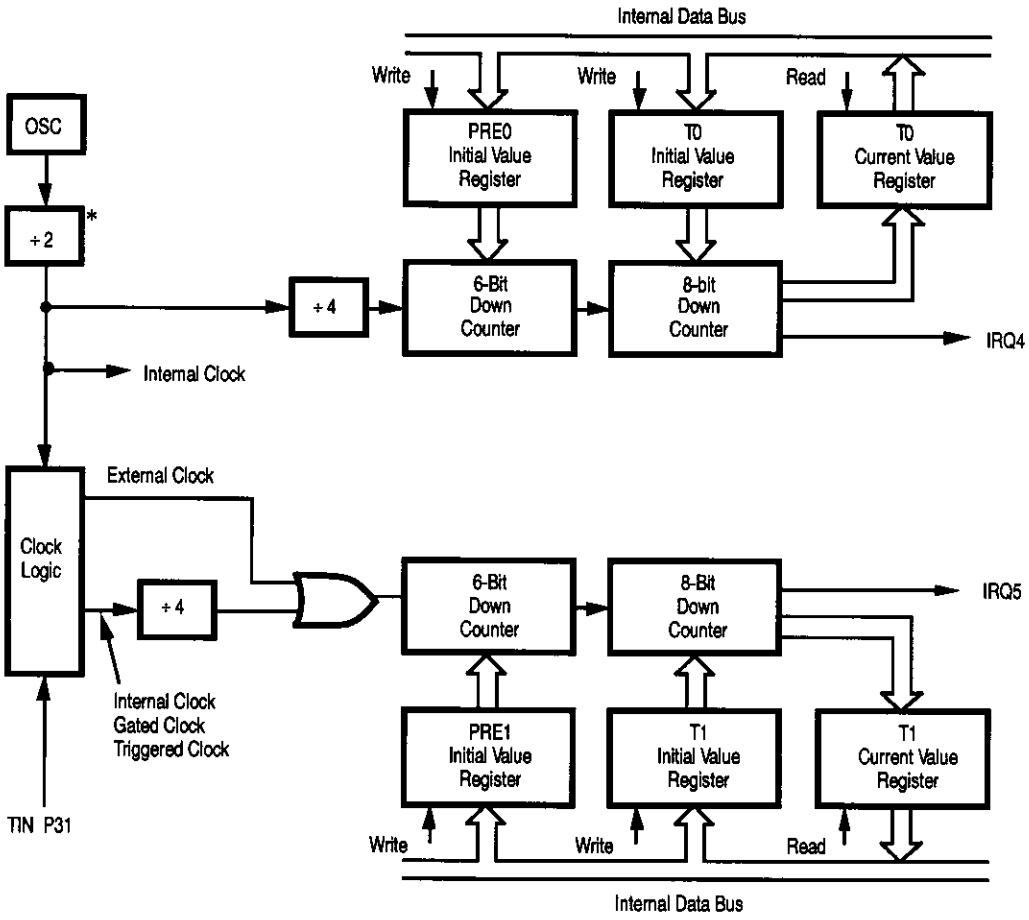



**Figure 7. Port 0 Configuration**




* **Note**: By passed, if Low EMI Mode is selected.

**Figure 14. Counter/Timers Block Diagram**

## Low EMI Emission

The Z8 can be programmed to operate in a low EMI Emission (Low Noise) Mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT Mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

In addition to $V_{DD}$ and GND ($V_{SS}$), the Z8 changes all its pin functions in the EPROM Mode. XTAL2 has no function, XTAL1 functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as $V_{PP}$, and P02 functions as $\overline{PGM}$.

**ROM Protect.** ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI **are supported** (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will not automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and $\overline{CE}$ pins be clamped to $V_{CC}$ through a diode to $V_{CC}$ to prevent accidentally entering the OTP Mode. The $V_{PP}$ requires both a diode and a 100 pF capacitor.

**Auto Latch Disable.** Auto Latch Disable option bit when programmed will globally disable all Auto Latches.

**WDT Enable.** The WDT Enable option bit, when programmed, will have the hardware enabled Permanent WDT enabled after exiting reset and can not be stopped in Halt or Stop Mode.

**EPROM/Test Mode Disable.** The EPROM/Test Mode Disable option bit, when programmed, will disable the EPROM Mode and the Factory Test Mode. Reading, verifying, and programming the Z8 will be disabled. To fully verify that this mode is disabled, the device must be power cycled.

**User Modes.** Table 7 shows the programming voltage of each mode.

**Table 7. OTP Programming Table**

| Programming Modes | $V_{PP}$ | EPM | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | ADDR | DATA | $V_{CC}$* |
|---|---|---|---|---|---|---|---|---|
| EPROM READ | NU | $V_H$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADDR | Out | 5.0V |
| PROGRAM | $V_H$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | ADDR | In | 6.4V |
| PROGRAM VERIFY | $V_H$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADDR | Out | 6.4V |
| EPROM PROTECT | $V_H$ | $V_H$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.4V |
| LOW NOISE SELECT | $V_H$ | $V_{IH}$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.4V |
| AUTO LATCH DISABLE | $V_H$ | $V_{IH}$ | $V_H$ | $V_{IL}$ | $V_{IL}$ | NU | NU | 6.4V |
| WDT ENABLE | $V_H$ | $V_{IL}$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.4V |
| EPROM/TEST MODE | $V_H$ | $V_{IL}$ | $V_H$ | $V_{IL}$ | $V_{IL}$ | NU | NU | 6.4V |

**Notes:**

1. $V_H$ =12.75V ± 0.25 $V_{DC}$ .
2. $V_{IH}$ = As per specific Z8 DC specification.
3. $V_{IL}$ = As per specific Z8 DC specification.
4. X = Not used, but must be set to $V_H$ or $V_{IH}$ level.
5. NU = Not used, but must be set to either $V_{IH}$ or $V_{IL}$ level.
6. $I_{PP}$ during programming = 40 mA maximum.
7. $I_{CC}$ during programming, verify, or read = 40 mA maximum.
8. * $V_{CC}$ has a tolerance of ±0.25V.

## FUNCTIONAL DESCRIPTION (Continued)

**Internal Address Counter.** The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

**Programming Waveform.** Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 23 shows the flow chart of the Z8 programming algorithm.

**Table 8. Timing of Programming Waveforms**

| Parameters | Name | Min | Max | Units |
|---|---|---|---|---|
| 1 | Address Setup Time | 2 | | µs |
| 2 | Data Setup Time | 2 | | µs |
| 3 | $V_{PP}$ Setup | 2 | | µs |
| 4 | $V_{CC}$ Setup Time | 2 | | µs |
| 5 | Chip Enable Setup Time | 2 | | µs |
| 6 | Program Pulse Width | 0.95 | | ms |
| 7 | Data Hold Time | 2 | | µs |
| 8 | $\overline{OE}$ Setup Time | 2 | | µs |
| 9 | Data Access Time | 188 | | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | µs |
| 13 | $\overline{PGM}$ Setup Time | 2 | | µs |
| 14 | Address to $\overline{OE}$ Setup Time | 2 | | µs |
| 15 | Option Program Pulse Width | 78 | | ms |
| 16 | $\overline{OE}$ Width | 250 | | ns |
| 17 | Address Valid to $\overline{OE}$ Low | 125 | | ns |

## FUNCTIONAL DESCRIPTION (Continued)

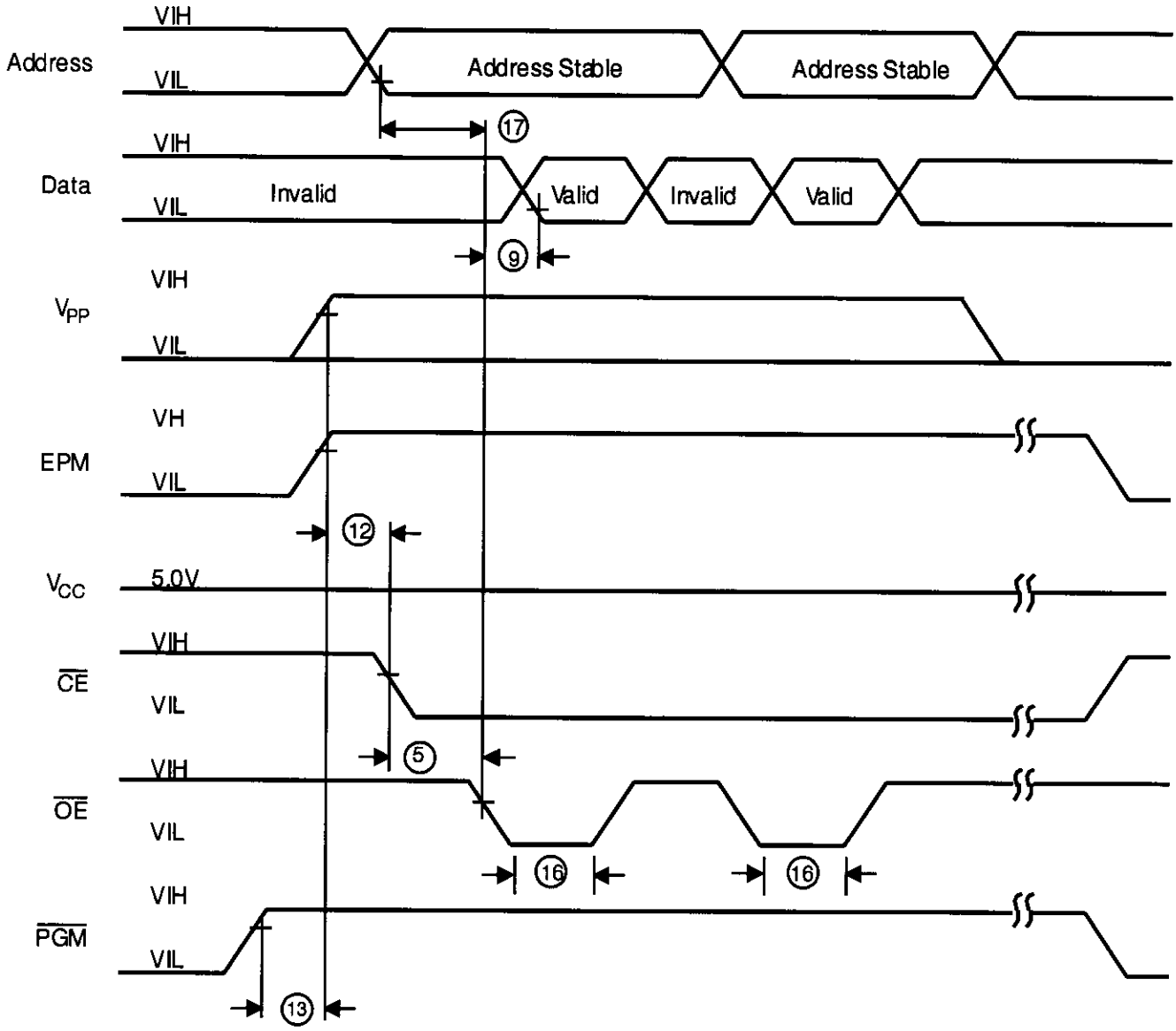



**Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)**

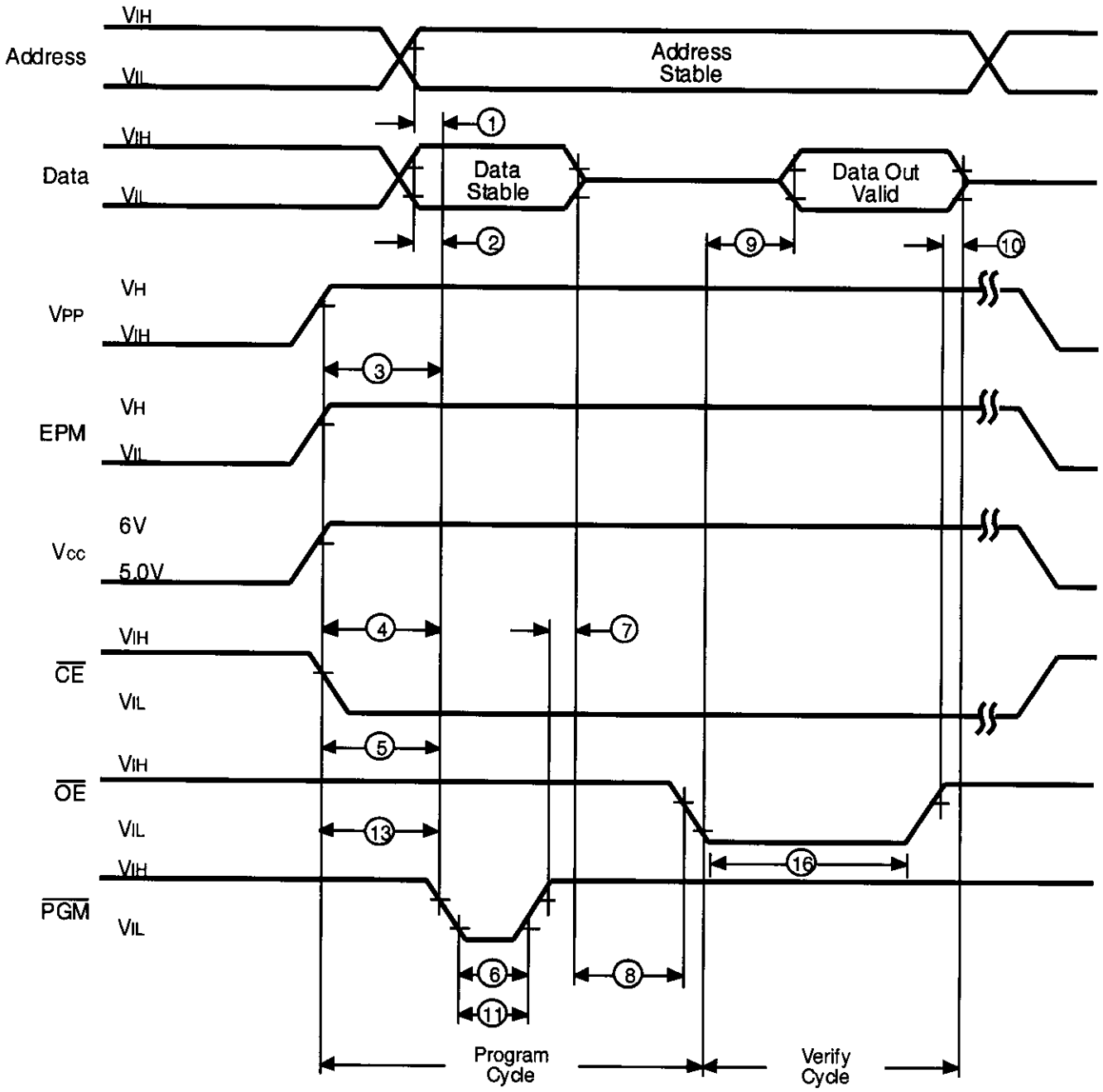



**Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)**

## FUNCTIONAL DESCRIPTION (Continued)

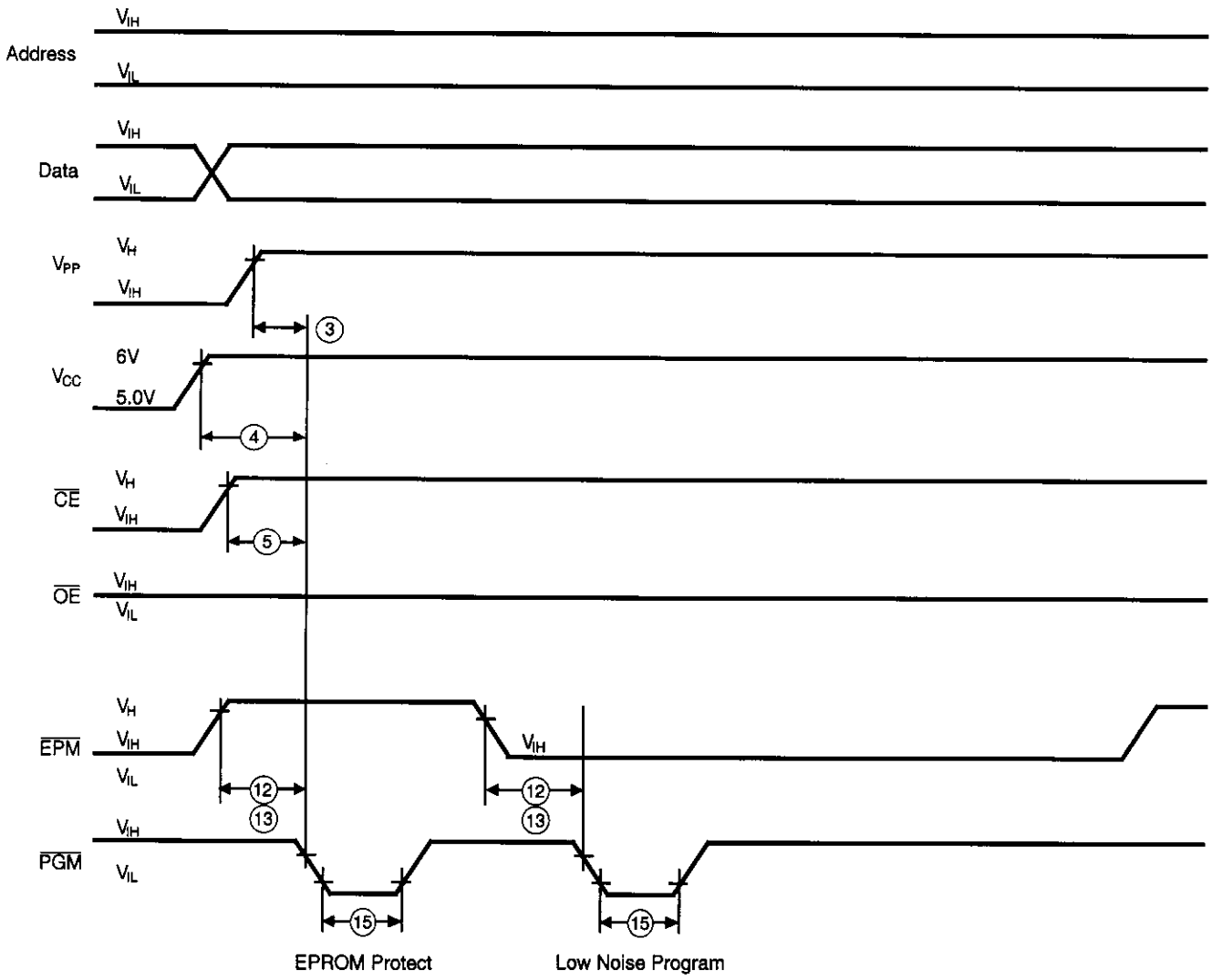



**Figure 21. Z86E04/E08 Programming Options Waveform (EPROM Protect and Low Noise Program)**

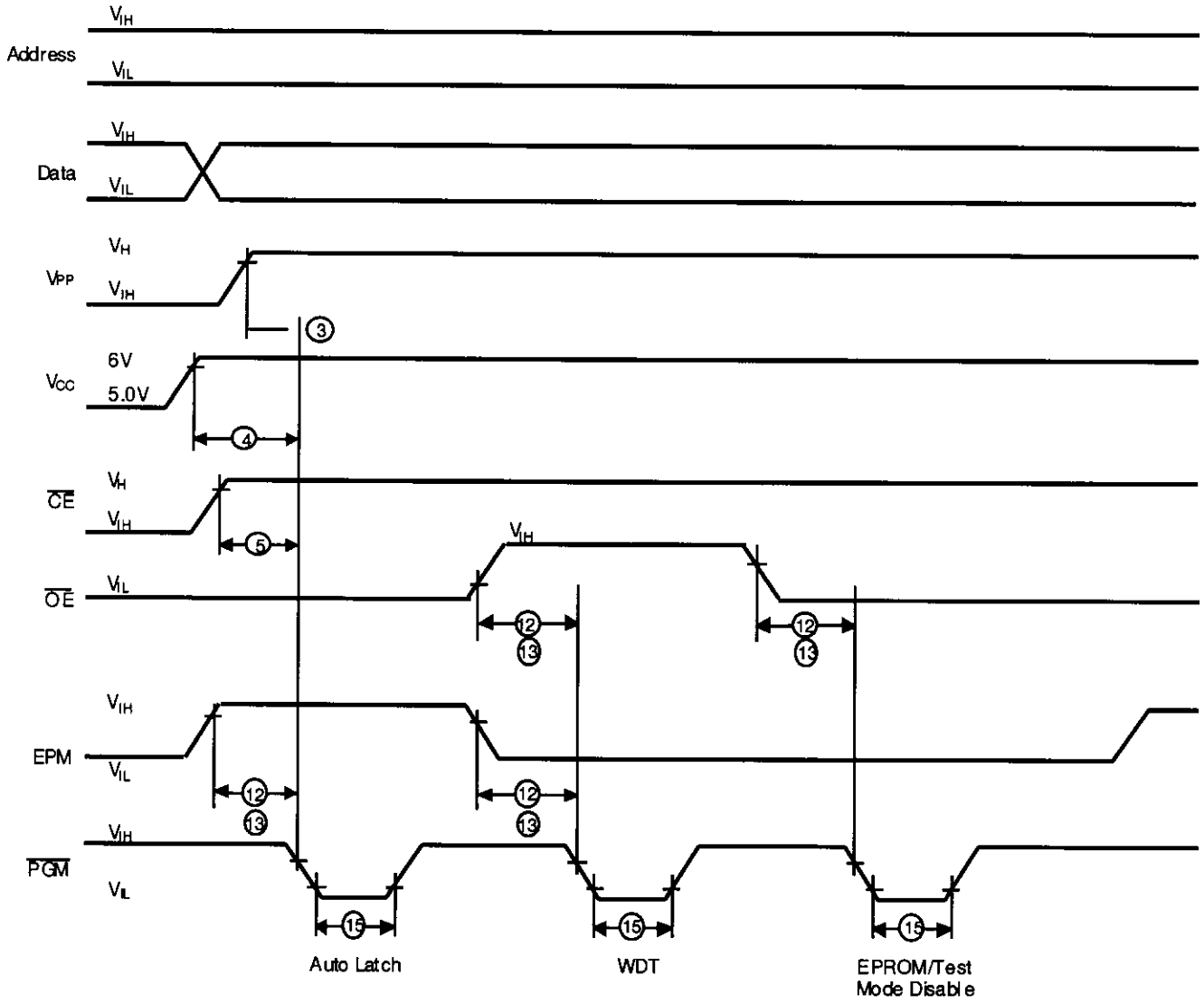



**Figure 22. Z86E04/E08 Programming Options Waveform (Auto Latch Disable, Permanent WDT Enable and EPROM/Test Mode Disable)**

## Z8 CONTROL REGISTERS (Continued)

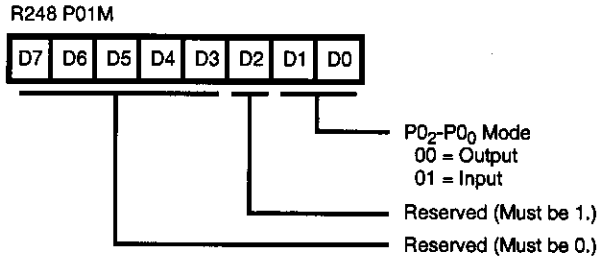



**Figure 31. Port 0 and 1 Mode Register ($F8_H$: Write Only)**

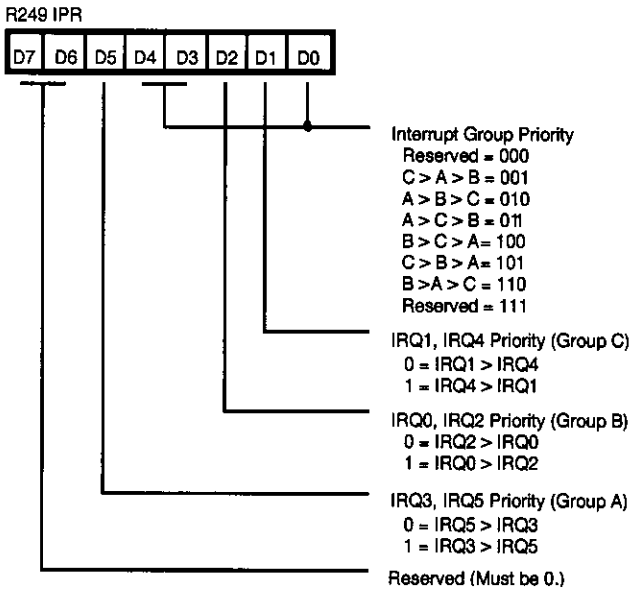



**Figure 32. Interrupt Priority Register ($F9_H$: Write Only)**

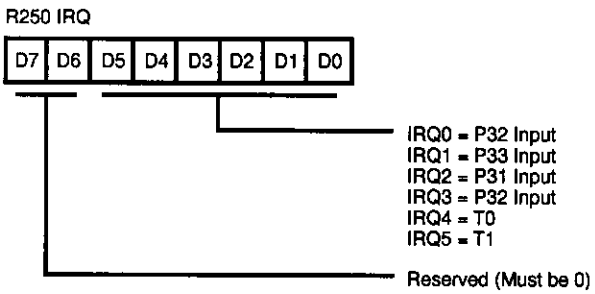



**Figure 33. Interrupt Request Register ($FA_H$: Read/Write)**

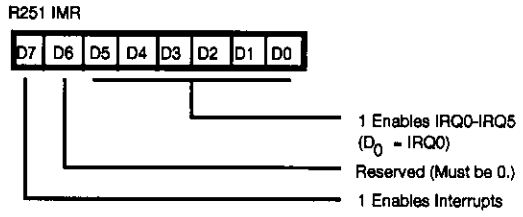



**Figure 34. Interrupt Mask Register ($FB_H$: Read/Write)**

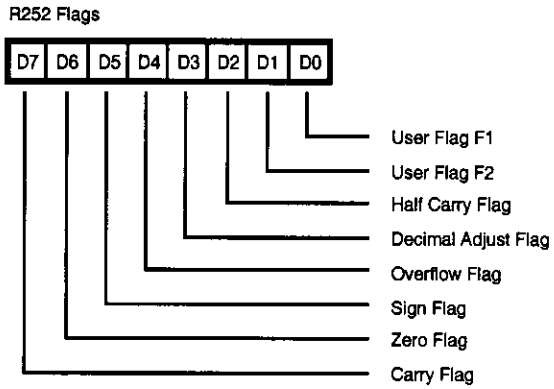



**Figure 35. Flag Register ($FC_H$: Read/Write)**

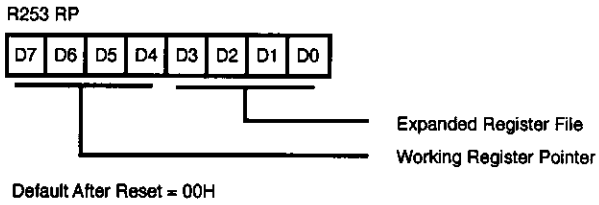



**Figure 36. Register Pointer ($FD_H$: Read/Write)**

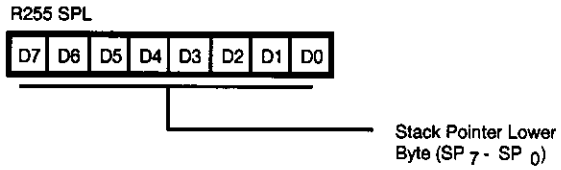



**Figure 37. Stack Pointer ($FF_H$: Read/Write)**

## ORDERING INFORMATION

| Z86E04 | | Z86E08 | |
|---|---|---|---|
| Standard Temperature | | Standard Temperature | |
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86E0412PSC | Z86E0412SSC | Z86E0812PSC | Z86E0812SSC |
| Z86E0412PEC | Z86E0412SEC | Z86E0812PEC | Z86E0812SEC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

### Codes

**Preferred Package**
P = Plastic DIP

**Longer Lead Time**
S = SOIC

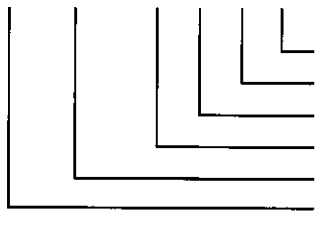
**Preferred Temperature**
S = 0°C to +70°C
E = –40°C to +105°C

**Speeds**
12 =12 MHz

**Environmental**
C = Plastic Standard

### Example:

**Z 86E04 12 P S C** is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.



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