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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 125 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86e0812hsg1903 |

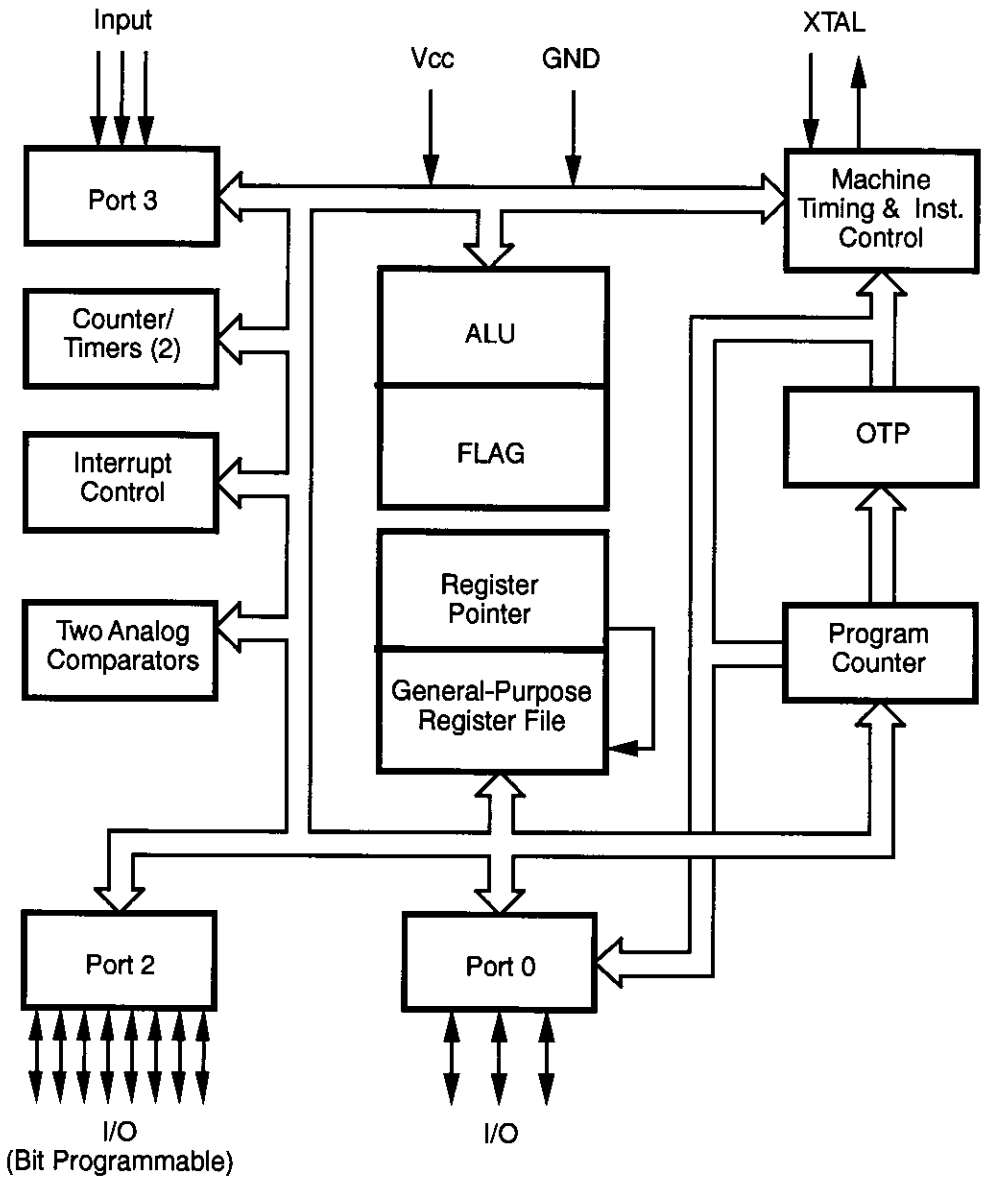



**Figure 1. Functional Block Diagram**

## GENERAL DESCRIPTION (Continued)

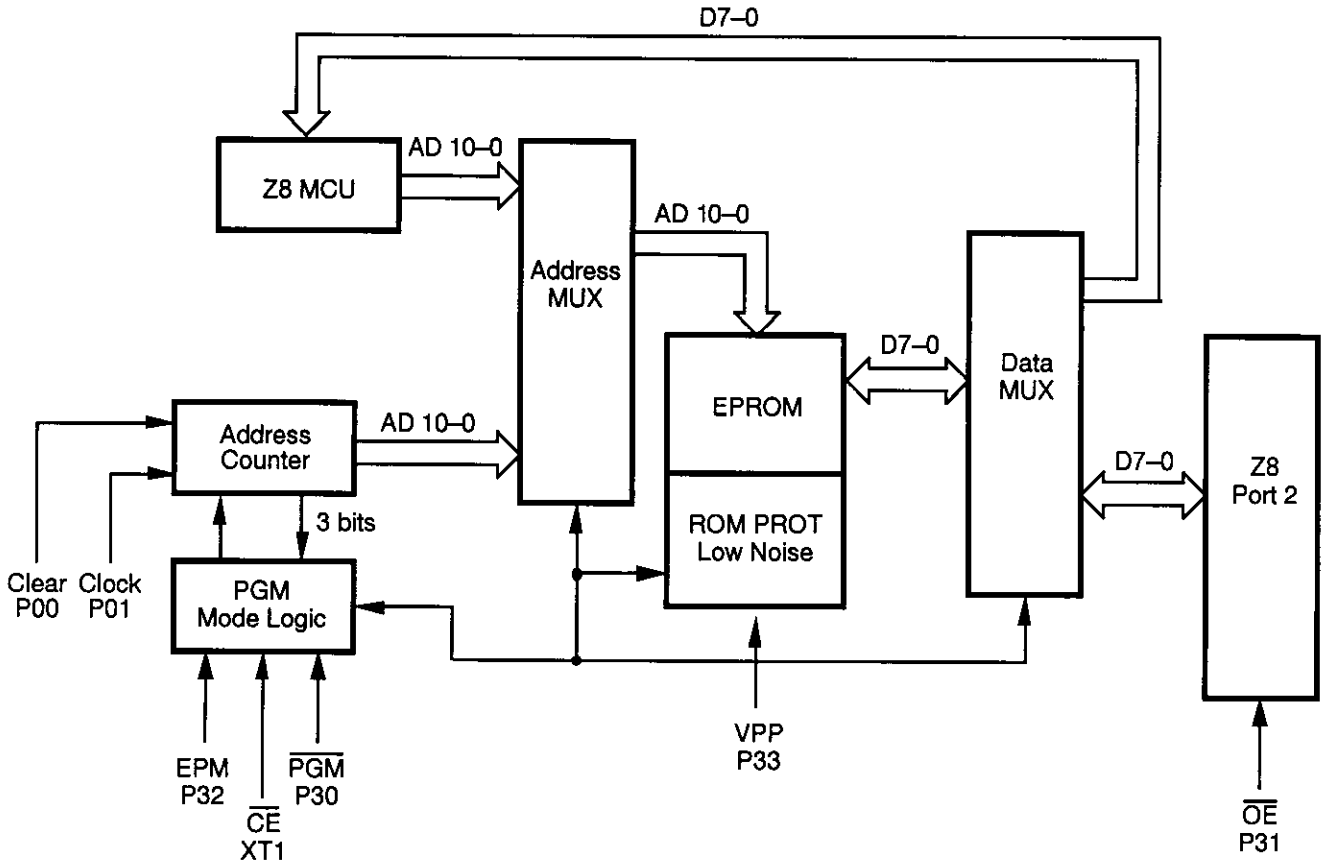



**Figure 2. EPROM Programming Mode Block Diagram**

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

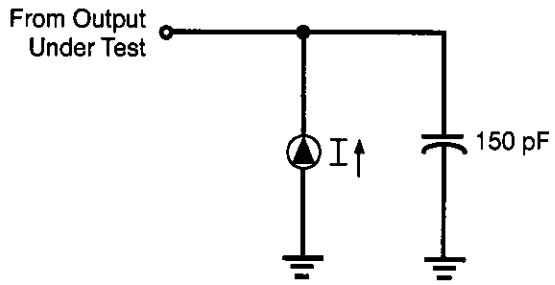



**Figure 5. Test Load Diagram**

## CAPACITANCE

$T_A$ = 25°C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 10 pF |
| Output capacitance | 0 | 20 pF |
| I/O capacitance | 0 | 25 pF |

## DC ELECTRICAL CHARACTERISTICS

Standard Temperature

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{INMAX}$ | Max Input Voltage | 4.5V | | 12 | | V | $I_{In}$<250 µA | 1 |
| | | 5.5V | | 12 | | V | $I_{In}$<250 µA | 1 |
| $V_{CH}$ | Clock Input High Voltage | 4.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 4.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 4.5V | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| $V_{OL1}$ | Output Low Voltage | 4.5V | | 0.8 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 4.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| $V_{OL2}$ | Output Low Voltage | 4.5V | | 0.8 | 0.8 | V | $I_{OL}$ = +12 mA, | 5 |
| | | 5.5V | | 0.8 | 0.8 | V | $I_{OL}$ = +12 mA, | 5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 4.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | 2.2 | 3.0 | 2.8 | V | @ 6 MHz Max. Int. CLK Freq. | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 4.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 4.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | | 0 | $V_{CC}$–1.0 | | V | | |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 4.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 4.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 5.5V | | 4.5 | 2.8 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 4 MHz | 7 |
| $I_{CC2}$ | Standby Current | 4.5V | | 10.0 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| | | 5.5V | | 10.0 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V,$V_{CC}$ WDT is not Running | 7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 4.5V | | 32.0 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | 32.0 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | | –16.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.5V | | –16.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | |

**Notes:**

1. Port 2 and Port 0 only
2. $V_{SS}$ = 0V = GND
3. The device operates down to $V_{LV}$ of the specified frequency for $V_{LV}$. The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{LV}$ at the ambient temperature. The $V_{LV}$ increases as the temperature decreases.
4. $V_{CC}$ = 4.5 to 5.5V, typical values measured at $V_{CC}$ = 5.0V.
   The $V_{CC}$ voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at $V_{CC}$ = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at $V_{CC}$ or $V_{SS}$ level.
8. If analog comparator is selected, then the comparator inputs must be at $V_{CC}$ level.

## AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

| | | | | $T_A$= –40 °C to +105 °C | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 4 MHz | | | |
| No | Symbol | Parameter | $V_{CC}$ | Min | Max | Min | Max | Units | Notes |
| 1 | TPC | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC<br>TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4. | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 4TpC | 4TpC | | | 1 |
| | | | 5.5V | | 4TpC | 4TpC | | | 1 |
| 7 | TrTin,<br>TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 10 | | 10 | | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

**Port 2, P27–P20.** Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

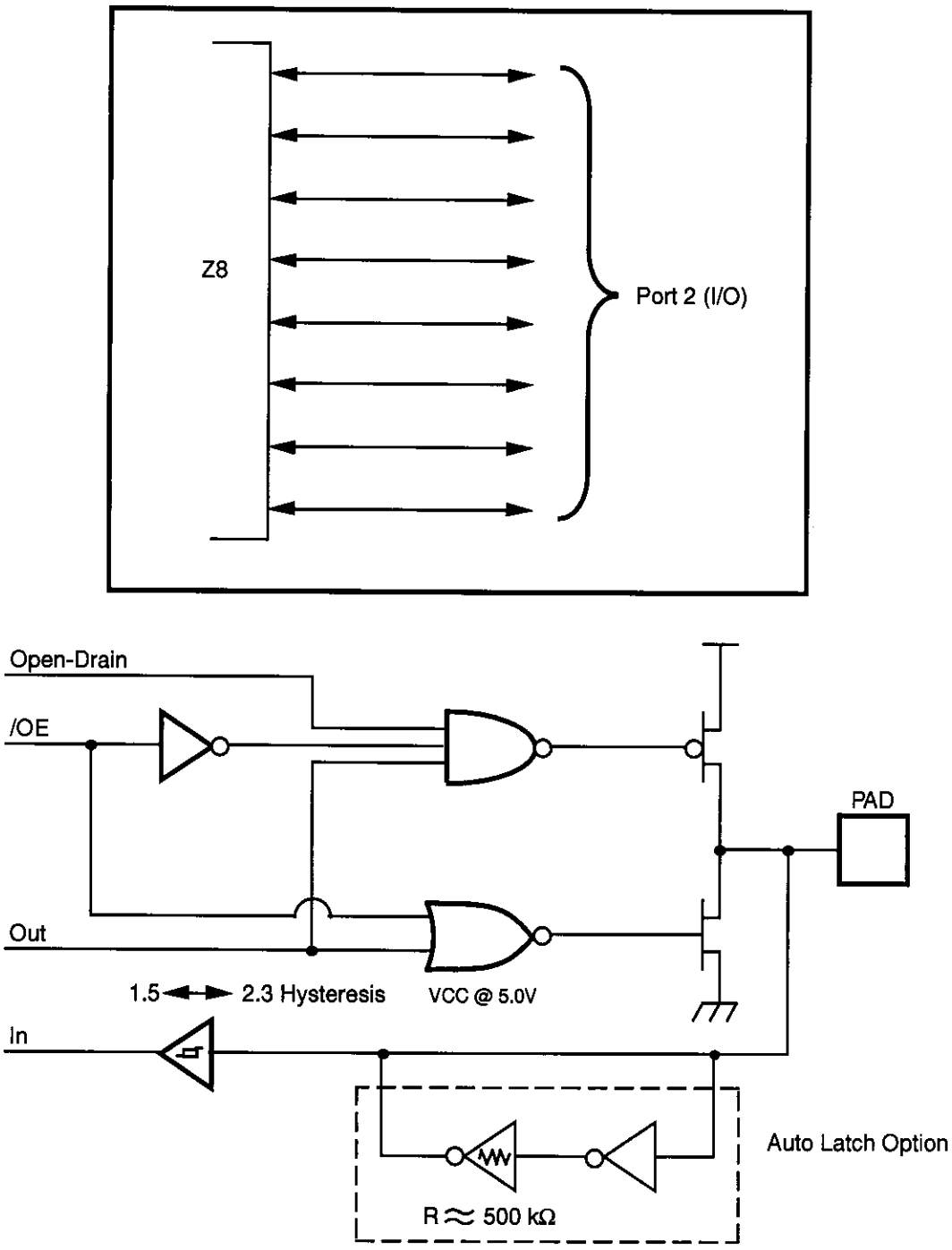



**Figure 8. Port 2 Configuration**

## PIN FUNCTIONS (Continued)

**Port 3, P33–P31.** Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal $T_{IN}$ (Figure 9).

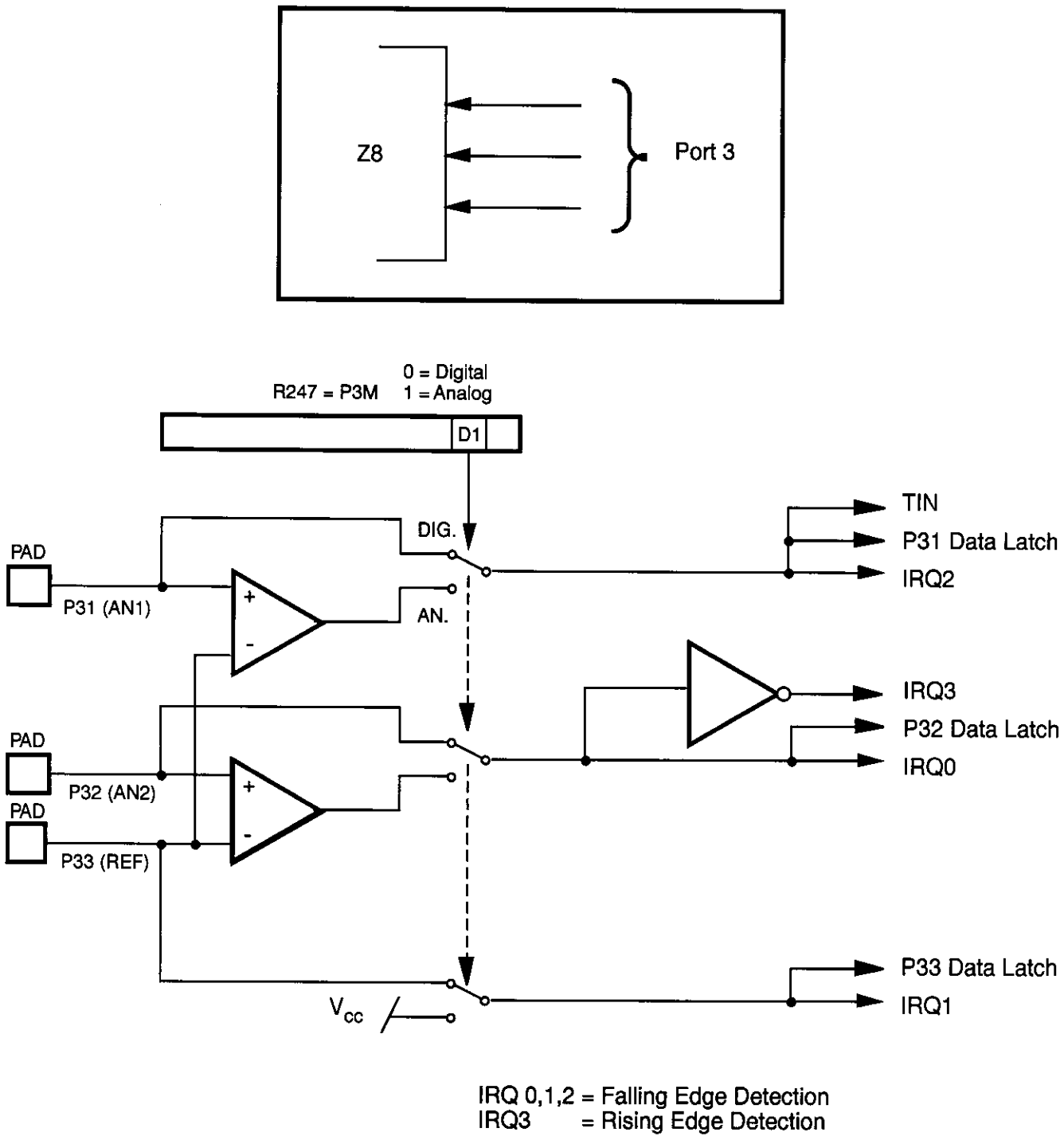



**Figure 9. Port 3 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0–4 V when the $V_{CC}$ is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or $T_{IN}$ through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

**RESET.** This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

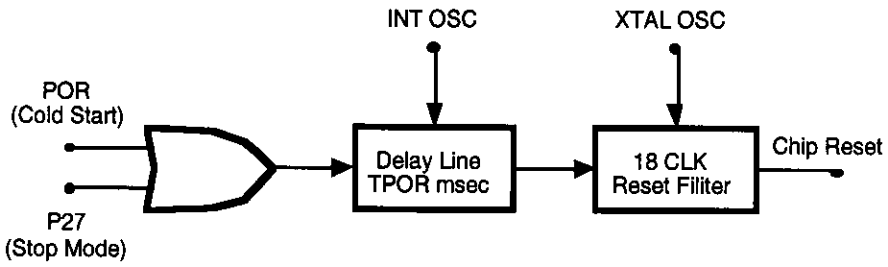



**Figure 10. Internal Reset Configuration**

**Power-On Reset (POR).** A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows $V_{CC}$ and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

**Watch-Dog Timer Reset.** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

**Note:** User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

**Table 4. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | AN2(P32) | 0,1 | External (F)Edge |
| IRQ1 | REF(P33) | 2,3 | External (F)Edge |
| IRQ2 | AN1(P31) | 4,5 | External (F)Edge |
| IRQ3 | AN2(P32) | 6,7 | External (R)Edge |
| IRQ4 | T0 | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |

**Notes:**
F = Falling edge triggered
R = Rising edge triggered

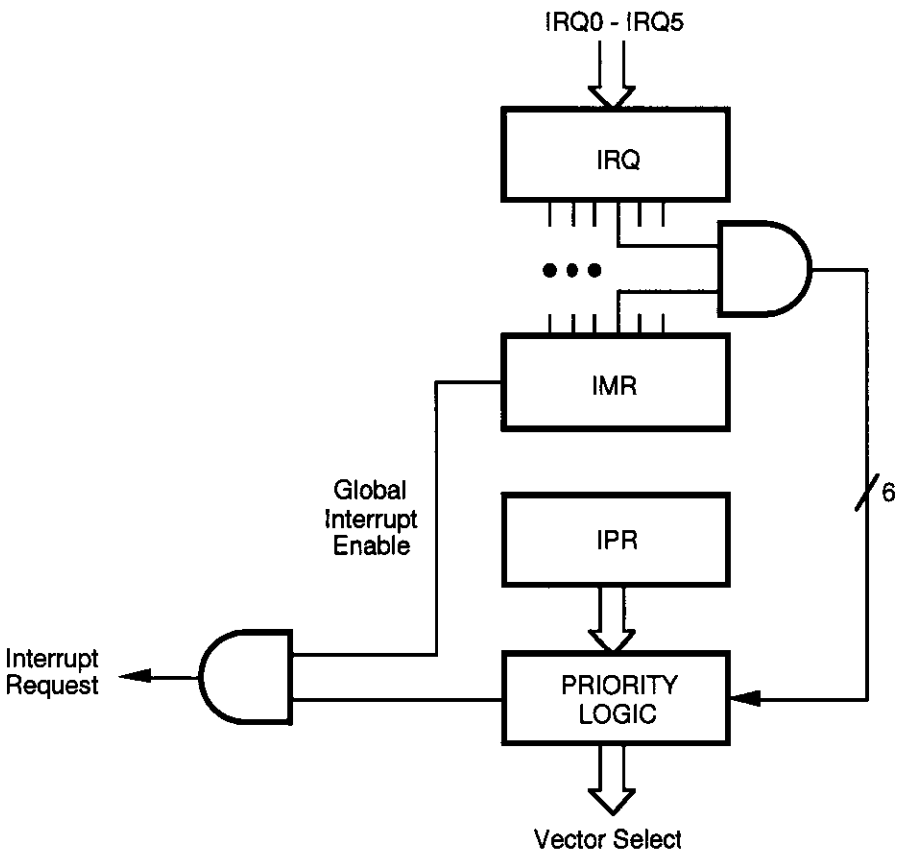
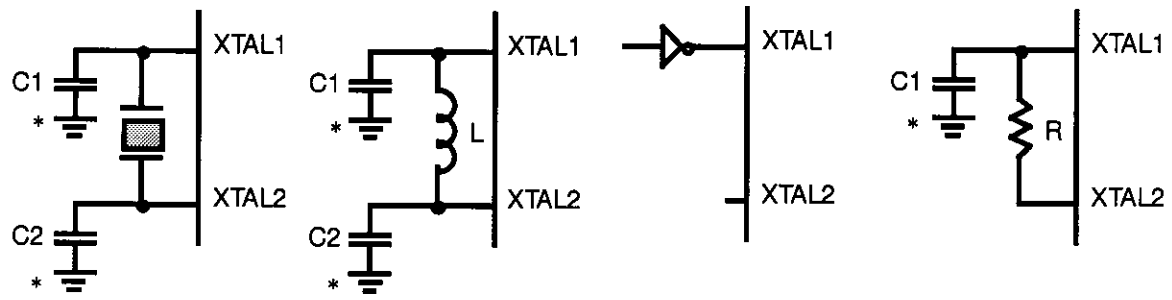



**Figure 15. Interrupt Block Diagram**

**Clock.** The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to $V_{SS}$, Pin 14 to reduce Ground noise injection.




Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC

External Clock

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz

* Typical value including pin parasitics

**Figure 16. Oscillator Configuration**

## FUNCTIONAL DESCRIPTION (Continued)

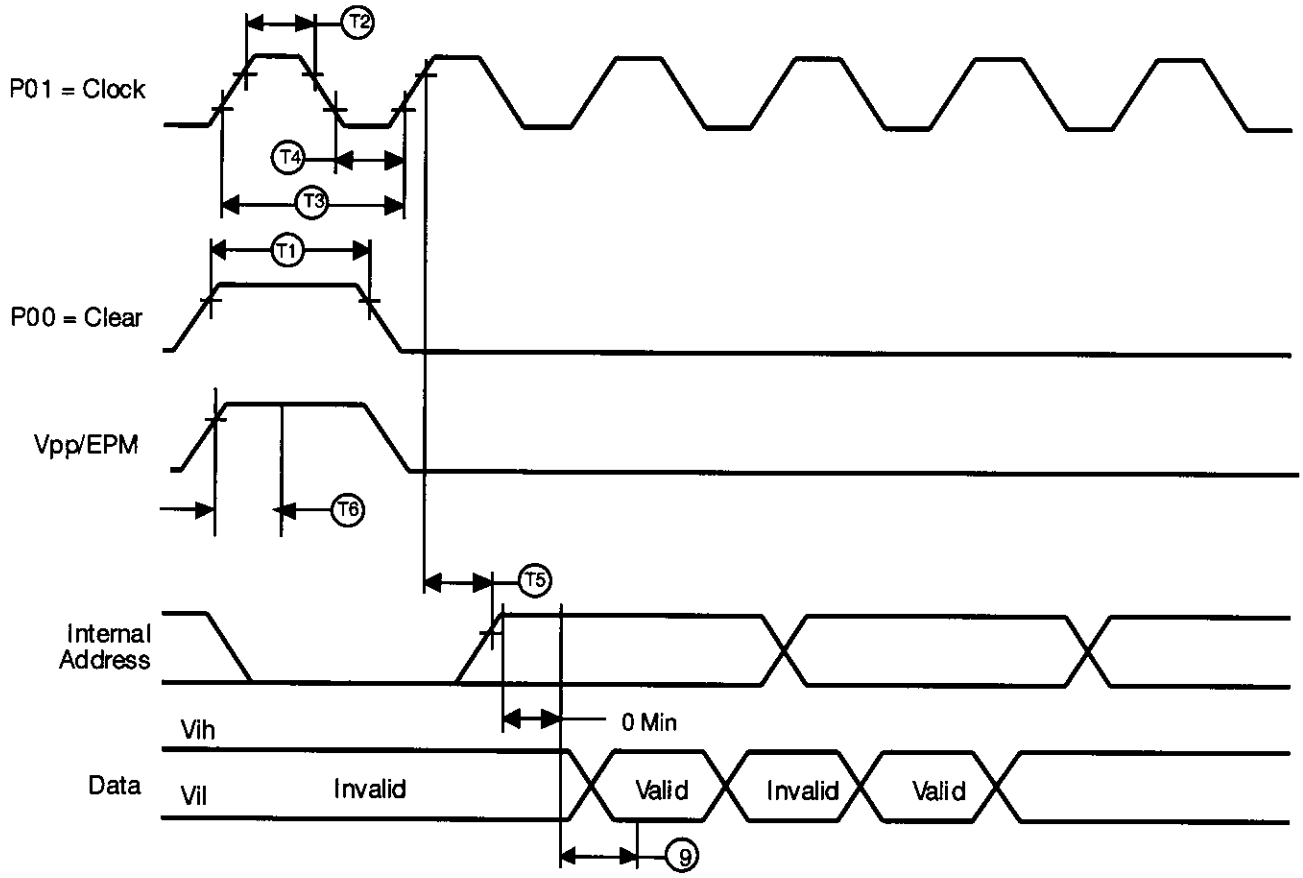
**Internal Address Counter.** The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

**Programming Waveform.** Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 23 shows the flow chart of the Z8 programming algorithm.

**Table 8. Timing of Programming Waveforms**

| Parameters | Name | Min | Max | Units |
|---|---|---|---|---|
| 1 | Address Setup Time | 2 | | µs |
| 2 | Data Setup Time | 2 | | µs |
| 3 | $V_{PP}$ Setup | 2 | | µs |
| 4 | $V_{CC}$ Setup Time | 2 | | µs |
| 5 | Chip Enable Setup Time | 2 | | µs |
| 6 | Program Pulse Width | 0.95 | | ms |
| 7 | Data Hold Time | 2 | | µs |
| 8 | $\overline{OE}$ Setup Time | 2 | | µs |
| 9 | Data Access Time | 188 | | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | µs |
| 13 | $\overline{PGM}$ Setup Time | 2 | | µs |
| 14 | Address to $\overline{OE}$ Setup Time | 2 | | µs |
| 15 | Option Program Pulse Width | 78 | | ms |
| 16 | $\overline{OE}$ Width | 250 | | ns |
| 17 | Address Valid to $\overline{OE}$ Low | 125 | | ns |




| Legend: | |
|---|---|
| T1 Reset Clock Width | 30 ns Min |
| T2 Input Clock High | 100 ns Min |
| T3 Input Clock Period | 200 ns Min |
| T4 Input Clock Low | 100 ns Min |
| T5 Clock to Address Counter Out Delay | 15 ns Max |
| T6 Epm/Vpp Set up Time | 40 µs Min |

**Figure 18. Z86E04/E08 Address Counter Waveform**

## FUNCTIONAL DESCRIPTION (Continued)

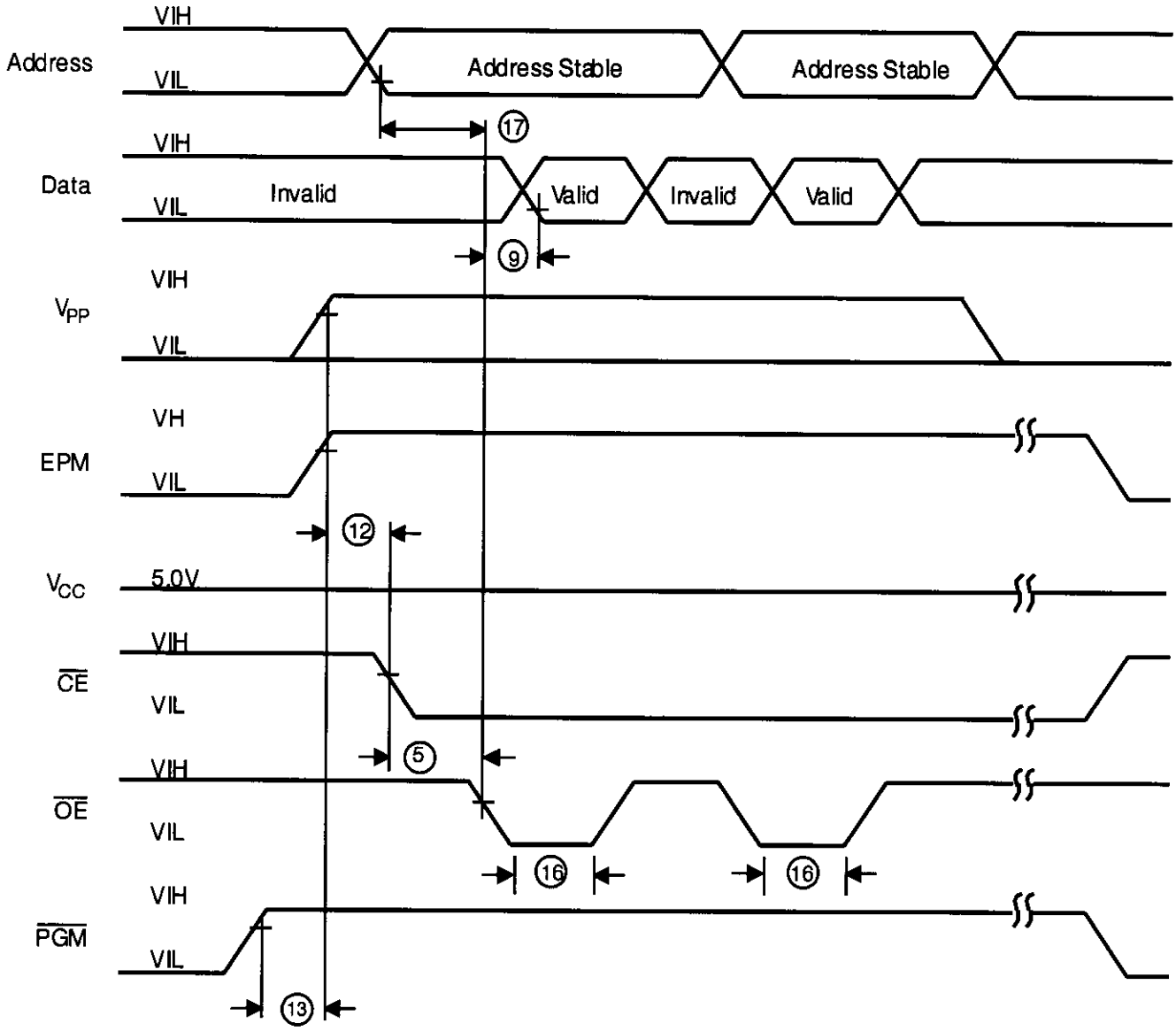



**Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)**

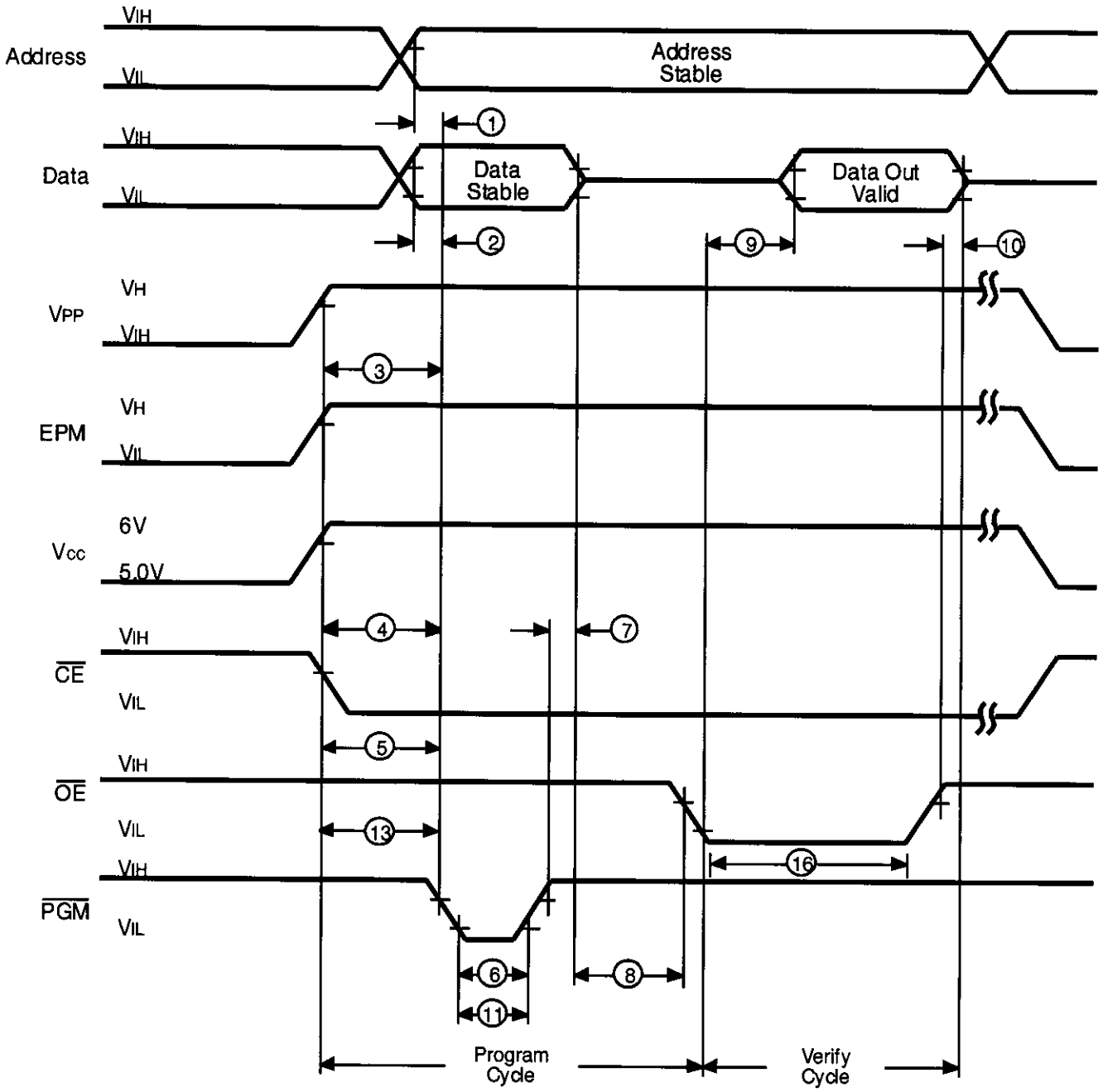



**Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)**

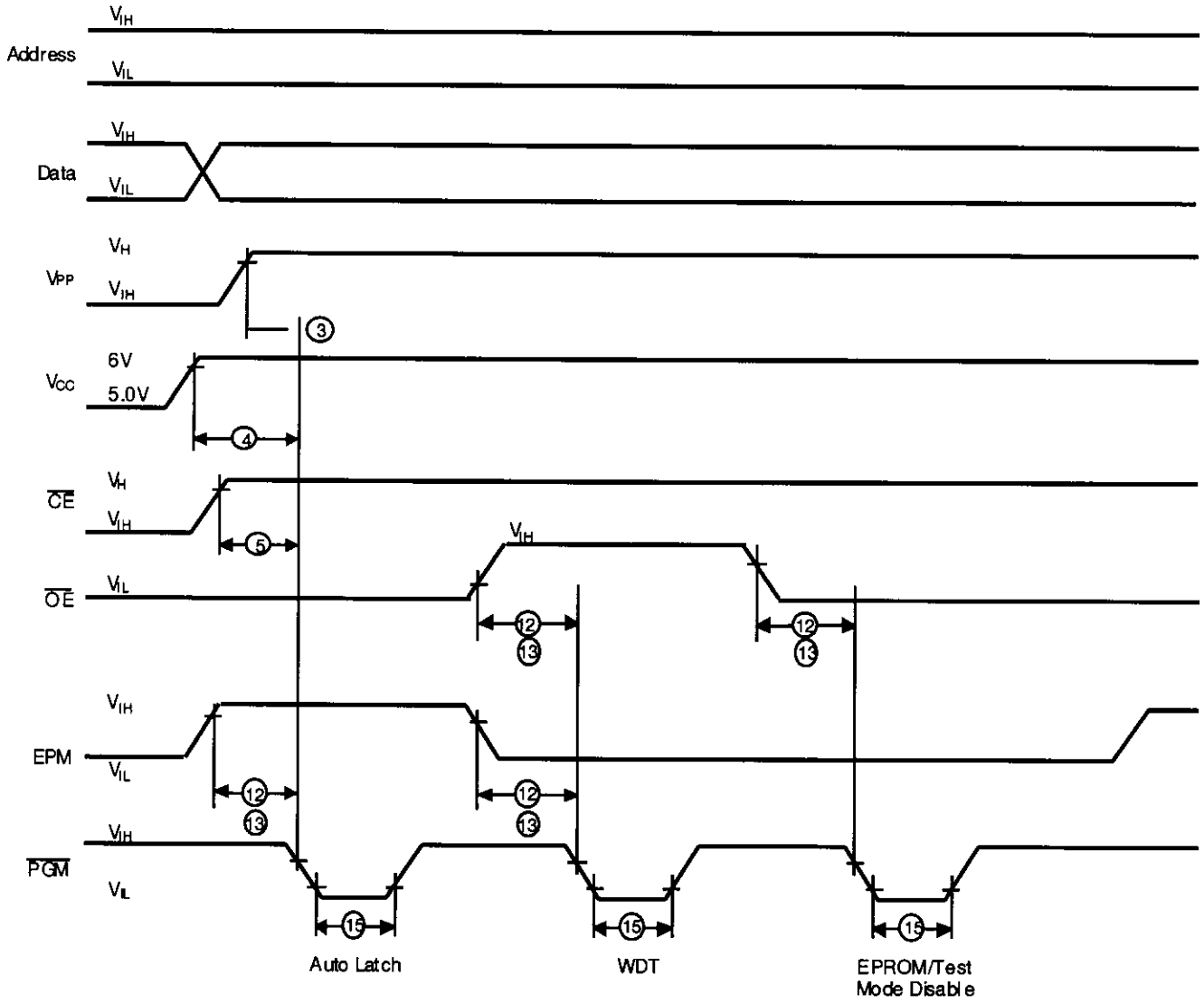



**Figure 22. Z86E04/E08 Programming Options Waveform (Auto Latch Disable, Permanent WDT Enable and EPROM/Test Mode Disable)**

## FUNCTIONAL DESCRIPTION (Continued)

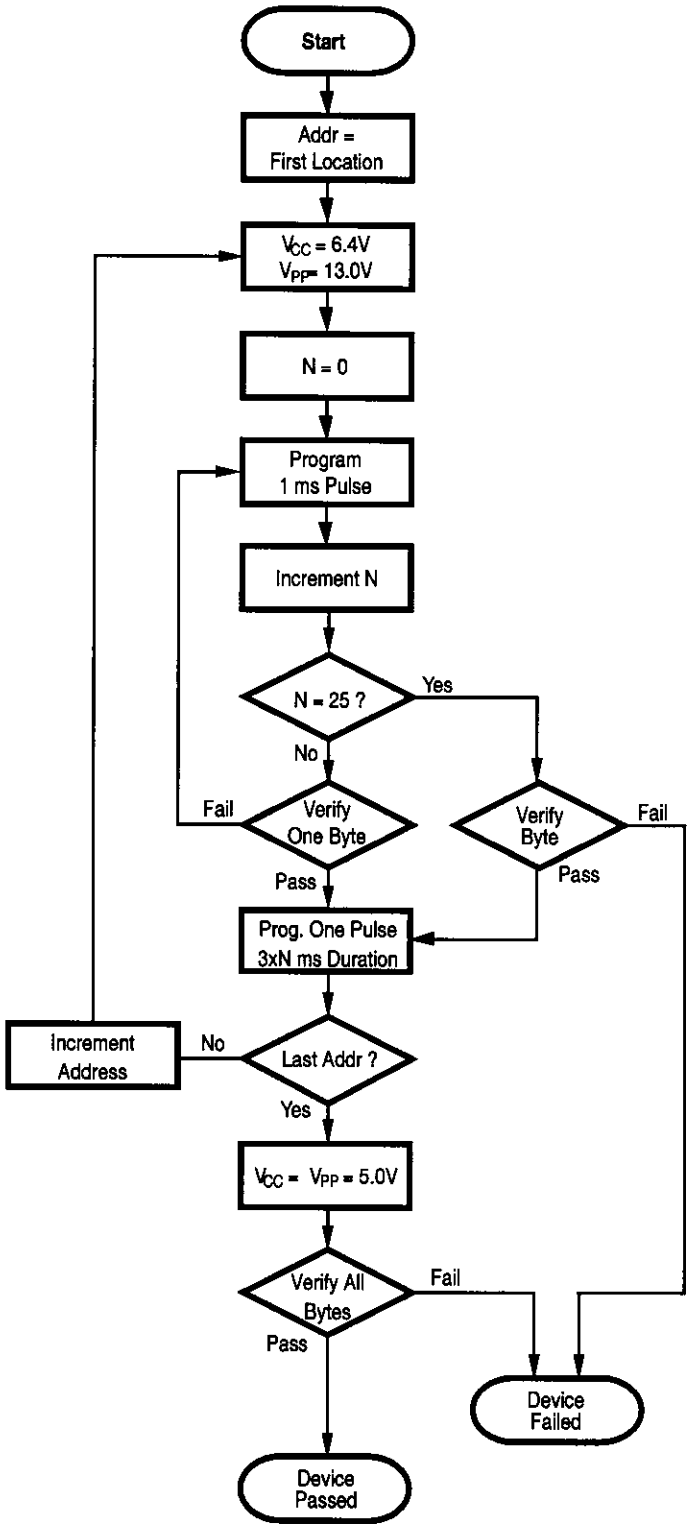



**Figure 23. Z86E04/E08 Programming Algorithm**

## Z8 CONTROL REGISTERS

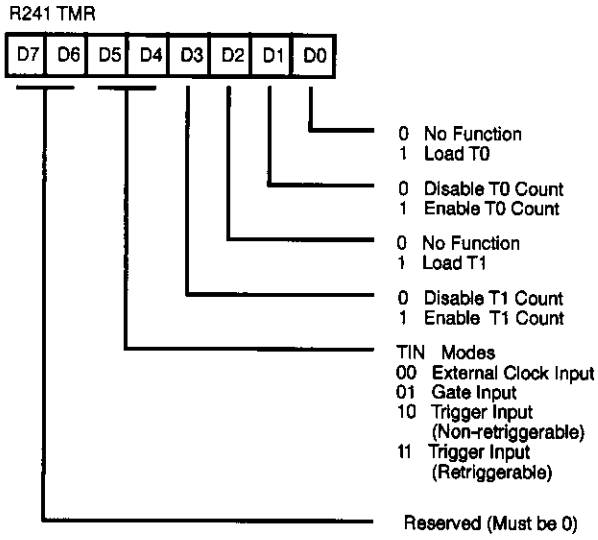



**Figure 24. Timer Mode Register ($F1_H$: Read/Write)**

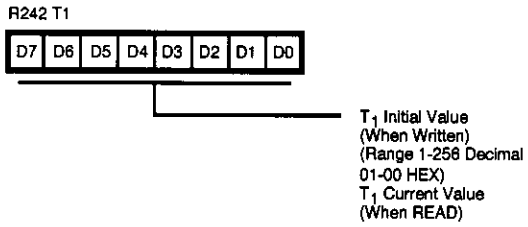



**Figure 25. Counter Timer 1 Register ($F2_H$: Read/Write)**

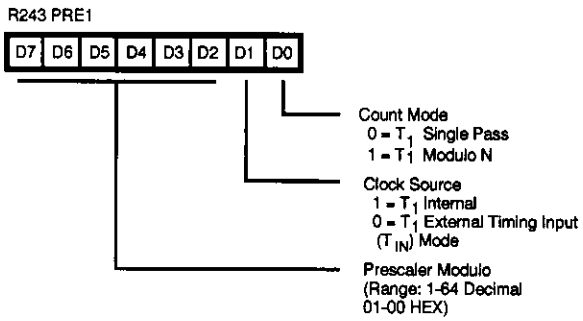



**Figure 26. Prescaler 1 Register ($F3_H$: Write Only)**

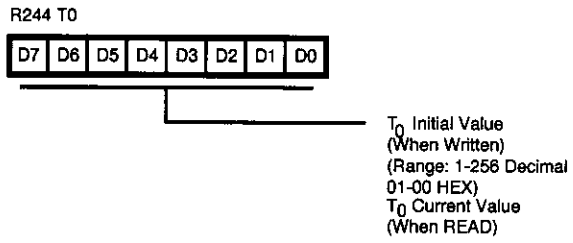



**Figure 27. Counter/Timer 0 Register ($F4_H$: Read/Write)**

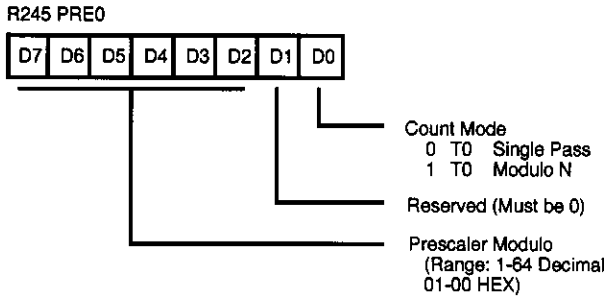



**Figure 28. Prescaler 0 Register ($F5_H$: Write Only)**

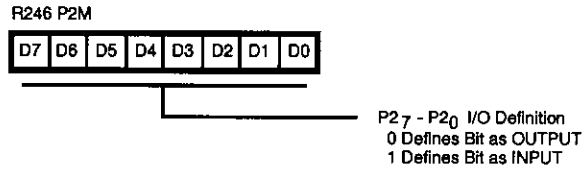



**Figure 29. Port 2 Mode Register ($F6_H$: Write Only)**

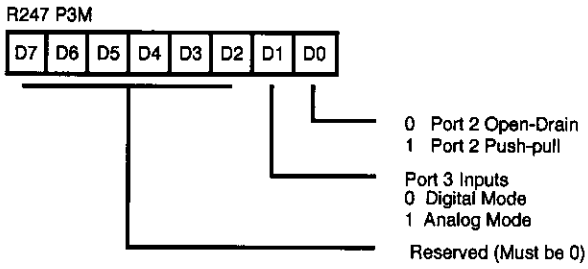



**Figure 30. Port 3 Mode Register ($F7_H$: Write Only)**

## ORDERING INFORMATION

| Z86E04 | | Z86E08 | |
|---|---|---|---|
| Standard Temperature | | Standard Temperature | |
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86E0412PSC | Z86E0412SSC | Z86E0812PSC | Z86E0812SSC |
| Z86E0412PEC | Z86E0412SEC | Z86E0812PEC | Z86E0812SEC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

### Codes

**Preferred Package**
P = Plastic DIP

**Longer Lead Time**
S = SOIC

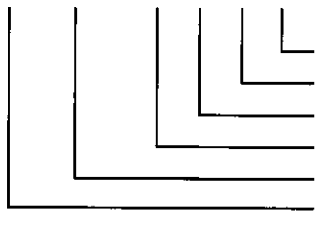
**Preferred Temperature**
S = 0°C to +70°C
E = –40°C to +105°C

**Speeds**
12 =12 MHz

**Environmental**
C = Plastic Standard

### Example:

**Z 86E04 12 P S C** is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.



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