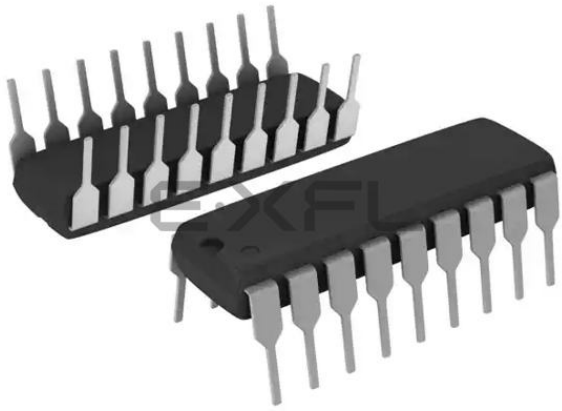

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812pec1903

GENERAL DESCRIPTION (Continued)

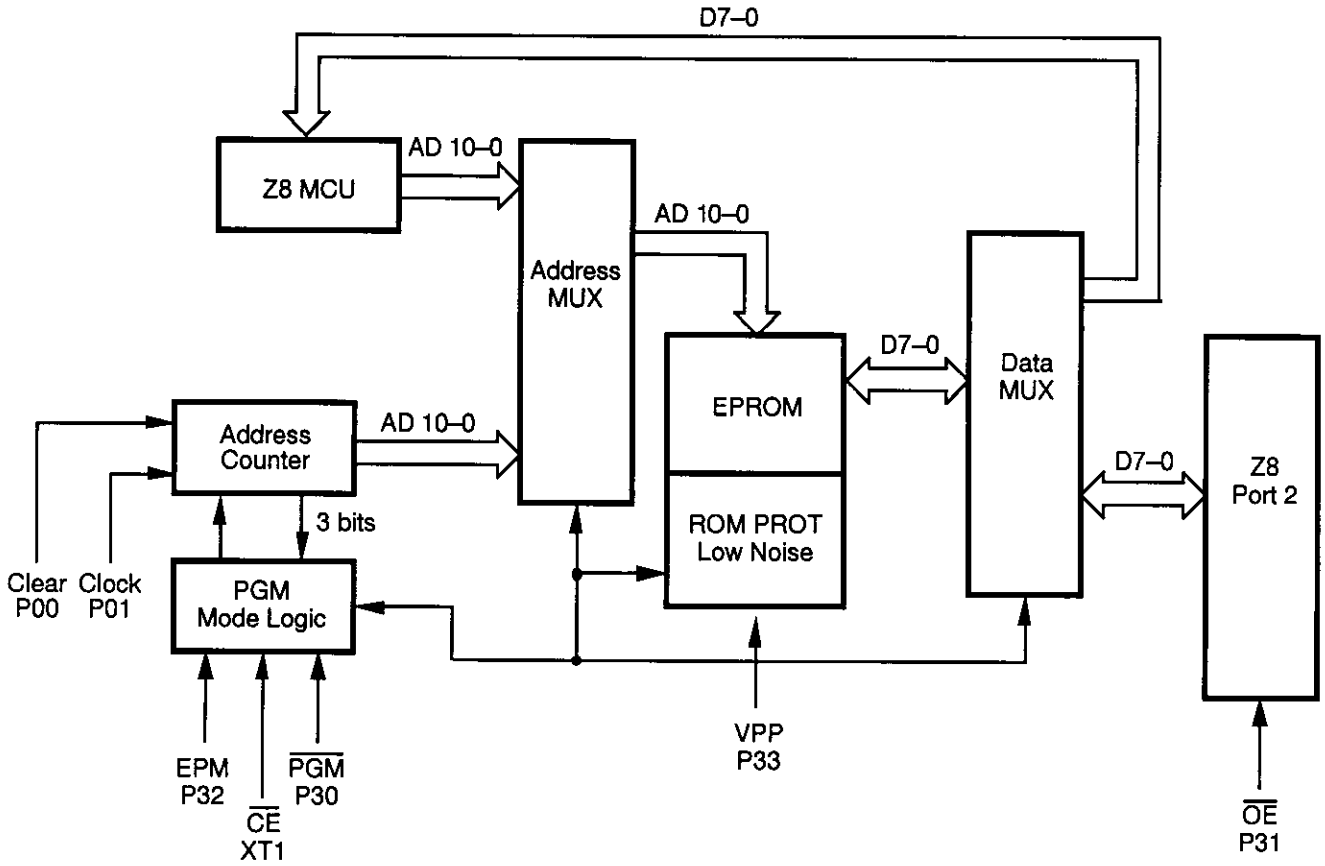


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

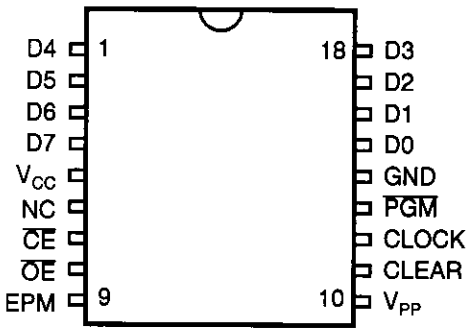


Figure 3. 18-Pin EPROM Mode Configuration

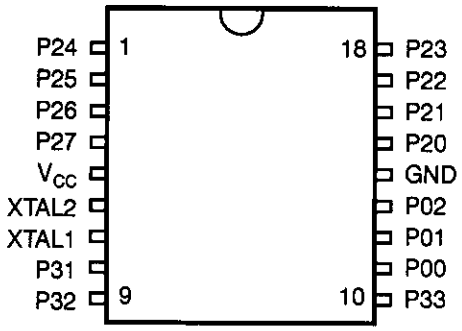


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	NC	No Connection	
7	$\overline{CE}$	Chip Enable	Input
8	$\overline{OE}$	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	$\overline{PGM}$	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0,1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10.0	1.0	µA	STOP Mode V_{IN} = 0V,V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		32.0	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–16.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5 to 5.5V, typical values measured at V_{CC} = 5.0V.
   The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

DC ELECTRICAL CHARACTERISTICS

Extended Temperature

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{INMAX}	Max Input Voltage	4.5V		12.0		V	I_{IN} < 250 µA	1
		5.5V		12.0		V	I_{IN} < 250 µA	1
V_{CH}	Clock Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	5
		4.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4			V	Low Noise @ I_{OH} = –0.5 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I_{OL} = +12 mA,	5
		5.5V		1.0	0.3	V	I_{OL} = +12 mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V		–1.0	1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	V_{CC} –1.5		V		

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bidirectional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

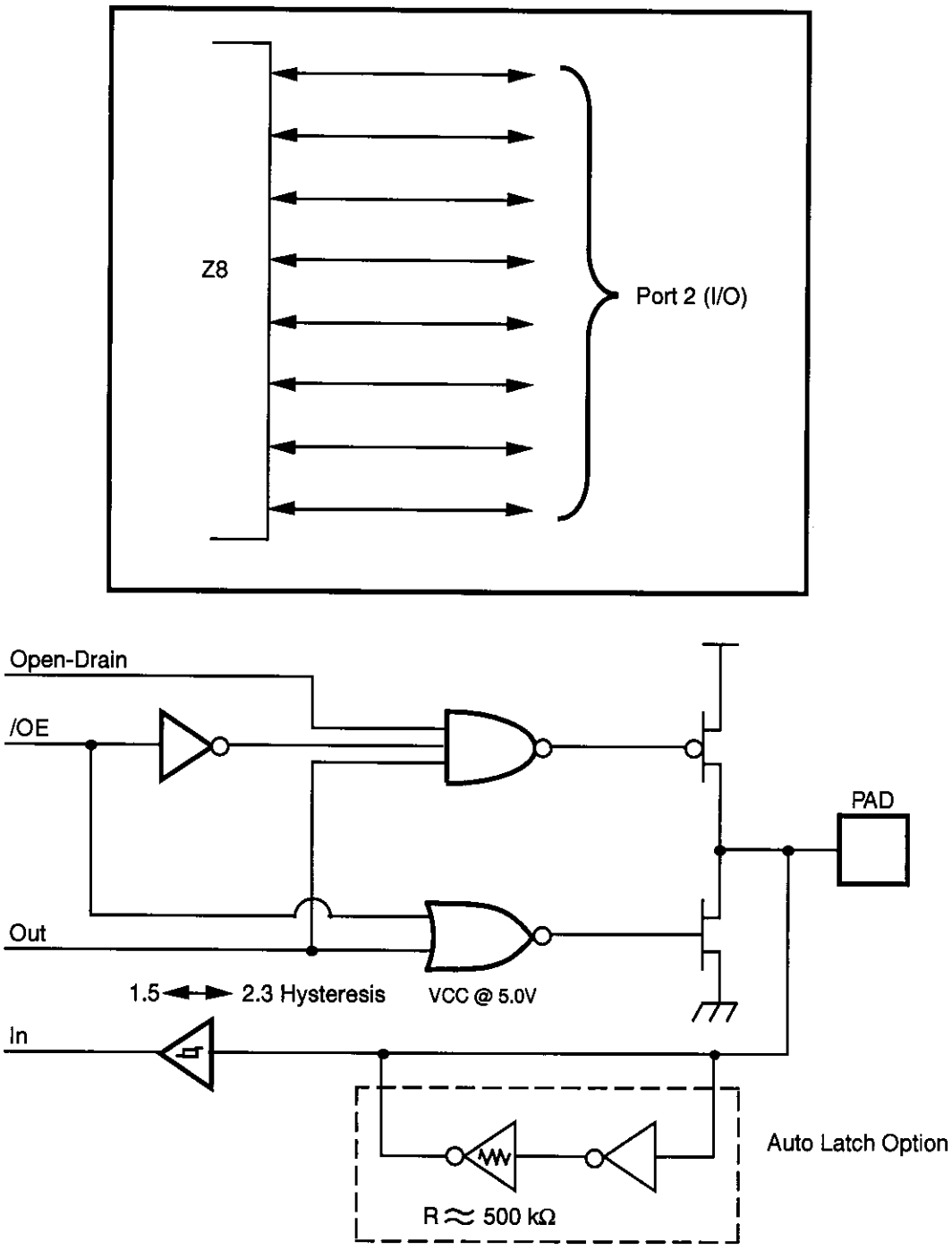


Figure 8. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).

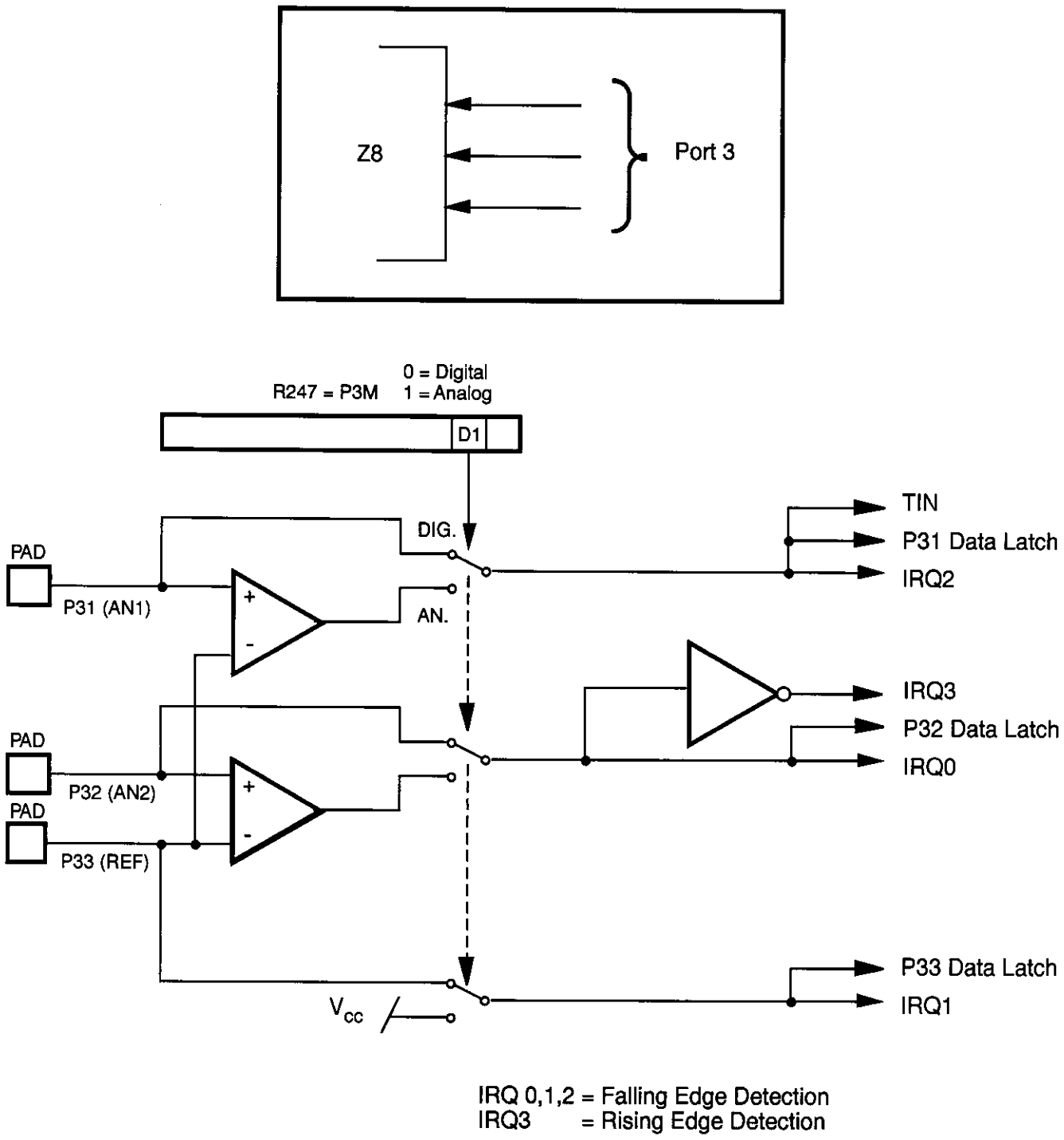


Figure 9. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

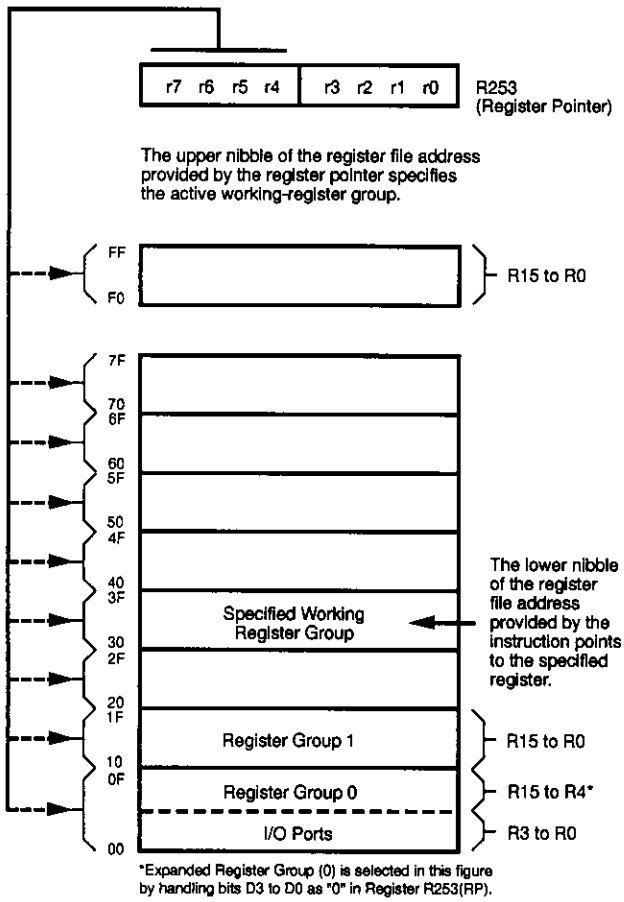


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

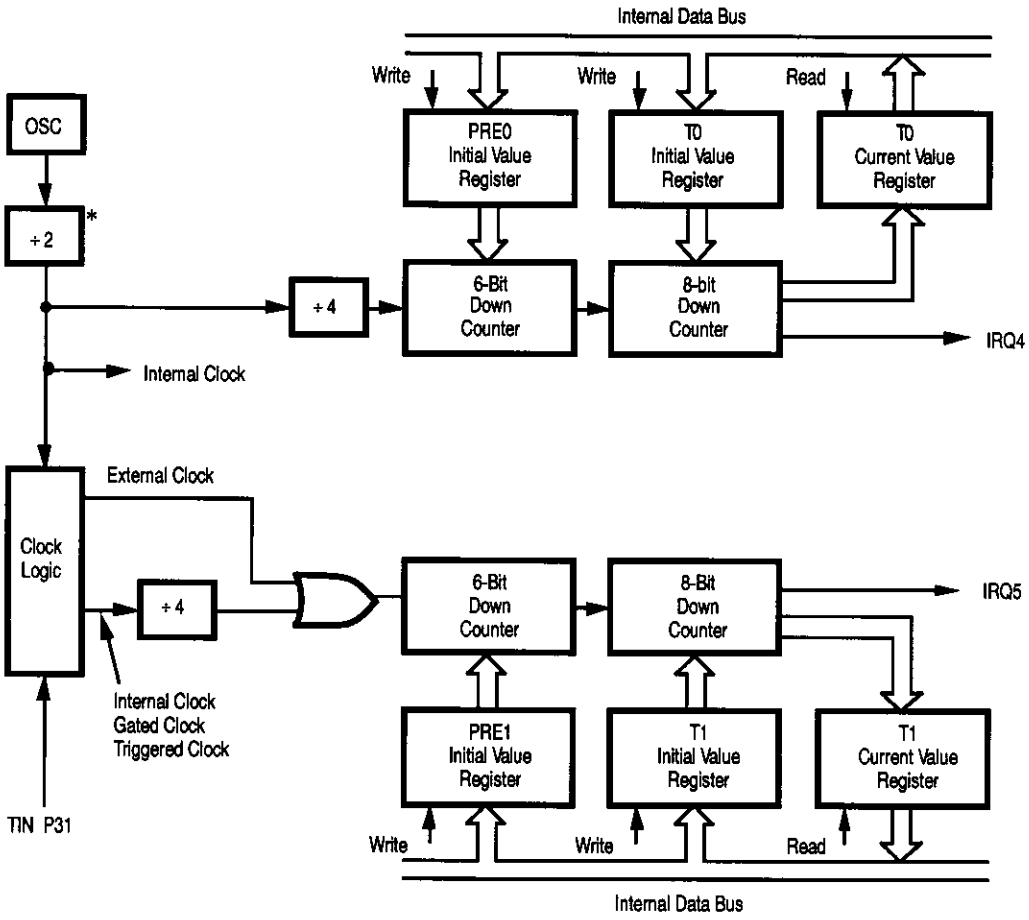
General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.



* **Note**: By passed, if Low EMI Mode is selected.

Figure 14. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

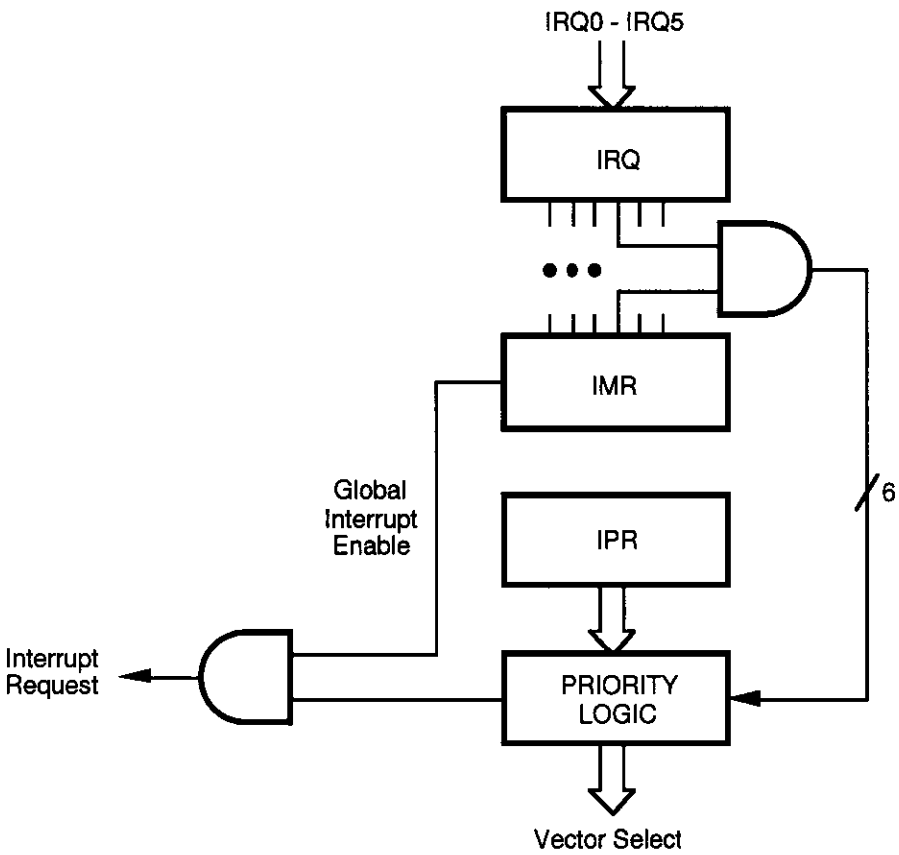


Figure 15. Interrupt Block Diagram

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
            or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}.

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

FUNCTIONAL DESCRIPTION (Continued)

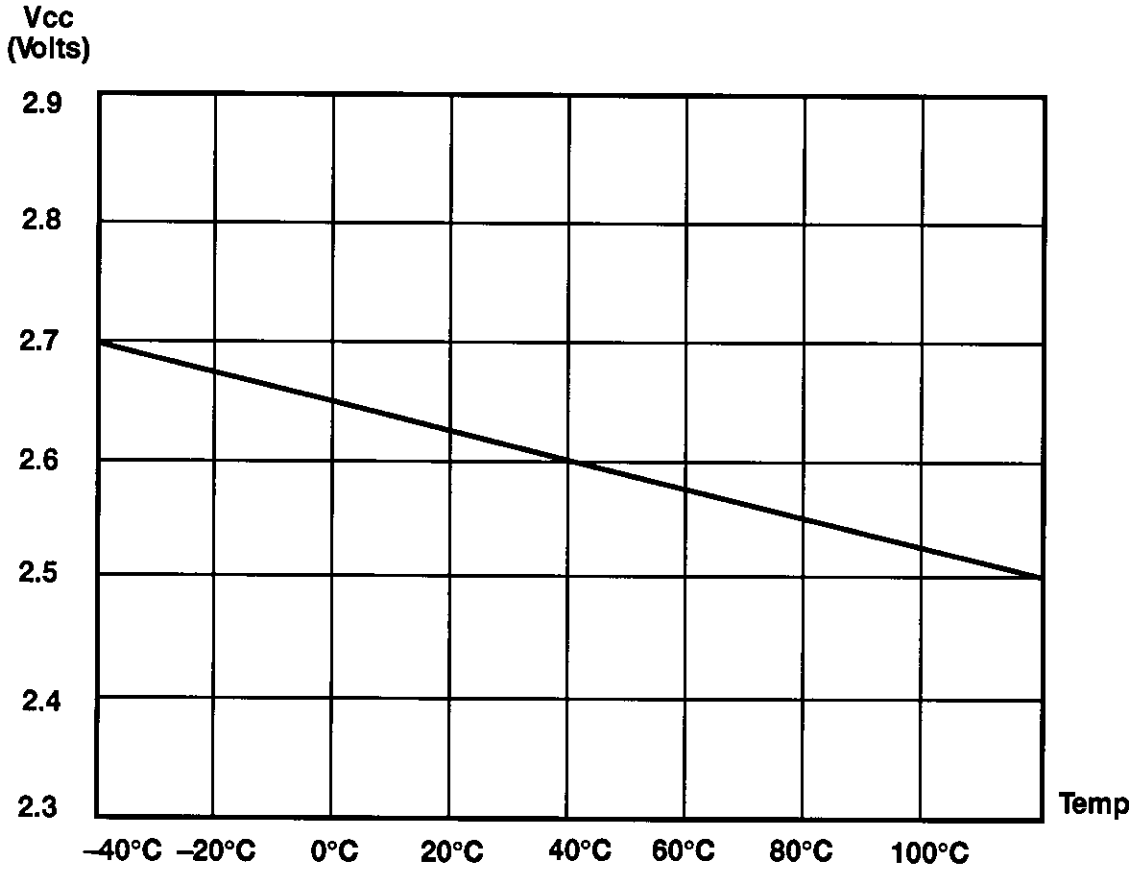


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

FUNCTIONAL DESCRIPTION (Continued)

Internal Address Counter. The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

Programming Waveform. Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

Programming Algorithm. Figure 23 shows the flow chart of the Z8 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms
16	$\overline{OE}$ Width	250		ns
17	Address Valid to $\overline{OE}$ Low	125		ns

FUNCTIONAL DESCRIPTION (Continued)

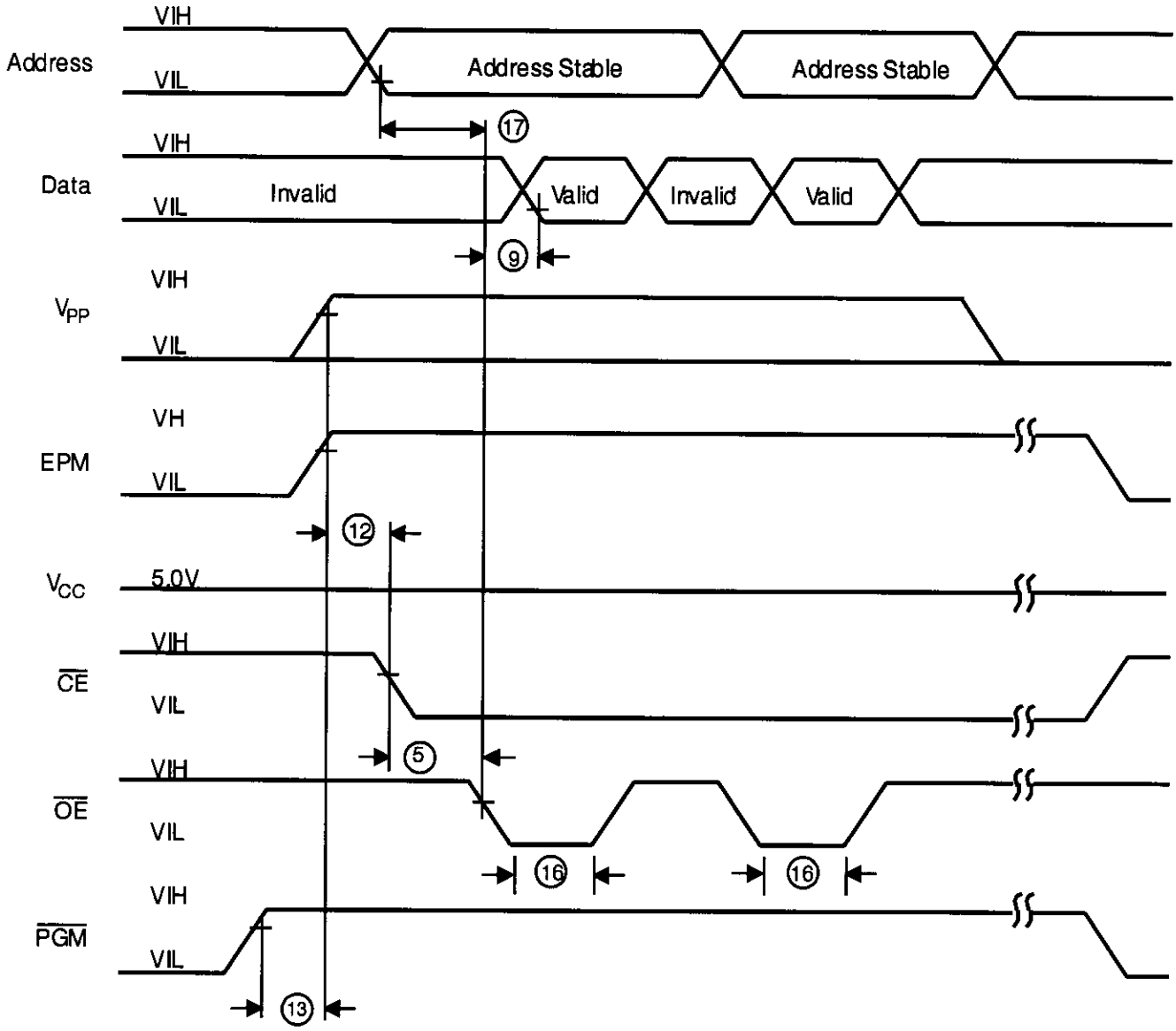


Figure 19. Z86E04/E08 Programming Waveform (EPROM Read)

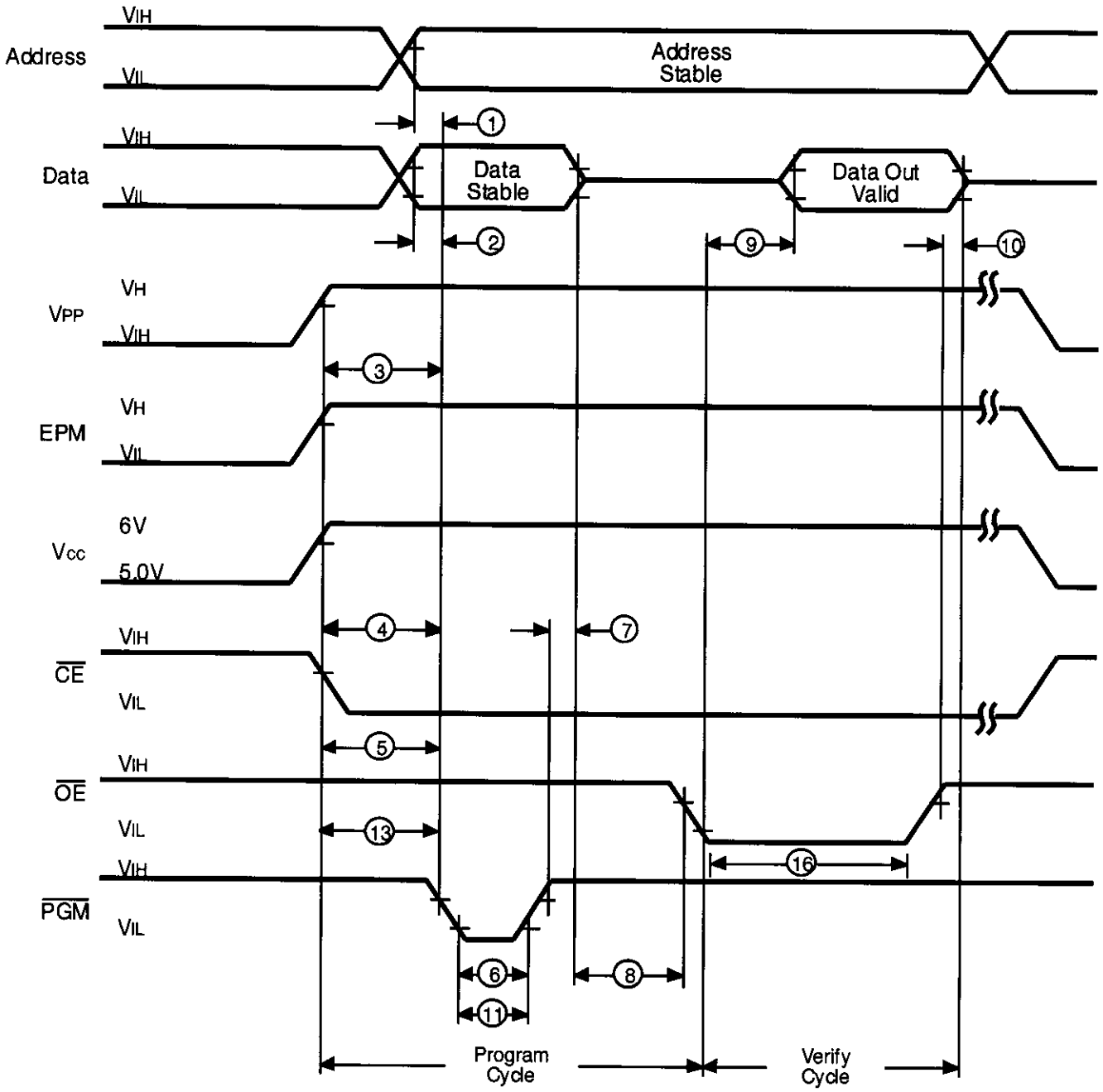


Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)

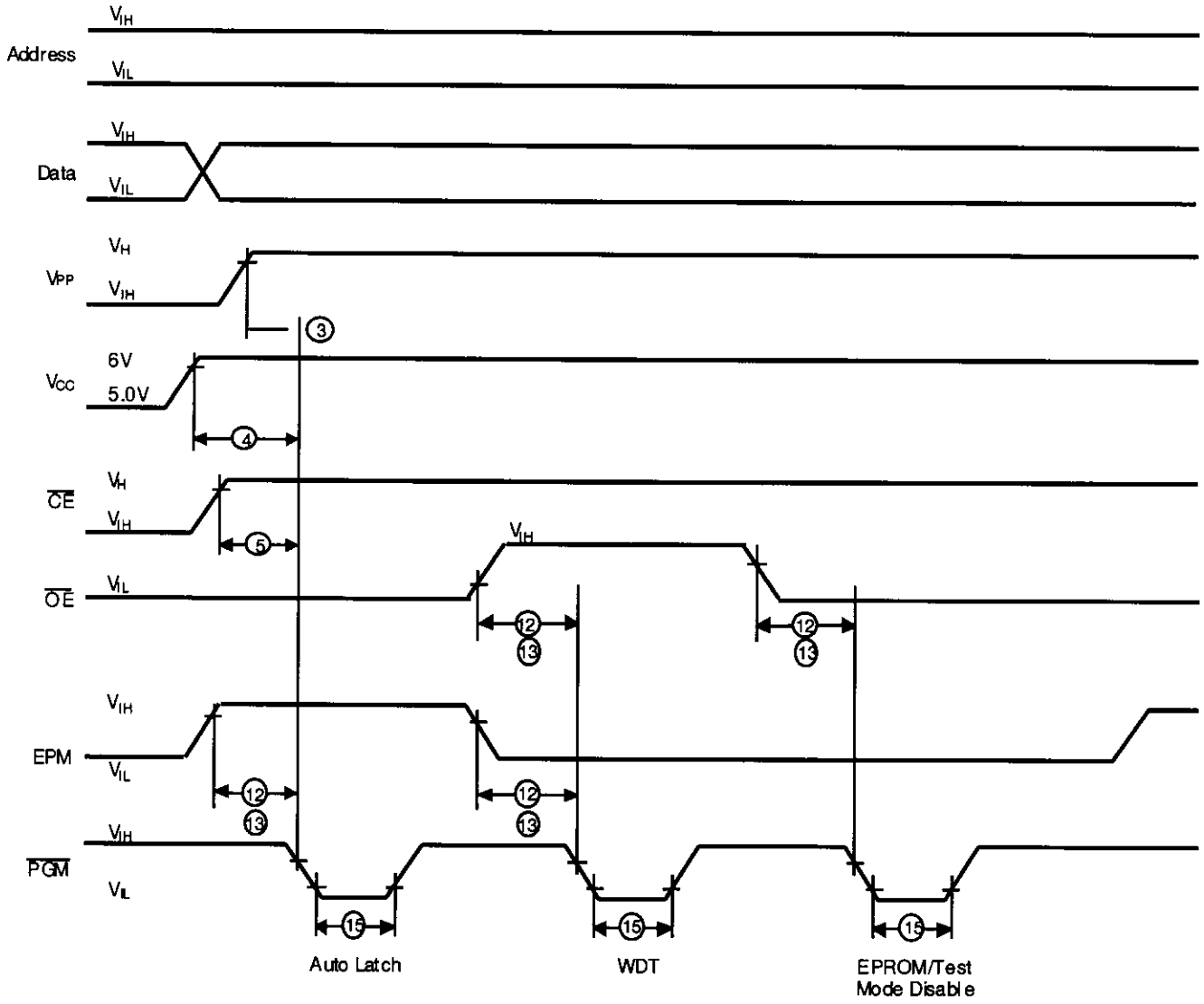


Figure 22. Z86E04/E08 Programming Options Waveform (Auto Latch Disable, Permanent WDT Enable and EPROM/Test Mode Disable)

FUNCTIONAL DESCRIPTION (Continued)

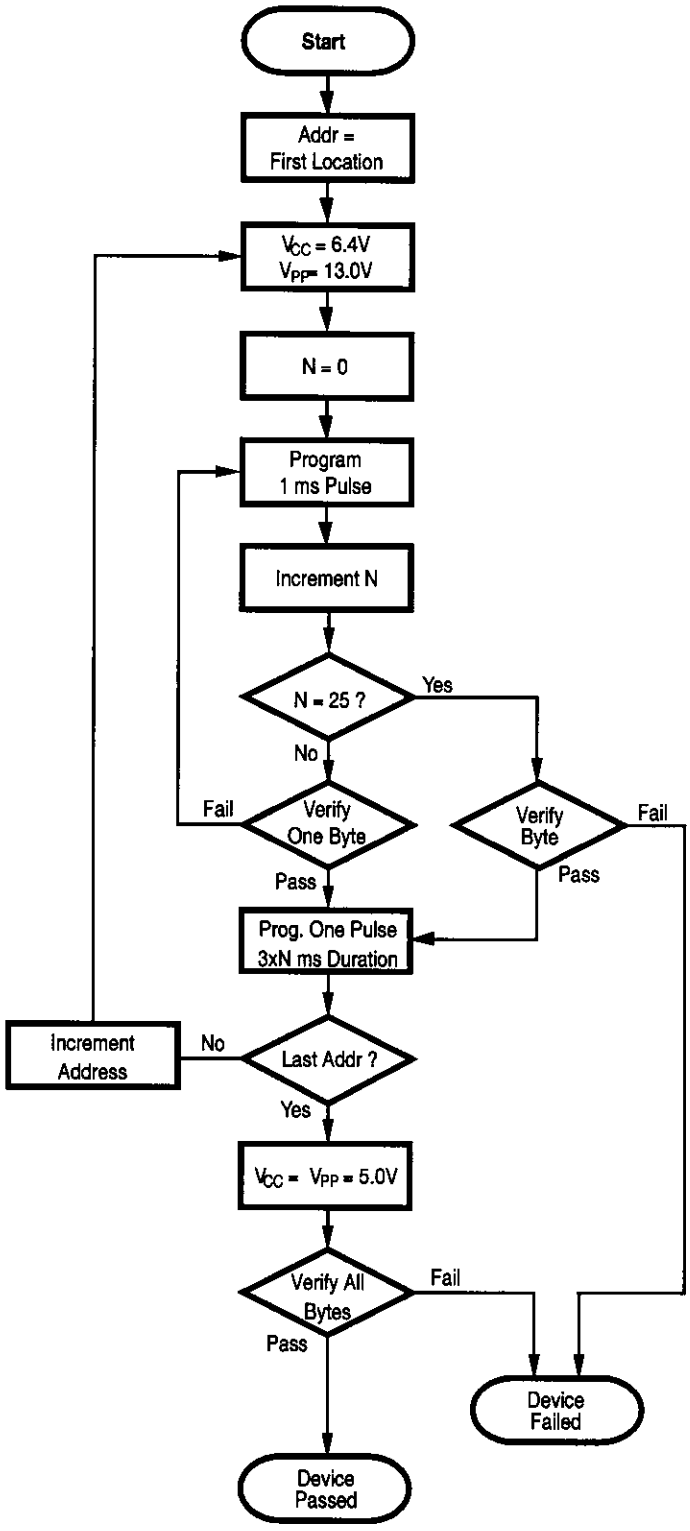


Figure 23. Z86E04/E08 Programming Algorithm

Z8 CONTROL REGISTERS

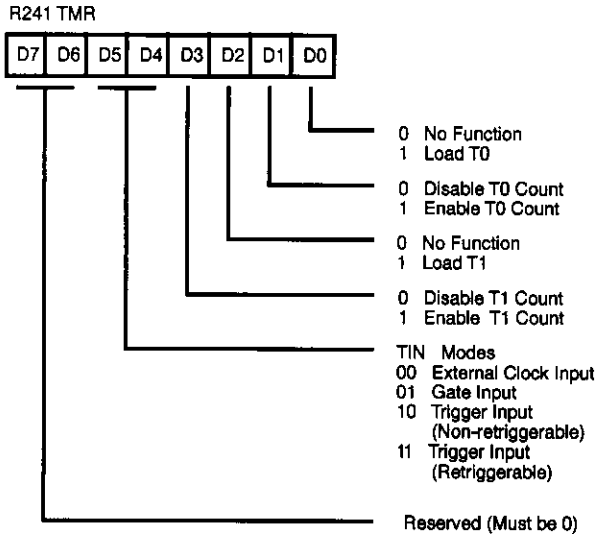


Figure 24. Timer Mode Register ($F1_H$: Read/Write)

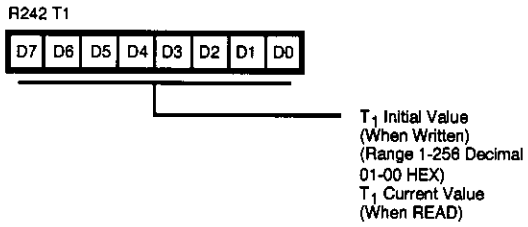


Figure 25. Counter Timer 1 Register ($F2_H$: Read/Write)

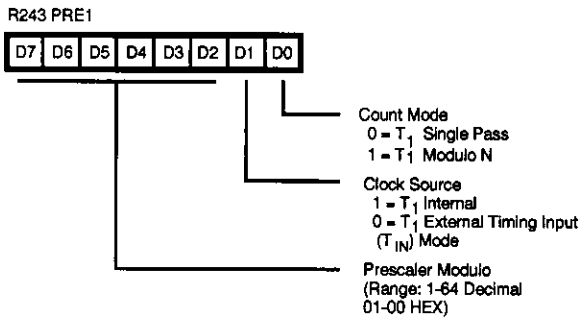


Figure 26. Prescaler 1 Register ($F3_H$: Write Only)

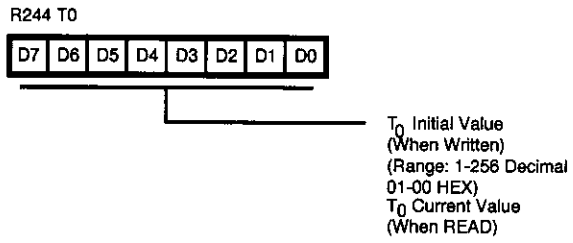


Figure 27. Counter/Timer 0 Register ($F4_H$: Read/Write)

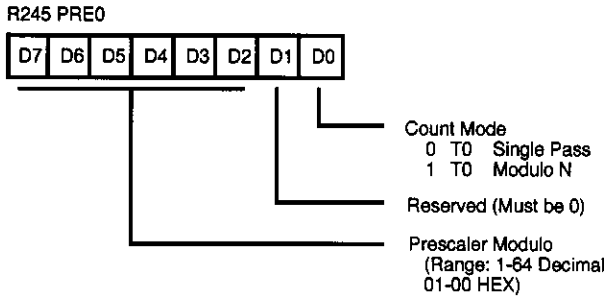


Figure 28. Prescaler 0 Register ($F5_H$: Write Only)

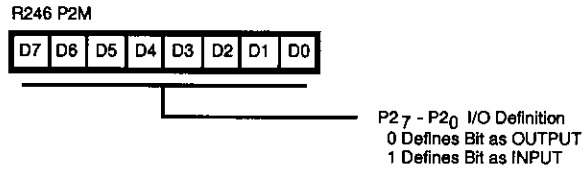


Figure 29. Port 2 Mode Register ($F6_H$: Write Only)

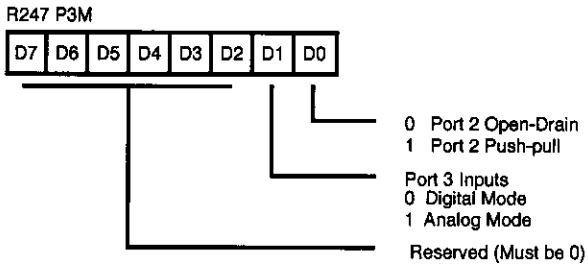


Figure 30. Port 3 Mode Register ($F7_H$: Write Only)

Z8 CONTROL REGISTERS (Continued)

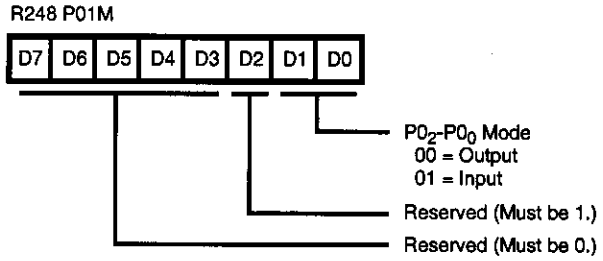


Figure 31. Port 0 and 1 Mode Register ($F8_H$: Write Only)

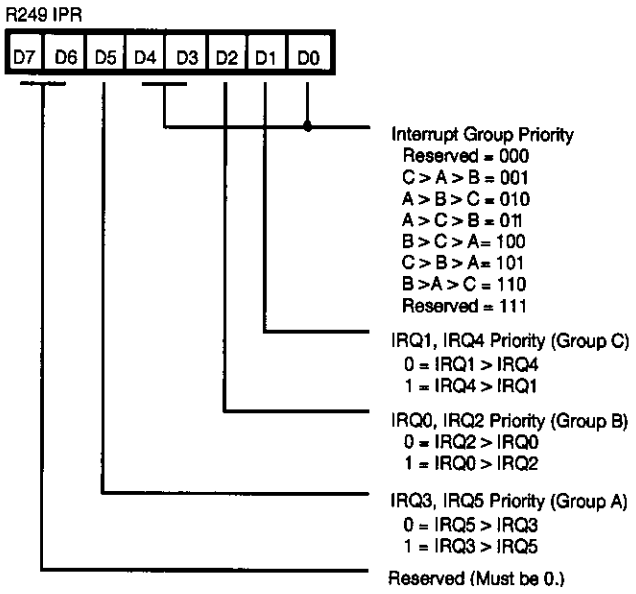


Figure 32. Interrupt Priority Register ($F9_H$: Write Only)

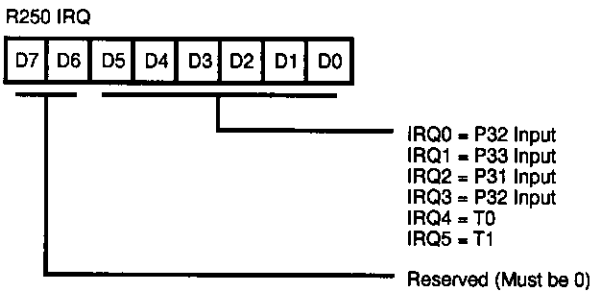


Figure 33. Interrupt Request Register (FA_H: Read/Write)

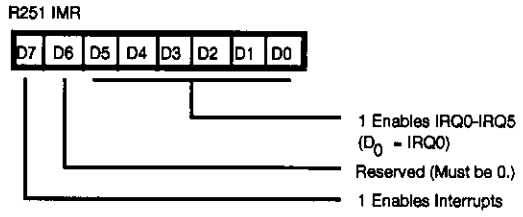


Figure 34. Interrupt Mask Register (FB_H: Read/Write)

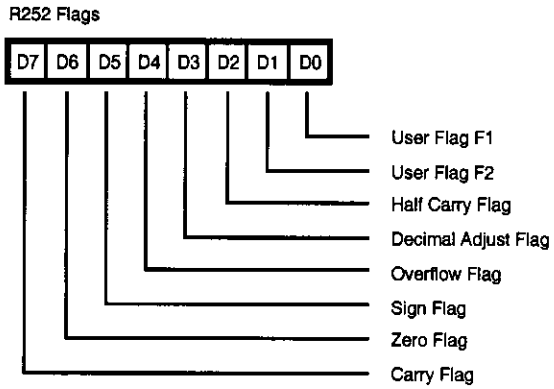


Figure 35. Flag Register (FC_H: Read/Write)

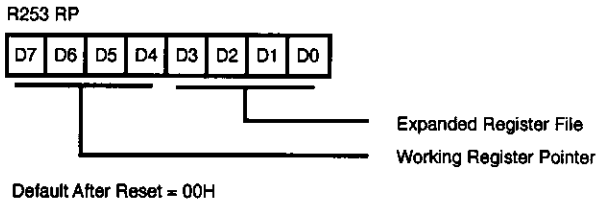


Figure 36. Register Pointer (FD_H: Read/Write)

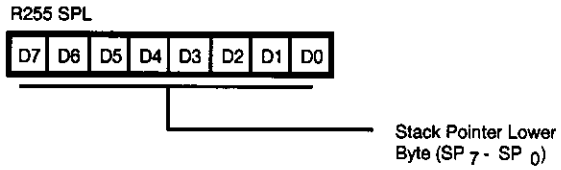


Figure 37. Stack Pointer (FF_H: Read/Write)

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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