What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

| Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812peg1903
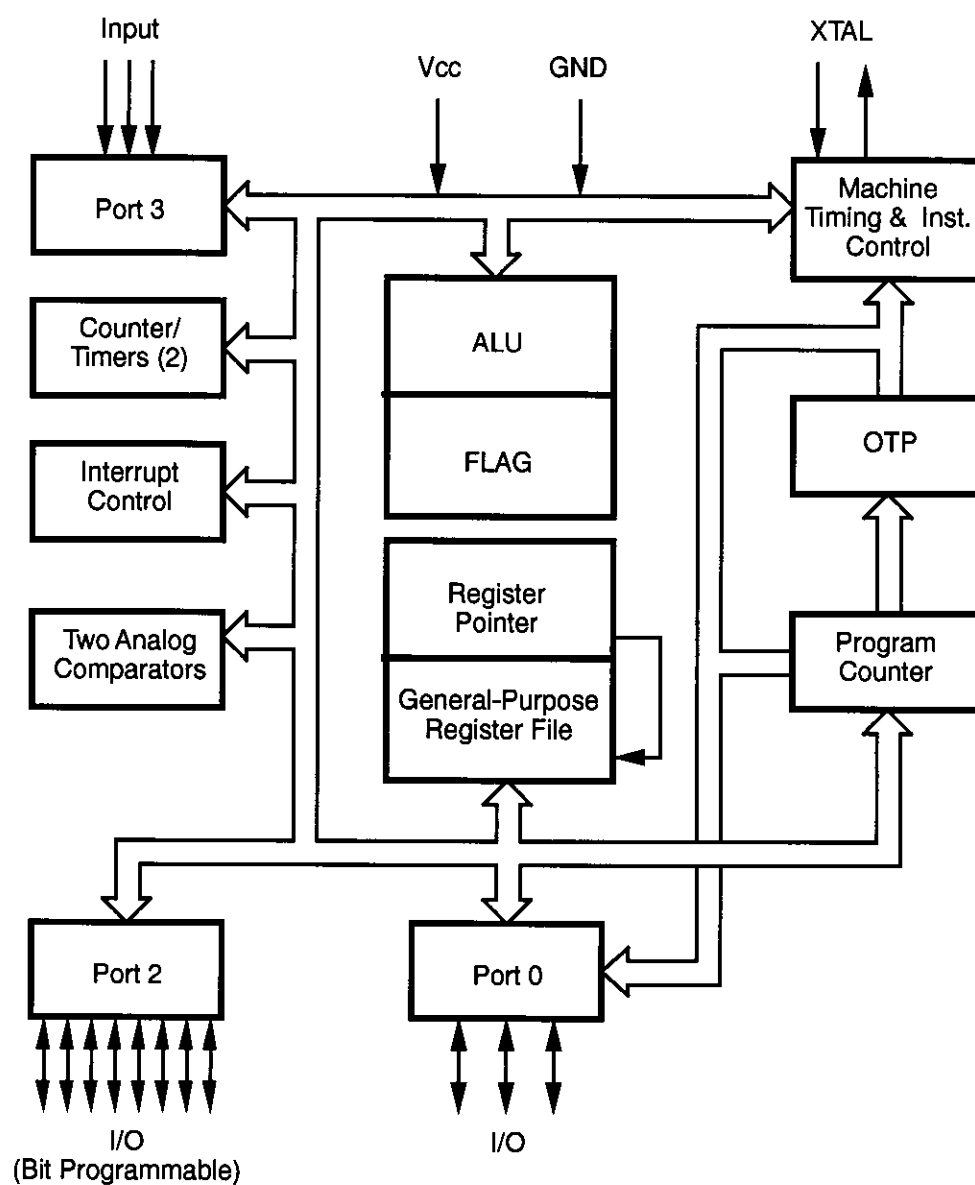
Figure 1. Functional Block Diagram

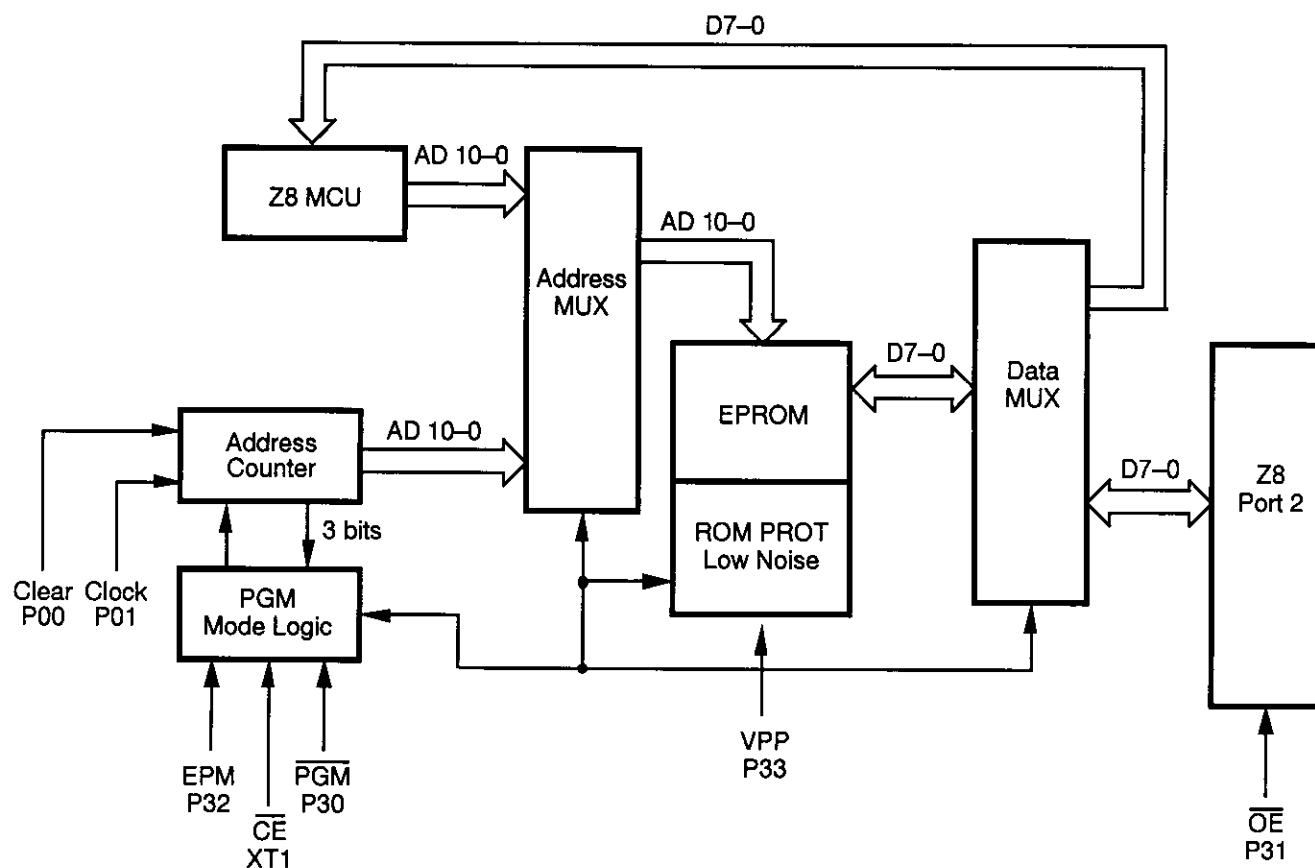## GENERAL DESCRIPTION (Continued)

Figure 2. EPROM Programming Mode Block Diagram

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).
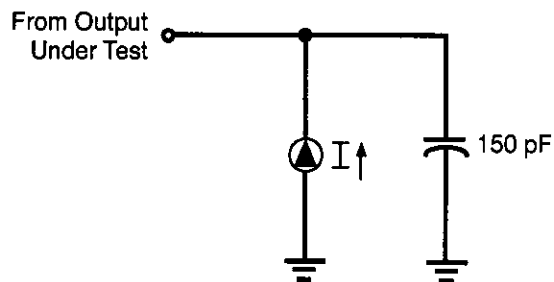

Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25°C$, $V_{CC} = GND = 0V$, $f = 1.0$ MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS
Extended Temperature

Sym	Parameter	V_{CC} [4]	$T_A = -40°C$ to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{INMAX}	Max Input Voltage	4.5V		12.0		V	$I_{IN} < 250 \mu A$	1
		5.5V		12.0		V	$I_{IN} < 250 \mu A$	1
V_{CH}	Clock Input High Voltage	4.5V	$0.8 V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
		5.5V	$0.8 V_{CC}$	$V_{CC}+0.3$	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.7	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.8	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.8	V		
V_{IL}	Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0$ mA	5
		4.5V	$V_{CC}-0.4$			V	Low Noise @ $I_{OH} = -0.5$ mA	
		5.5V	$V_{CC}-0.4$			V	Low Noise @ $I_{OH} = -0.5$ mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	$I_{OL} = +4.0$ mA	5
		5.5V		0.4	0.1	V	$I_{OL} = +4.0$ mA	5
		4.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
		5.5V		0.4	0.1	V	Low Noise @ $I_{OL} = 1.0$ mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	$I_{OL} = +12$ mA,	5
		5.5V		1.0	0.3	V	$I_{OL} = +12$ mA,	5
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
I_{OL}	Output Leakage	4.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V		-1.0	1.0	μA	$V_{IN} = 0V, V_{CC}$	
V_{ICR}	Comparator Input Common Mode Voltage Range		0	$V_{CC}-1.5$		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym	Parameter	V_{CC} [4]	$T_A = -40°C$ to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

AC ELECTRICAL CHARACTERISTICS
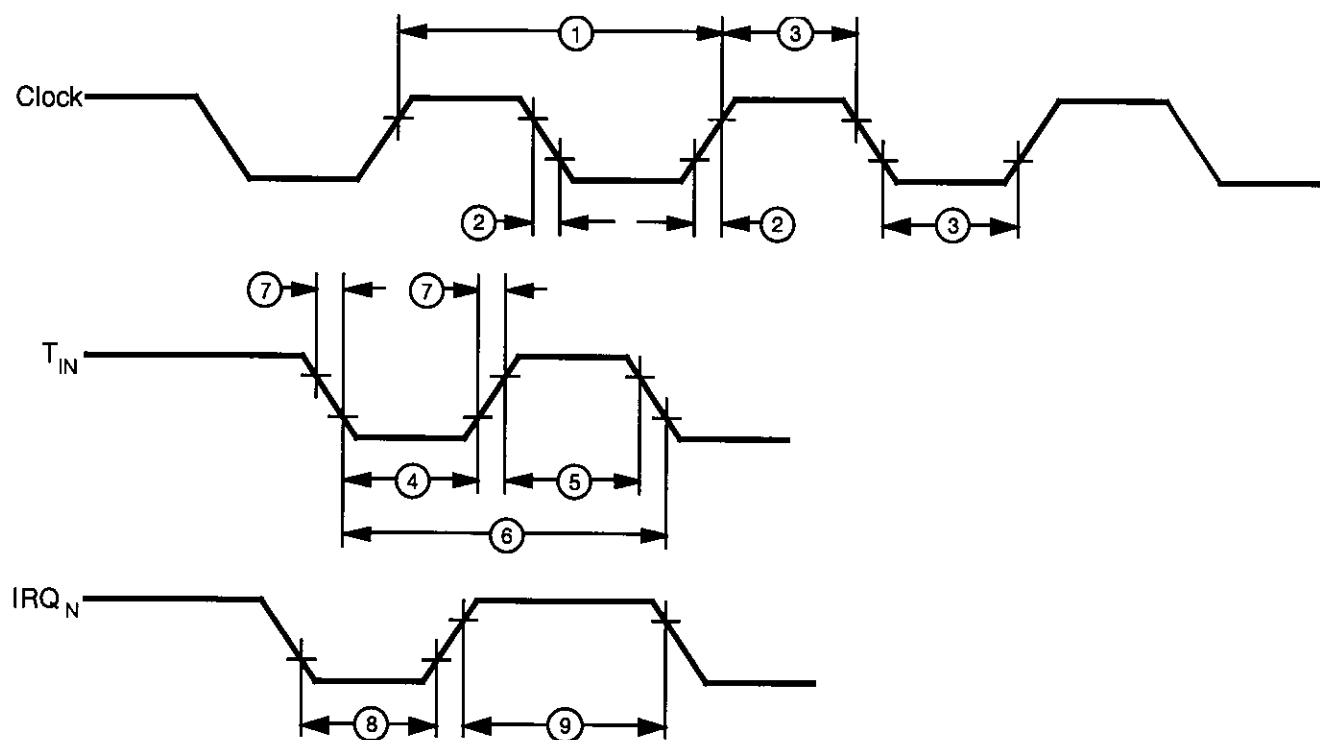
Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Standard Temperature

15				T_A= 0 °C to +70 °C					
				8 MHz		**12 MHz**			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	1
			5.5V	125	DC	83	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	4.5V		25		15	ns	1
			5.5V		25		15	ns	1
3	TwC	Input Clock Width	4.5V	62		41		ns	1
			5.5V	62		41		ns	1
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	4.5V		8TpC	8TpC			1
			5.5V		8TpC	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V		5TpC	5TpC			1,2
			5.5V		5TpC	5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1
11	Tpor	Power-On Reset Time	4.5V	20	80	20	80	ms	1
			5.5V	20	80	20	80	ms	1

Notes:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).
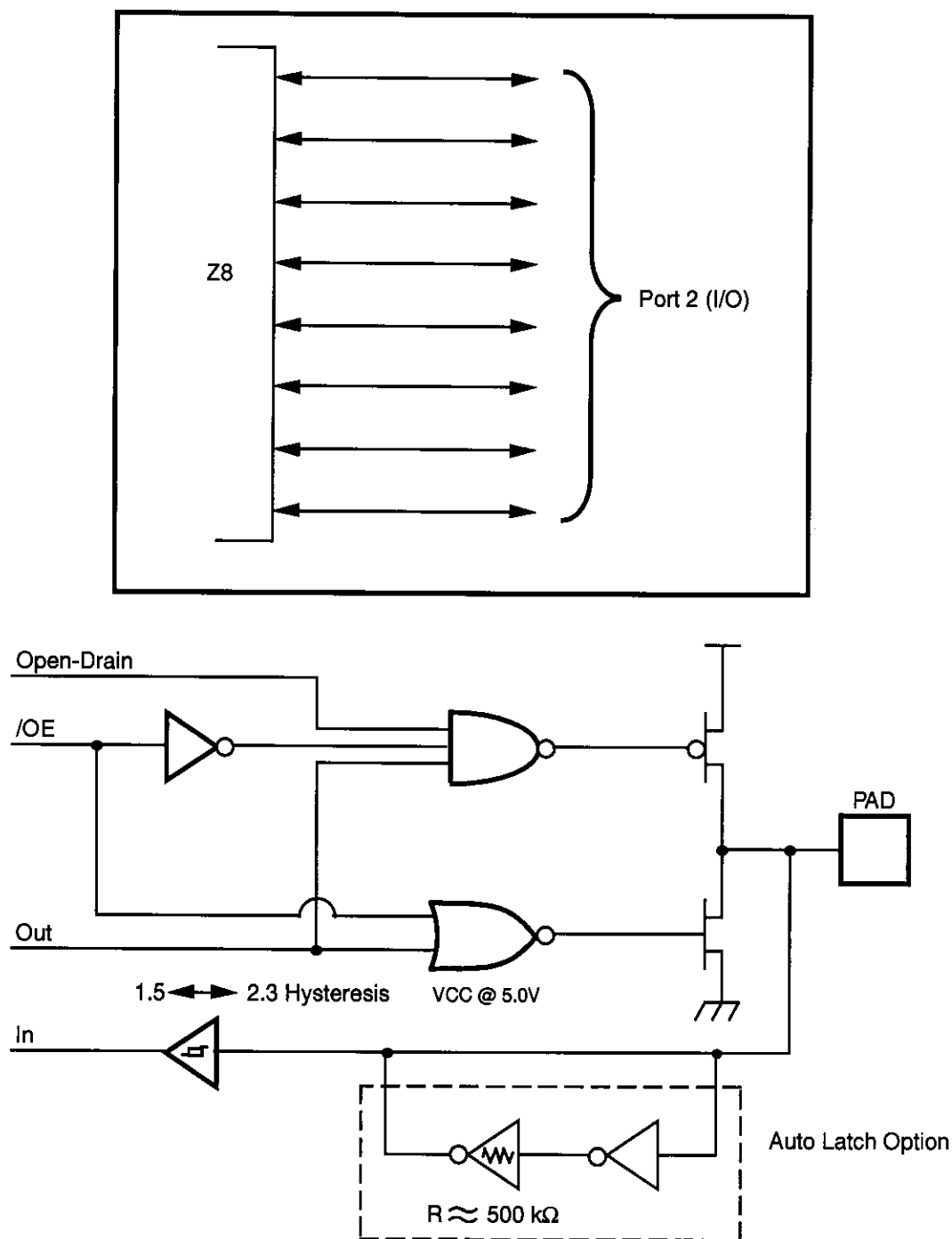

Figure 8. Port 2 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Notes:
F = Falling edge triggered
R = Rising edge triggered

Figure 15. Interrupt Block Diagram

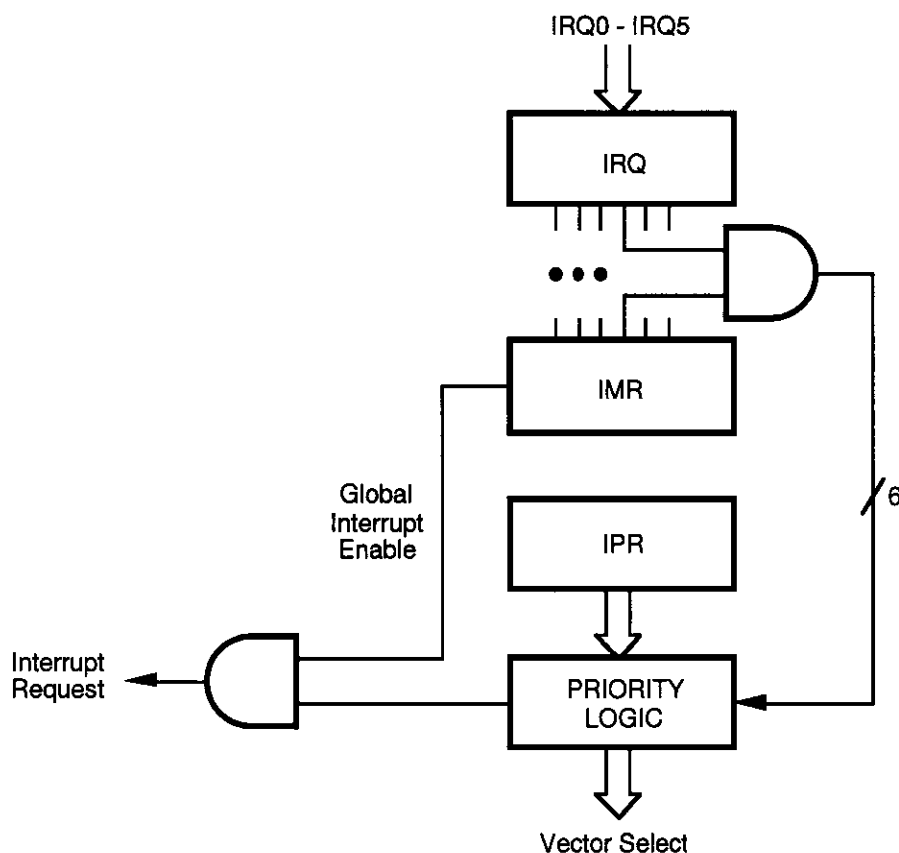**PRELIMINARY**

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.

Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC

External Clock

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz
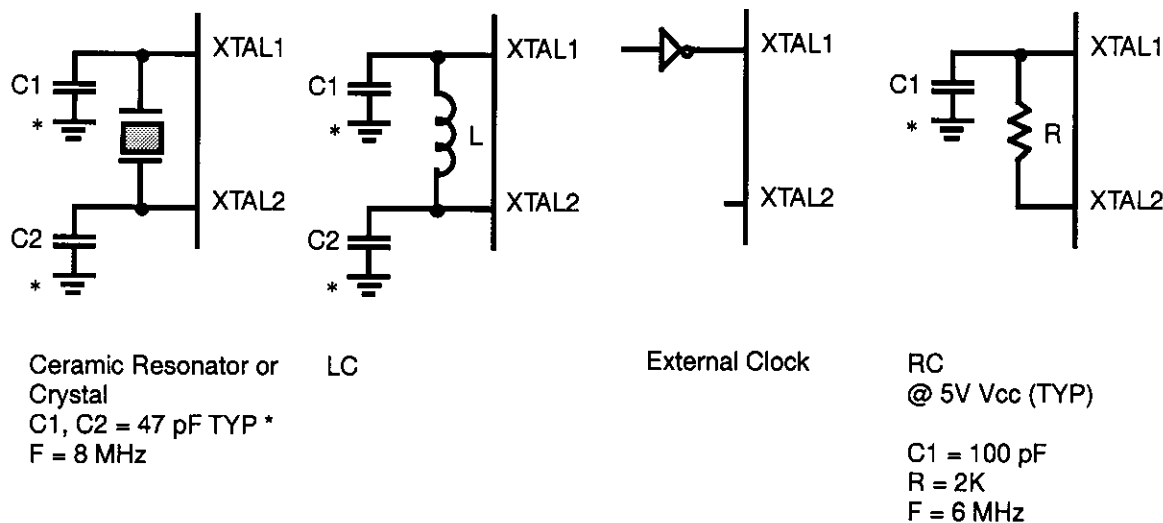
* Typical value including pin parasitics

Figure 16. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
V_{CC} = 5.0V @ 25°C

	Load Capacitor							
	33 pFd		56 pFd		100 pFd		0.00 1μFd	
Resistor (R)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	33K	31K	20K	20K	12K	11K	1.4K	1.4K
560K	56K	52K	34K	32K	20K	19K	2.5K	2.4K
220K	144K	130K	84K	78K	48K	45K	6K	6K
100K	315K	270K	182K	164K	100K	95K	12K	12K
56K	552K	480K	330K	300K	185K	170K	23K	22K
20K	1.4M	1M	884K	740K	500K	450K	65K	61K
10K	2.6M	2M	1.6M	1.3M	980K	820K	130K	123K
5K	4.4M	3M	2.8M	2M	1.7K	1.3M	245K	225K
2K	8M	5M	6M	4M	3.8K	2.7M	600K	536K
1K	12M	7M	8.8M	6M	6.3K	4.2M	1.0M	950K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
V_{CC} = 3.3V @ 25°C

	Load Capacitor							
Resistor (R)	33 pFd		56 pFd		100 pFd		0.00 1μFd	
	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)	A(Hz)	B(Hz)
1.0M	18K	18K	12K	12K	7.4K	7.7K	1K	1K
560K	30K	30K	20K	20K	12K	12K	1.6K	1.6K
220K	70K	70K	47K	47K	30K	30K	4K	4K
100K	150K	148K	97K	96K	60K	60K	8K	8K
56K	268K	250K	176K	170K	100K	100K	15K	15K
20K	690M	600K	463K	416K	286K	266K	40K	40K
10K	1.2M	1M	860K	730K	540K	480K	80K	76K
5K	2M	1.7M	1.5M	1.2M	950K	820K	151K	138K
2K	4.6M	3M	3.3M	2.4M	2.2M	1.6M	360K	316K
1K	7M	4.6M	5M	3.6M	3.6K	2.6M	660K	565K

Notes:
A = STD Mode Frequency.
B = Low EMI Mode Frequency.

FUNCTIONAL DESCRIPTION (Continued)

Internal Address Counter. The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

Programming Waveform. Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

Programming Algorithm. Figure 23 shows the flow chart of the Z8 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V_{PP} Setup	2		μs
4	V_{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		μs
8	$\overline{OE}$ Setup Time	2		μs
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	$\overline{PGM}$ Setup Time	2		μs
14	Address to $\overline{OE}$ Setup Time	2		μs
15	Option Program Pulse Width	78		ms
16	$\overline{OE}$ Width	250		ns
17	Address Valid to $\overline{OE}$ Low	125		ns

Figure 18. Z86E04/E08 Address Counter Waveform
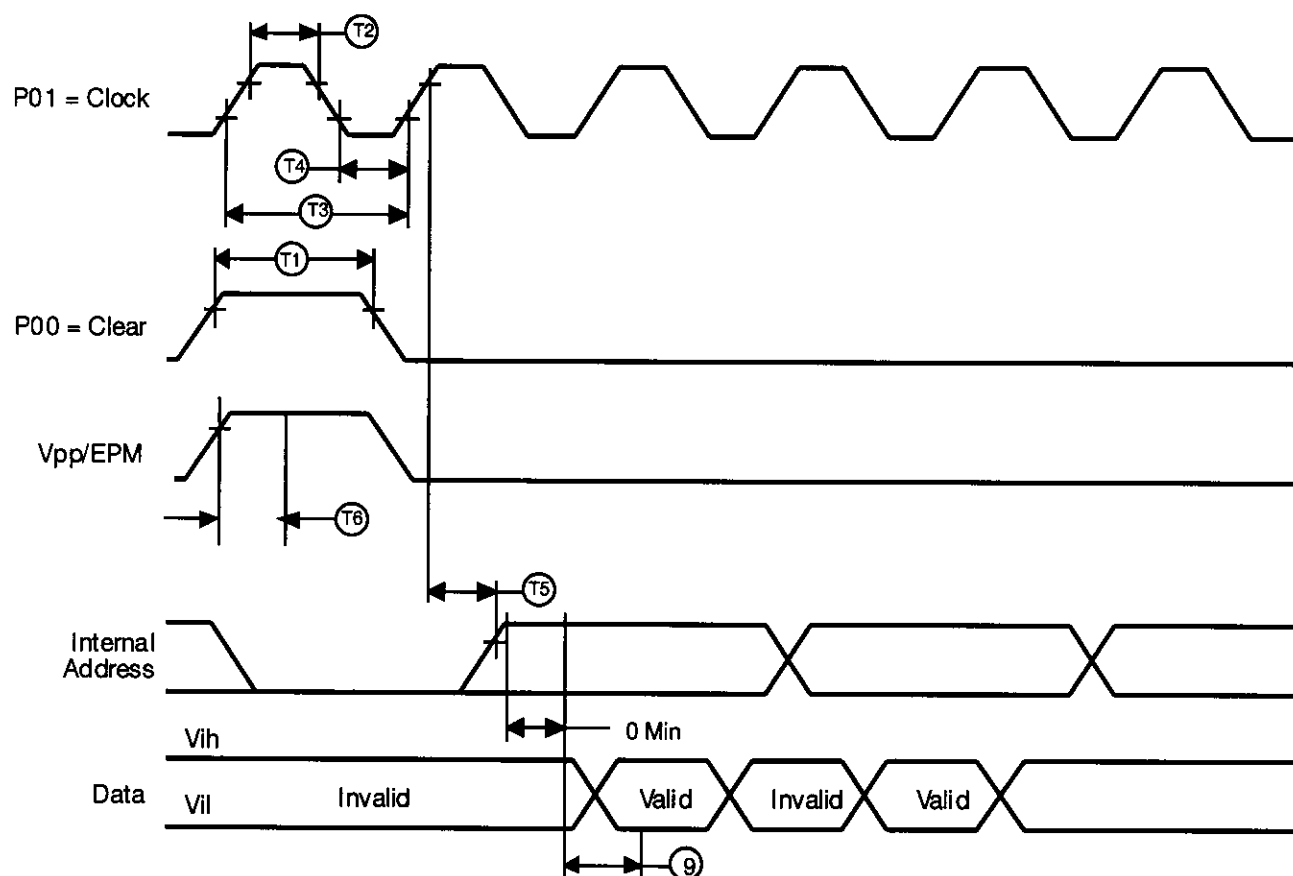
Legend:

T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 μs Min

FUNCTIONAL DESCRIPTION (Continued)
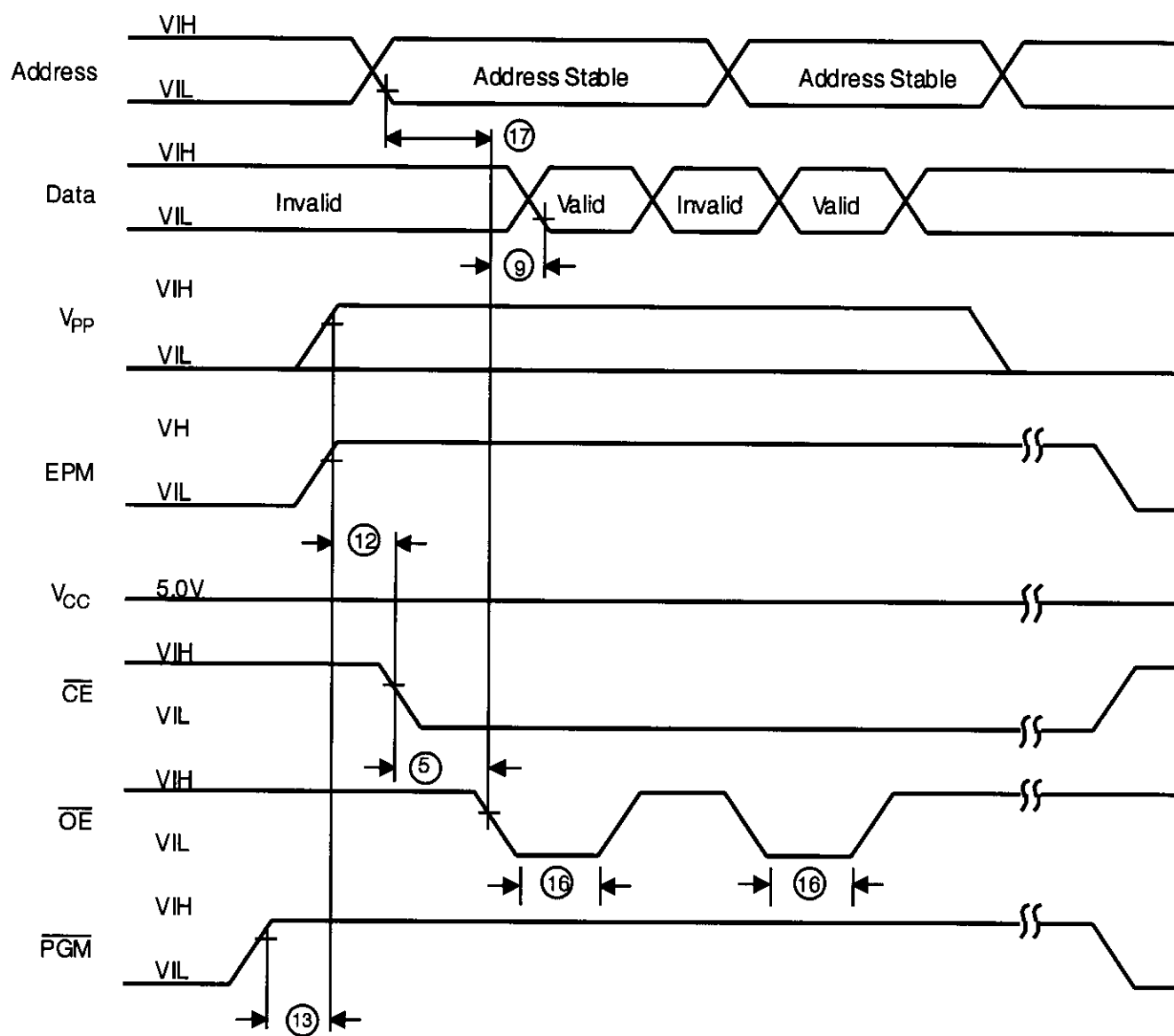
**Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)**
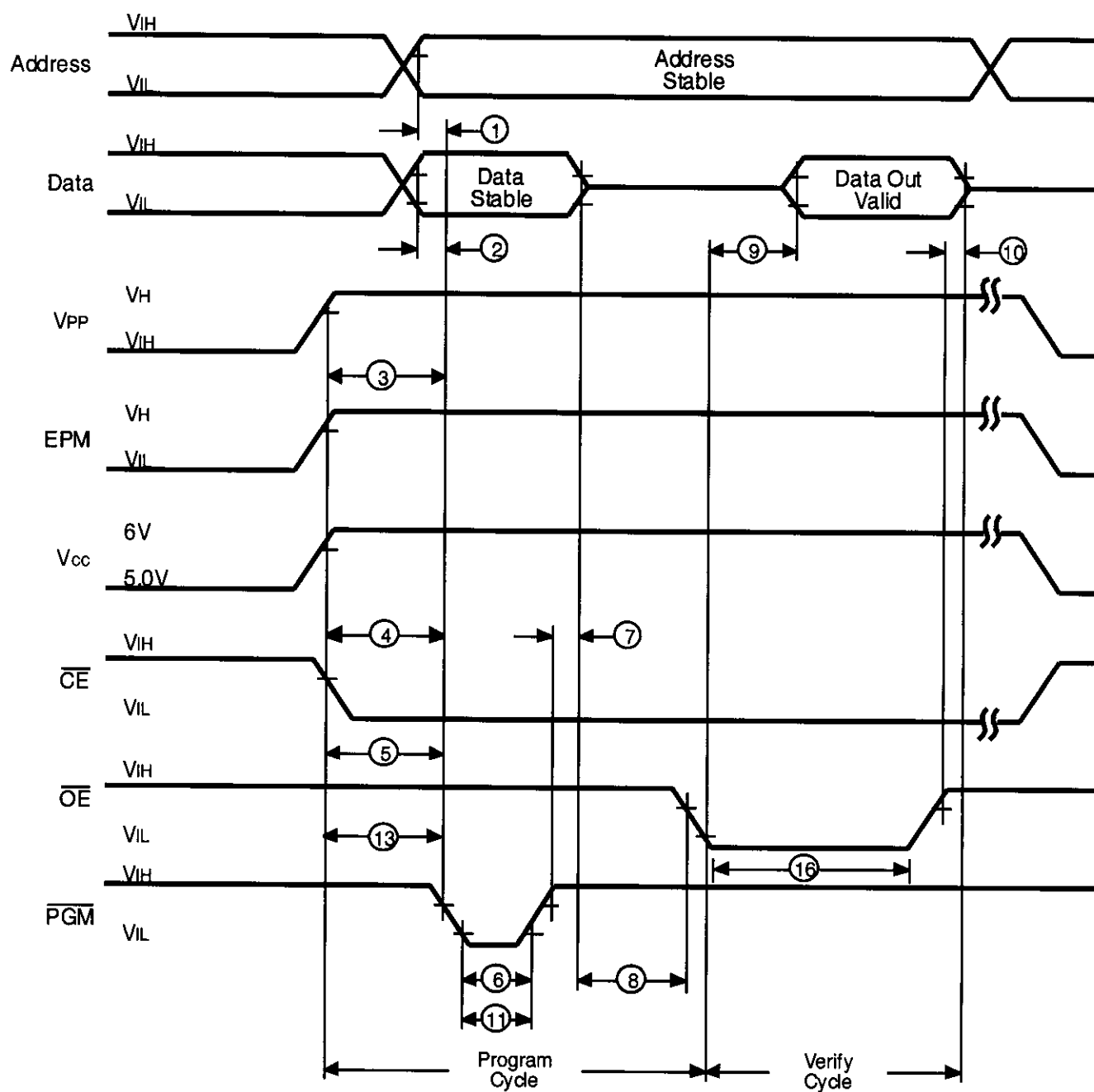
**Figure 20. Z86E04/E08 Programming Waveform
(Program and Verify)**
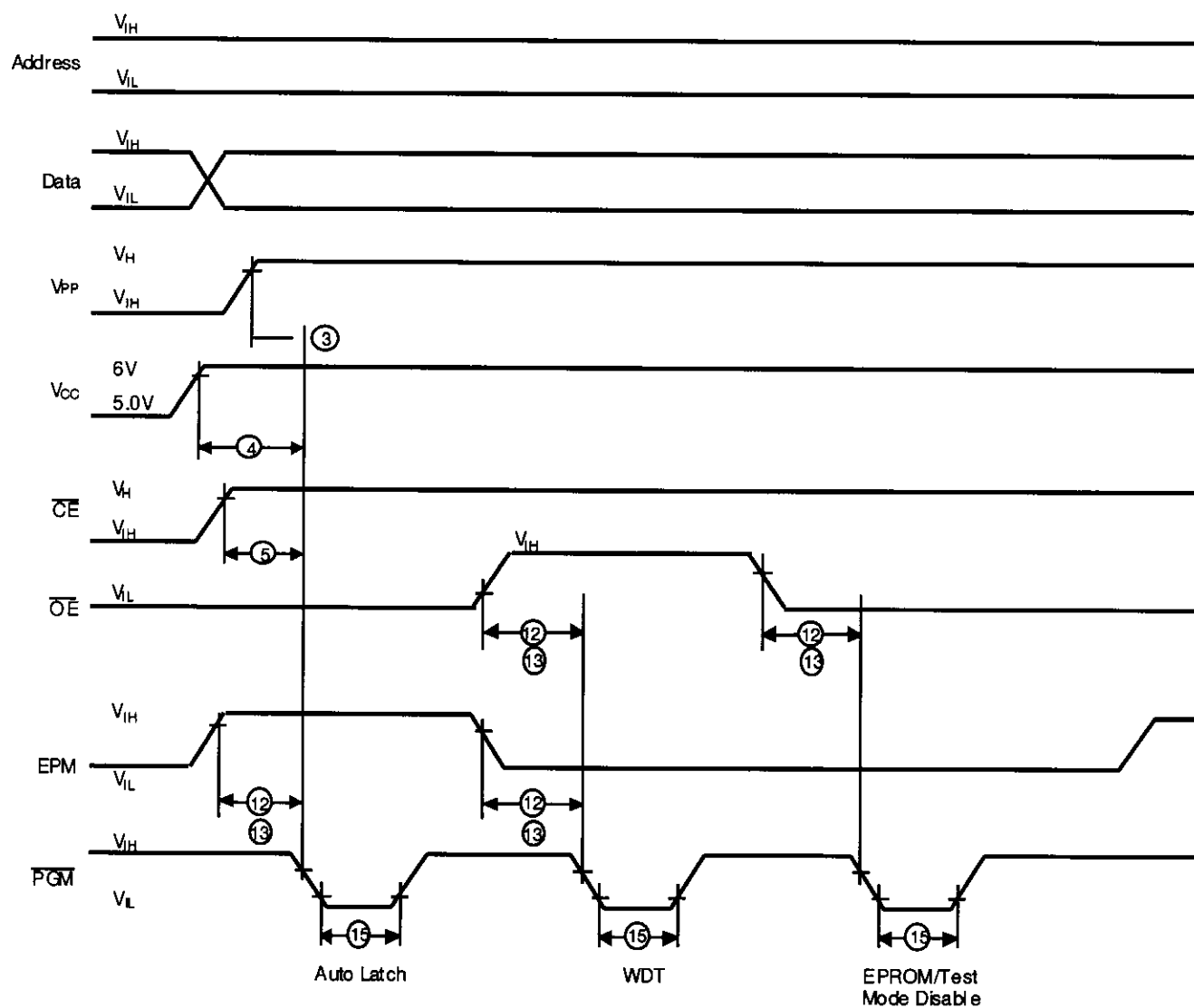
Figure 22. Z86E04/E08 Programming Options Waveform
(Auto Latch Disable, Permanent WDT Enable and
EPROM/Test Mode Disable)

FUNCTIONAL DESCRIPTION (Continued)
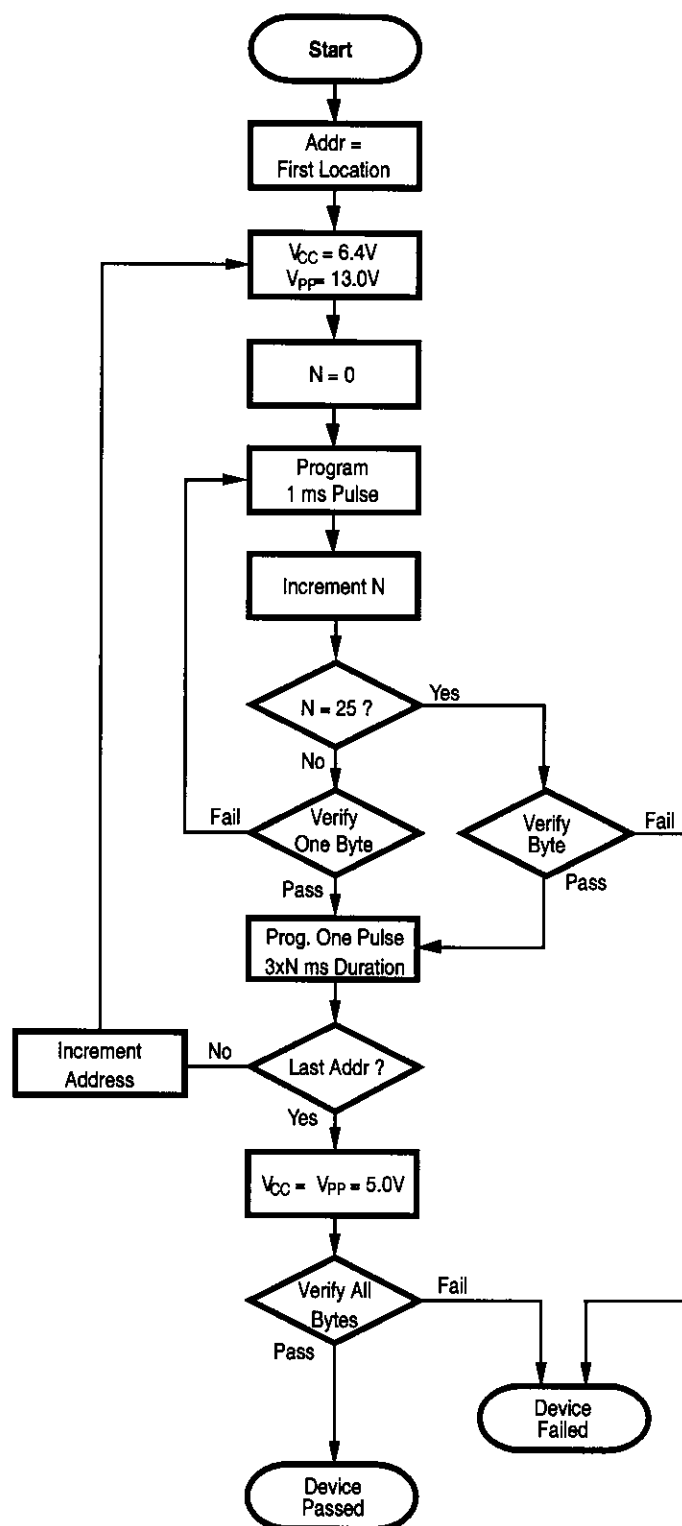
Figure 23. Z86E04/E08 Programming Algorithm

Z8 CONTROL REGISTERS

R241 TMR
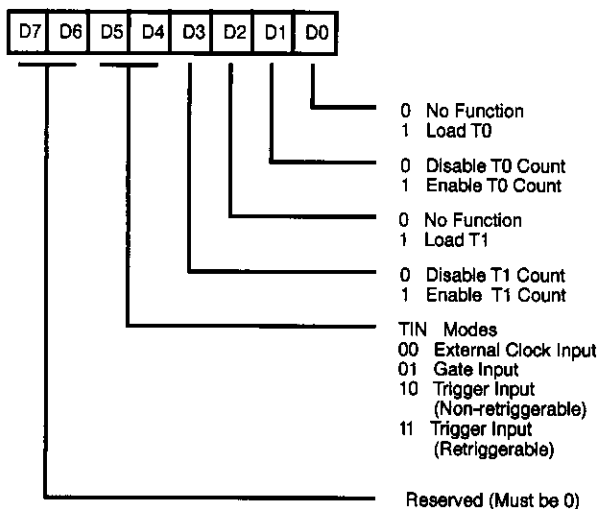
Figure 24. Timer Mode Register (F1$_H$: Read/Write)

R242 T1

T$_1$ Initial Value
(When Written)
(Range 1-256 Decimal
01-00 HEX)
T$_1$ Current Value
(When READ)
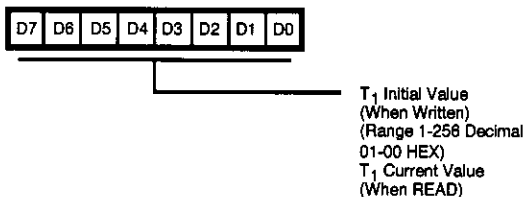
Figure 25. Counter Timer 1 Register (F2$_H$: Read/Write)

R243 PRE1

Count Mode
0 = T$_1$ Single Pass
1 = T$_1$ Modulo N

Clock Source
1 = T$_1$ Internal
0 = T$_1$ External Timing Input
(T$_{IN}$) Mode

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
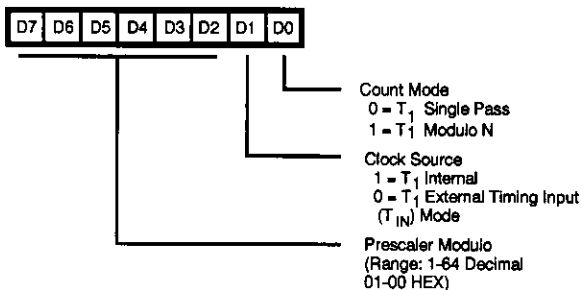
Figure 26. Prescaler 1 Register (F3$_H$: Write Only)

R244 T0

T$_0$ Initial Value
(When Written)
(Range: 1-256 Decimal
01-00 HEX)
T$_0$ Current Value
(When READ)
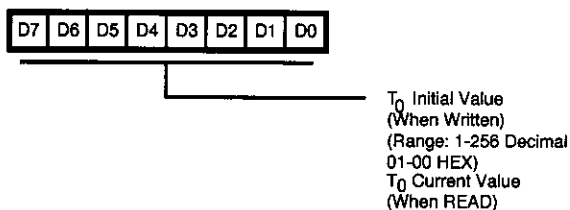
Figure 27. Counter/Timer 0 Register (F4$_H$: Read/Write)

R245 PRE0

Count Mode
0 T0 Single Pass
1 T0 Modulo N

Reserved (Must be 0)

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
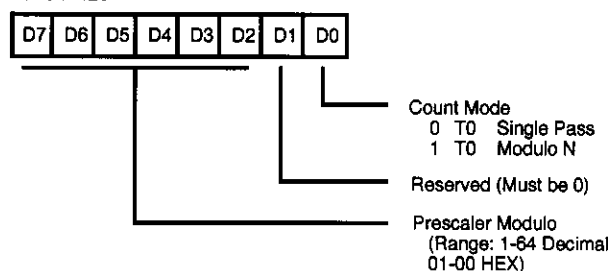
Figure 28. Prescaler 0 Register (F5$_H$: Write Only)

R246 P2M

P2$_7$ - P2$_0$ I/O Definition
0 Defines Bit as OUTPUT
1 Defines Bit as INPUT
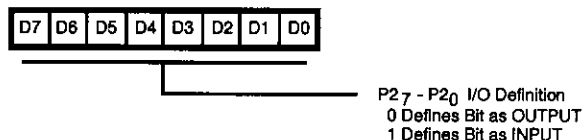
Figure 29. Port 2 Mode Register (F6$_H$: Write Only)

R247 P3M

0 Port 2 Open-Drain
1 Port 2 Push-pull

Port 3 Inputs
0 Digital Mode
1 Analog Mode

Reserved (Must be 0)
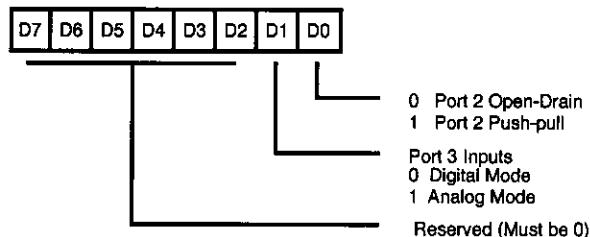
Figure 30. Port 3 Mode Register (F7$_H$: Write Only)

Z8 CONTROL REGISTERS (Continued)

R248 P01M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

P0$_2$-P0$_0$ Mode
00 = Output
01 = Input

Reserved (Must be 1.)

Reserved (Must be 0.)
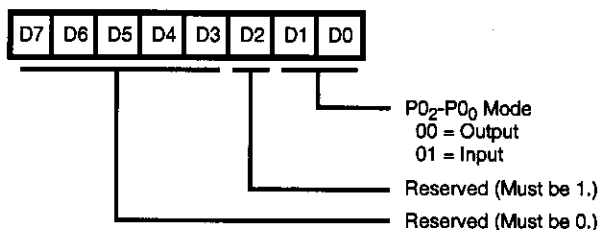
Figure 31. Port 0 and 1 Mode Register
(F8$_H$: Write Only)

R249 IPR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Interrupt Group Priority
Reserved = 000
C > A > B = 001
A > B > C = 010
A > C > B = 011
B > C > A = 100
C > B > A = 101
B > A > C = 110
Reserved = 111

IRQ1, IRQ4 Priority (Group C)
0 = IRQ1 > IRQ4
1 = IRQ4 > IRQ1

IRQ0, IRQ2 Priority (Group B)
0 = IRQ2 > IRQ0
1 = IRQ0 > IRQ2

IRQ3, IRQ5 Priority (Group A)
0 = IRQ5 > IRQ3
1 = IRQ3 > IRQ5

Reserved (Must be 0.)
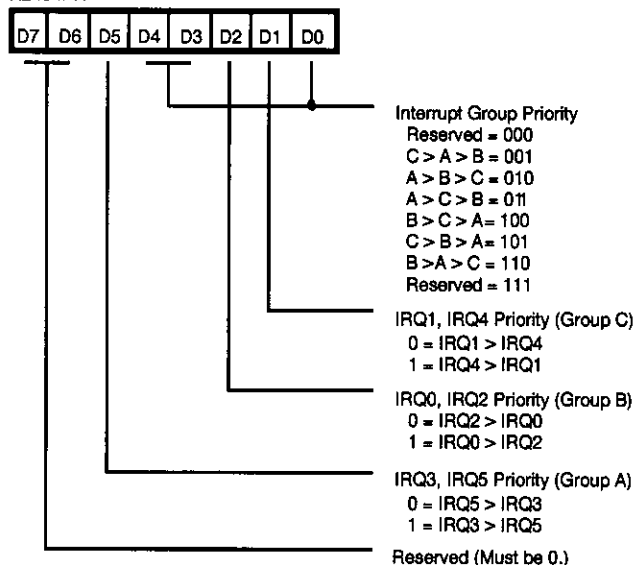
Figure 32. Interrupt Priority Register
(F9$_H$: Write Only)

R250 IRQ

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = P32 Input
IRQ4 = T0
IRQ5 = T1

Reserved (Must be 0)
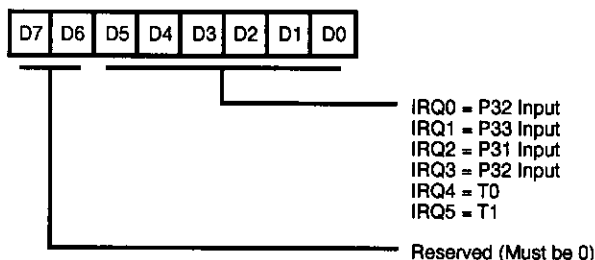
Figure 33. Interrupt Request Register
(FA$_H$: Read/Write)

R251 IMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1 Enables IRQ0-IRQ5
(D$_0$ = IRQ0)

Reserved (Must be 0.)

1 Enables Interrupts
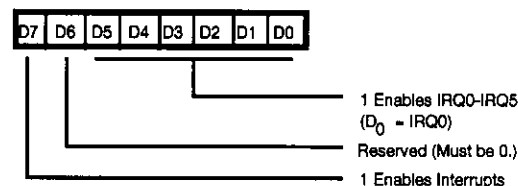
Figure 34. Interrupt Mask Register
(FB$_H$: Read/Write)

R252 Flags

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

User Flag F1

User Flag F2

Half Carry Flag

Decimal Adjust Flag

Overflow Flag

Sign Flag

Zero Flag

Carry Flag
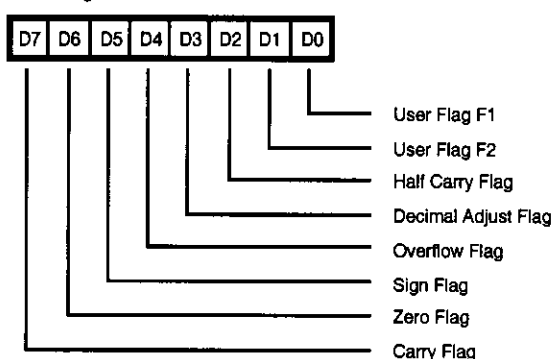
Figure 35. Flag Register
(FC$_H$: Read/Write)

R253 RP

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Expanded Register File

Working Register Pointer

Default After Reset = 00H
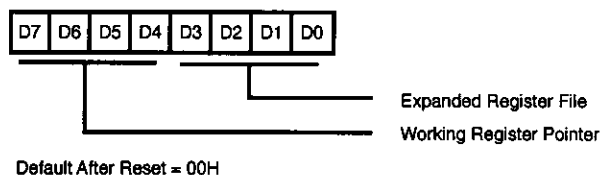
Figure 36. Register Pointer
(FD$_H$: Read/Write)

R255 SPL

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stack Pointer Lower
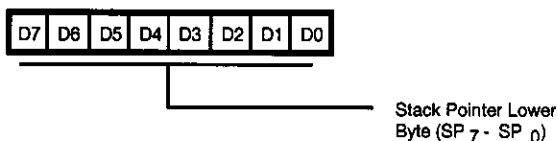Byte (SP$_7$ - SP$_0$)

Figure 37. Stack Pointer
(FF$_H$: Read/Write)

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.