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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z86e0812ssc1866tr">https://www.e-xfl.com/product-detail/zilog/z86e0812ssc1866tr</a>

## FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1 $\mu$ s @ 12 MHz)
- RAM Bytes (125)

## GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8<sup>®</sup> MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

**Note:** All Signals with an overline, " $\overline{\phantom{x}}$ ", are active Low, for example:  $\overline{B/W}$  (WORD is active Low);  $\overline{B}/W$  (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

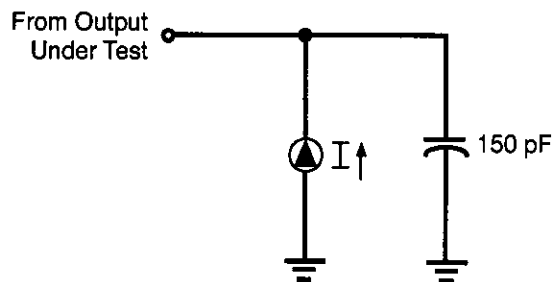


Figure 5. Test Load Diagram

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

## DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V <sub>CC</sub> [4]	T <sub>A</sub> = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
I <sub>CC1</sub>	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 4 MHz	7
I <sub>CC2</sub>	Standby Current	4.5V		10.0	1.0	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	7,8
		5.5V		10.0	1.0	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	7,8
I <sub>ALL</sub>	Auto Latch Low Current	4.5V		32.0	16	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
		5.5V		32.0	16	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
I <sub>ALH</sub>	Auto Latch High Current	4.5V		-16.0	-8.0	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	
		5.5V		-16.0	-8.0	μA	0V < V <sub>IN</sub> < V <sub>CC</sub>	

## Notes:

- Port 2 and Port 0 only
- V<sub>SS</sub> = 0V = GND
- The device operates down to V<sub>LV</sub> of the specified frequency for V<sub>LV</sub>. The minimum operational V<sub>CC</sub> is determined on the value of the voltage V<sub>LV</sub> at the ambient temperature. The V<sub>LV</sub> increases as the temperature decreases.
- V<sub>CC</sub> = 4.5 to 5.5V, typical values measured at V<sub>CC</sub> = 5.0V.  
The V<sub>CC</sub> voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V<sub>CC</sub> = 5.0V.
- Standard Mode (not Low EMI Mode)
- Z86E08 only
- All outputs unloaded and all inputs are at V<sub>CC</sub> or V<sub>SS</sub> level.
- If analog comparator is selected, then the comparator inputs must be at V<sub>CC</sub> level.

## AC ELECTRICAL CHARACTERISTICS

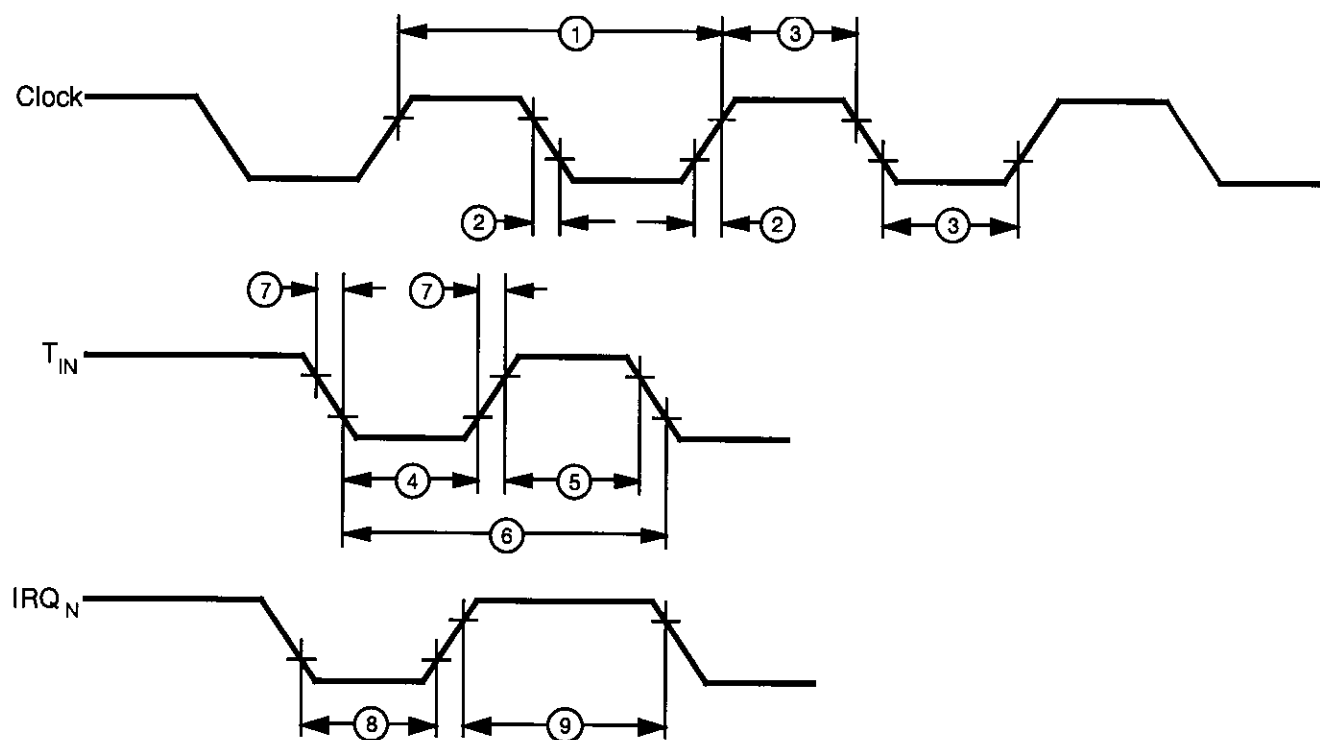


Figure 6. AC Electrical Timing Diagram

**AC ELECTRICAL CHARACTERISTICS**

Low Noise Mode, Standard Temperature

No	Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0 °C to +70 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

**Notes:**

1. Timing Reference uses 0.7 V<sub>CC</sub> for a logic 1 and 0.2 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

## LOW NOISE VERSION

### Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

## PIN FUNCTIONS

### OTP Programming Mode

**D7–D0 Data Bus.** Data can be read from, or written to, the EPROM through this data bus.

**V<sub>CC</sub> Power Supply.** It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

**$\overline{CE}$  Chip Enable** (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

**$\overline{OE}$  Output Enable** (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

**EPM EPROM Program Mode.** This pin controls the different EPROM Program Modes by applying different voltages.

**V<sub>PP</sub> Program Voltage.** This pin supplies the program voltage.

**Clear Clear** (active High). This pin resets the internal address counter at the High Level.

**Clock Address Clock.** This pin is a clock input. The internal address counter increases by one with one clock cycle.

**PGM Program Mode** (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

### Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V<sub>CC</sub> occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V<sub>PP</sub>,  $\overline{CE}$ , EPM,  $\overline{OE}$  pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V<sub>CC</sub>.
- Adding a capacitor to the affected pin.

**Note:** Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

**Port 2, P27–P20.** Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software

control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

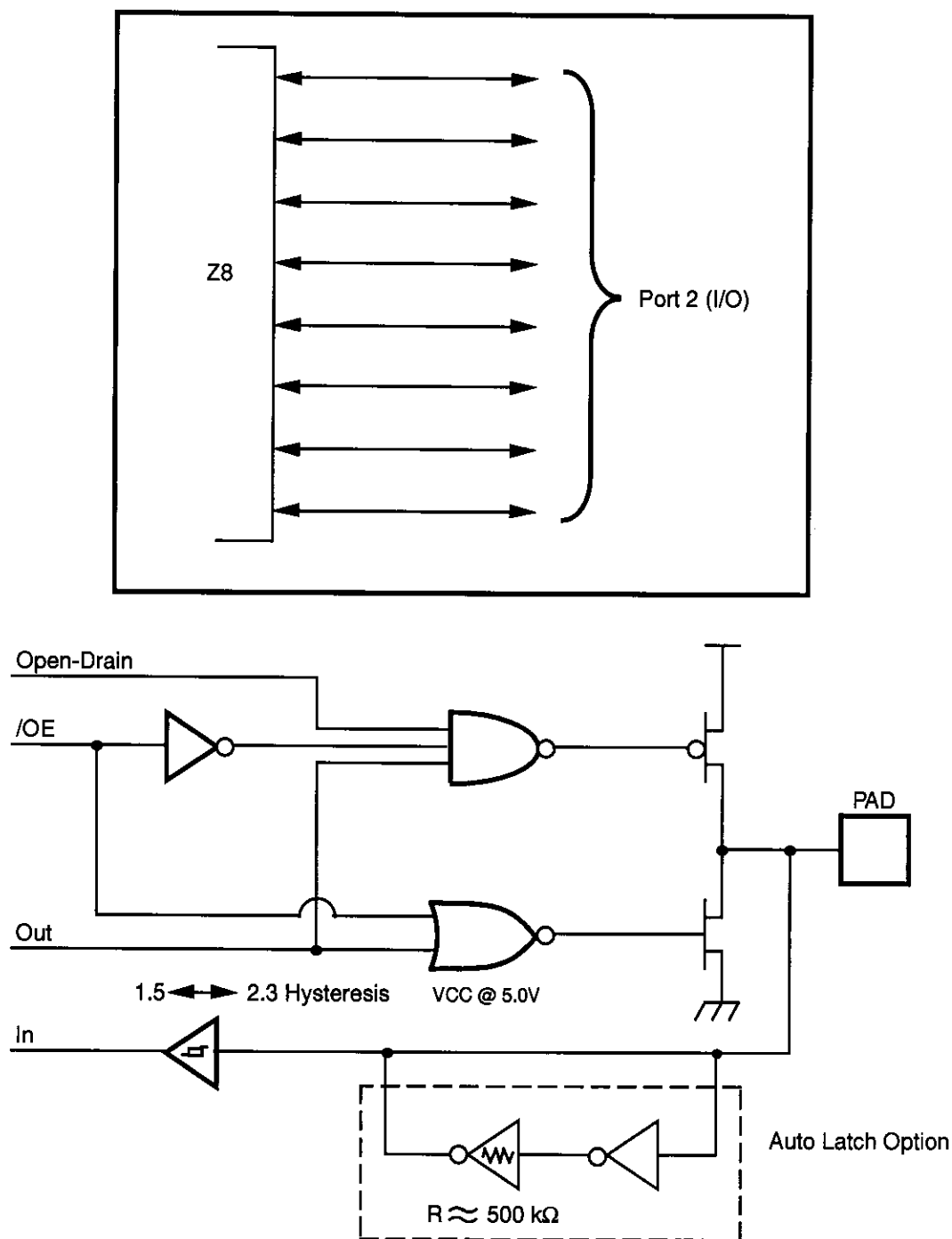


Figure 8. Port 2 Configuration



**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the  $V_{CC}$  is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or  $T_{IN}$  through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

**RESET.** This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for  $T_{POR}$  ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.

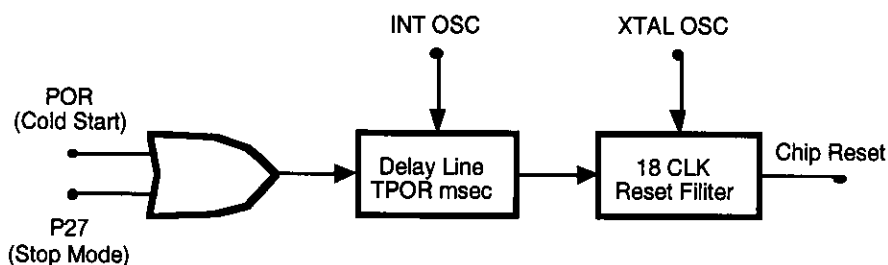


Figure 10. Internal Reset Configuration

**Power-On Reset (POR).** A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows  $V_{CC}$  and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

**Watch-Dog Timer Reset.** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

**Program Memory.** The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

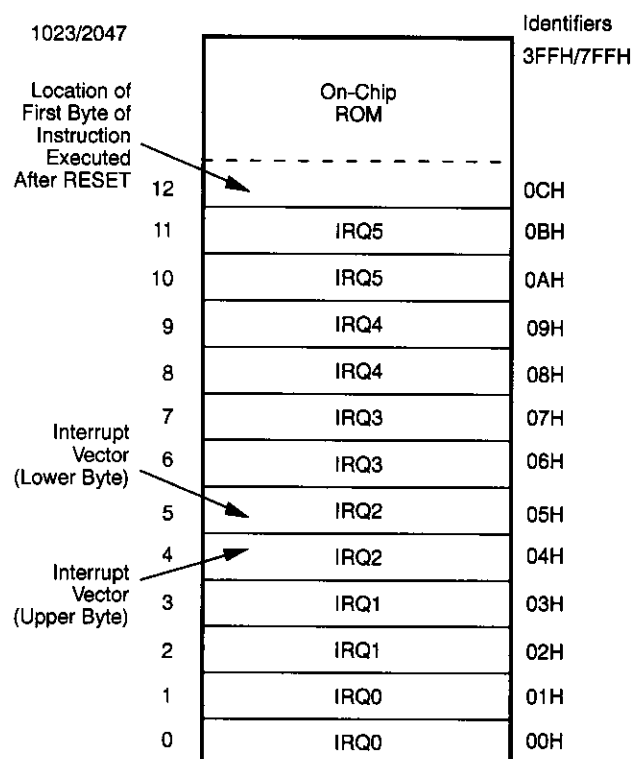


Figure 11. Program Memory Map

**Register File.** The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

Location	Identifiers
255 (FFH)	Stack Pointer (Bits 7-0) SPL
254 (FE)	General-Purpose Register GPR
253 (FD)	Register Pointer RP
252 (FC)	Program Control Flags FLAGS
251 (FB)	Interrupt Mask Register IMR
250 (FA)	Interrupt Request Register IRQ
249 (F9)	Interrupt Priority Register IPR
248 (F8)	Ports 0-1 Mode P01M
247 (F7)	Port 3 Mode P3M
246 (F6)	Port 2 Mode P2M
245 (F5)	T0 Prescaler PRE0
244 (F4)	Timer/Counter 0 T0
243 (F3)	T1 Prescaler PRE1
242 (F2)	Timer/Counter 1 T1
241 (F1H)	Timer Mode TMR
128	Not Implemented
127 (7FH)	General-Purpose Registers
4	
3	Port 3 P3
2	Port 2 P2
1	Reserved P1
0 (00H)	Port 0 P0

Figure 12. Register File

## FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

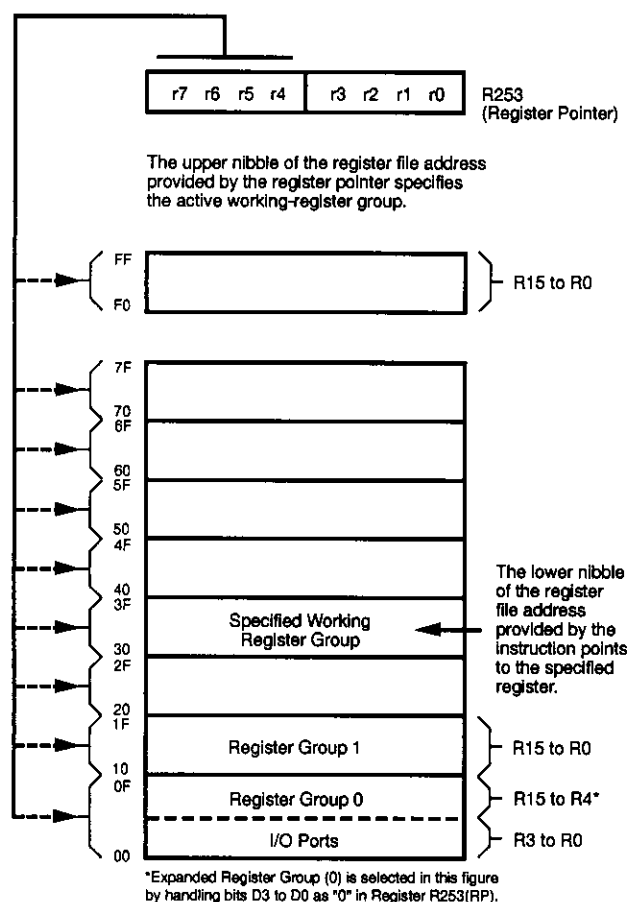


Figure 13. Register Pointer

**Stack Pointer.** The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

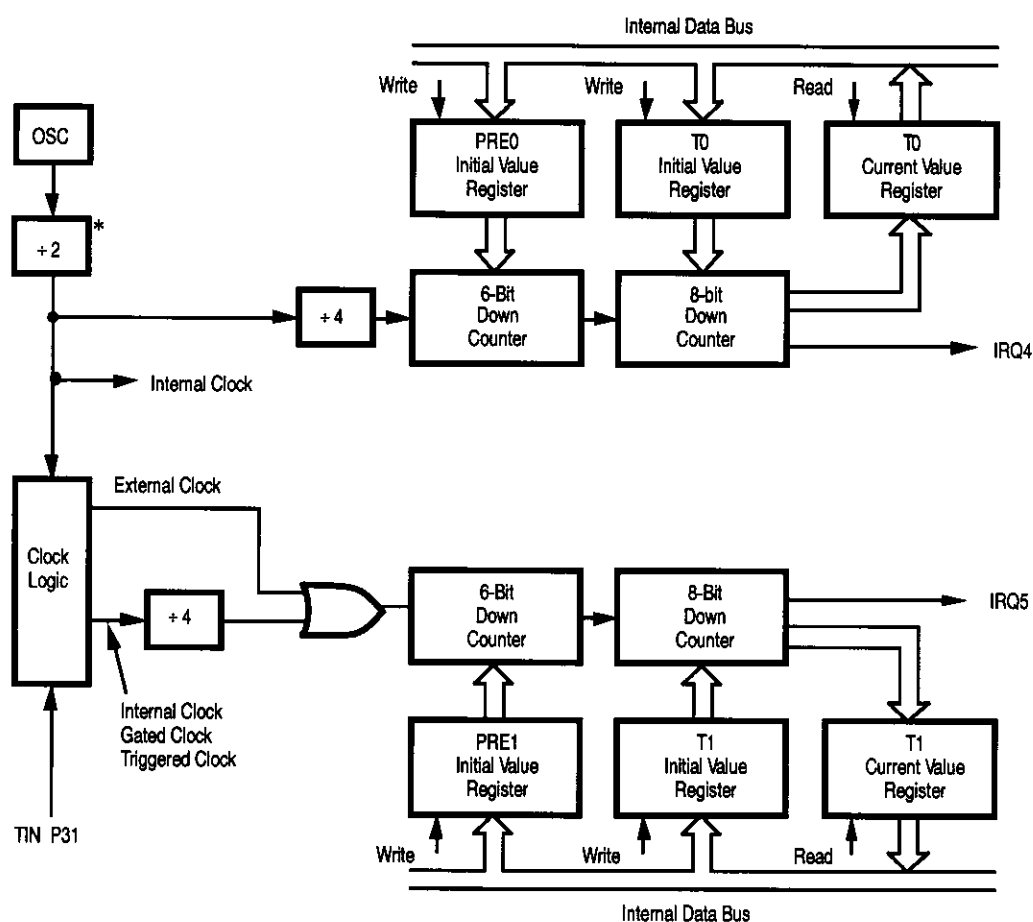
**General-Purpose Registers (GPR).** These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the  $V_{CC}$  voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

**Counter/Timer.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.



\* **Note:** By passed, if Low EMI Mode is selected.

Figure 14. Counter/Timers Block Diagram

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

**Note:** User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

**Notes:**

F = Falling edge triggered

R = Rising edge triggered

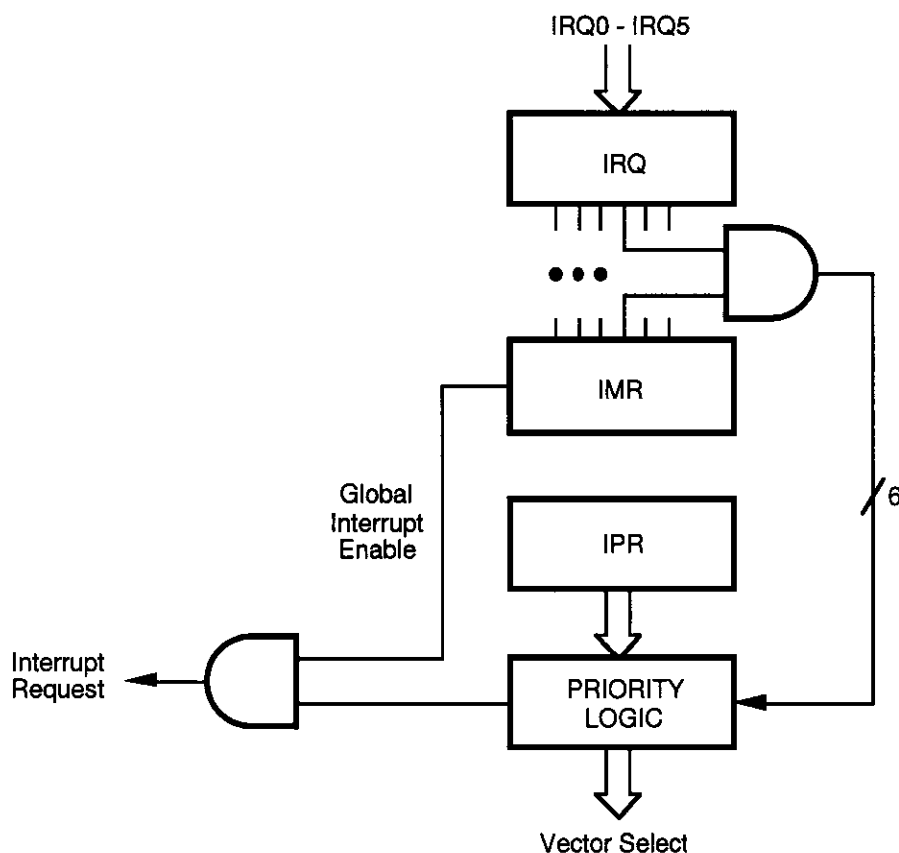
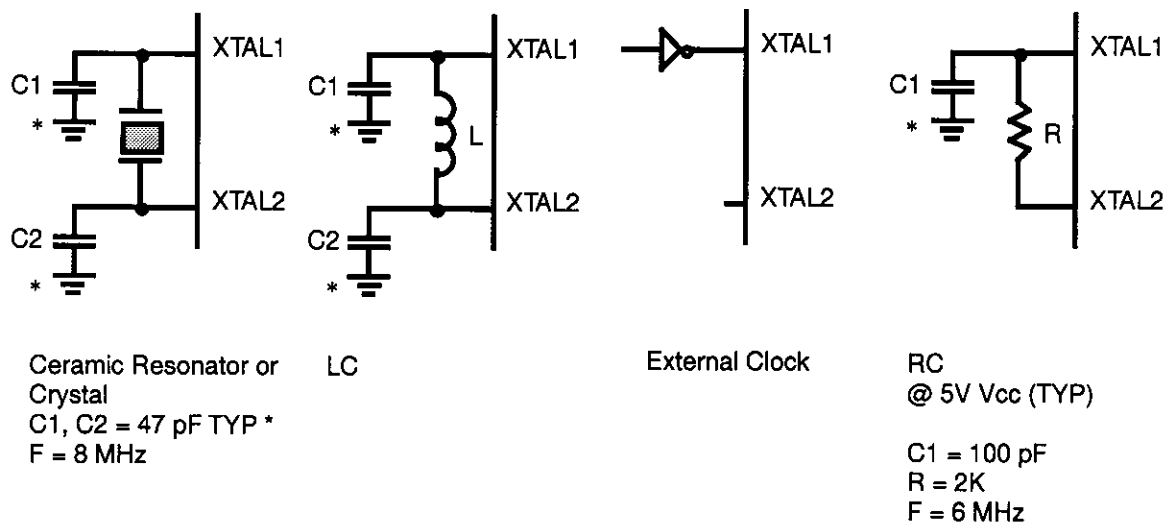


Figure 15. Interrupt Block Diagram

**Clock.** The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V<sub>SS</sub>, Pin 14 to reduce Ground noise injection.



\* Typical value including pin parasitics

**Figure 16. Oscillator Configuration**

**HALT Mode.** This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

**Note:** On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

**STOP Mode.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10  $\mu$ A. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

**Note:** A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

**Watch-Dog Timer (WDT).** The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

**Opcode WDT (5FH).** The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every  $T_{WDT}$ ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of  $T_{POR}$ , plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

**Opcode WDH (4FH).** When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

**Permanent WDT.** Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

**Auto Reset Voltage ( $V_{LV}$ ).** The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the  $V_{CC}$  below  $V_{LV}$ .

Figure 17 shows the Auto Reset Voltage versus temperature. If the  $V_{CC}$  drops below the VCC operating voltage range, the Z8 will function down to the  $V_{LV}$  unless the internal clock frequency is higher than the specified maximum  $V_{LV}$  frequency.

**FUNCTIONAL DESCRIPTION (Continued)**

**Internal Address Counter.** The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

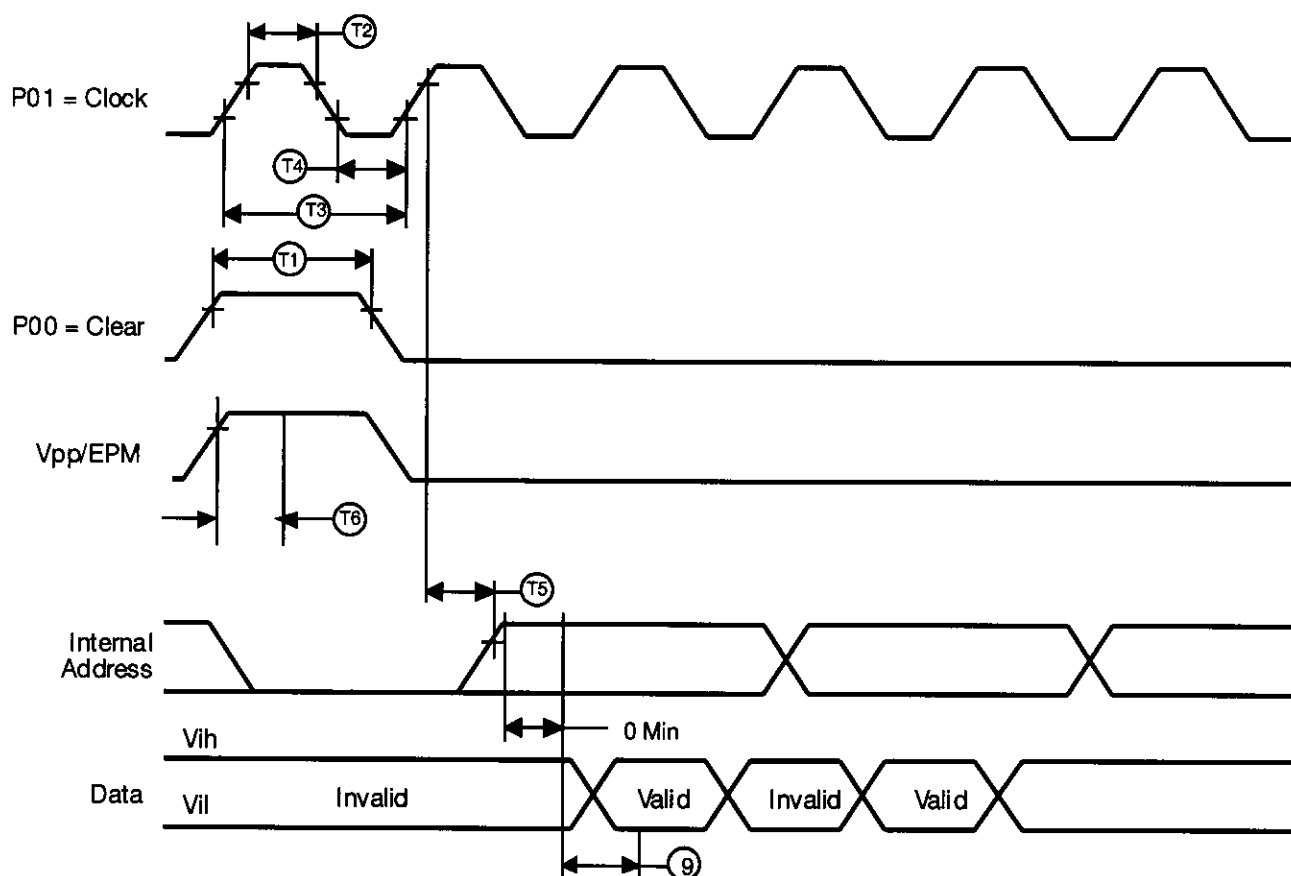
**Programming Waveform.** Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 23 shows the flow chart of the Z8 programming algorithm.

**Table 8. Timing of Programming Waveforms**

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		$\mu$ s
2	Data Setup Time	2		$\mu$ s
3	V <sub>pp</sub> Setup	2		$\mu$ s
4	V <sub>cc</sub> Setup Time	2		$\mu$ s
5	Chip Enable Setup Time	2		$\mu$ s
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		$\mu$ s
8	OE Setup Time	2		$\mu$ s
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		$\mu$ s
13	PGM Setup Time	2		$\mu$ s
14	Address to OE Setup Time	2		$\mu$ s
15	Option Program Pulse Width	78		ms
16	OE Width	250		ns
17	Address Valid to OE Low	125		ns





Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 $\mu$ s Min

Figure 18. Z86E04/E08 Address Counter Waveform

# FUNCTIONAL DESCRIPTION (Continued)

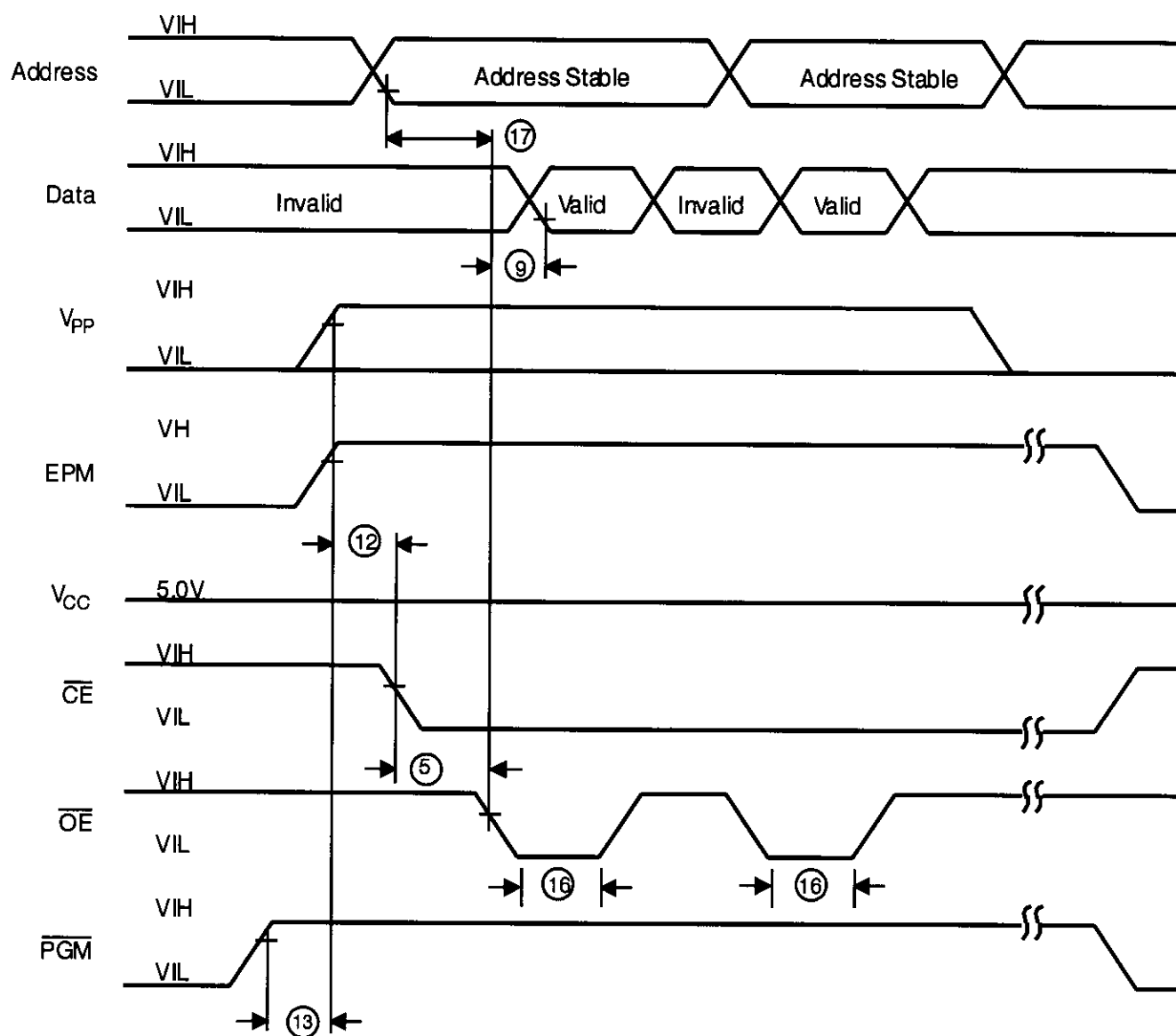


Figure 19. Z86E04/E08 Programming Waveform  
(EPROM Read)

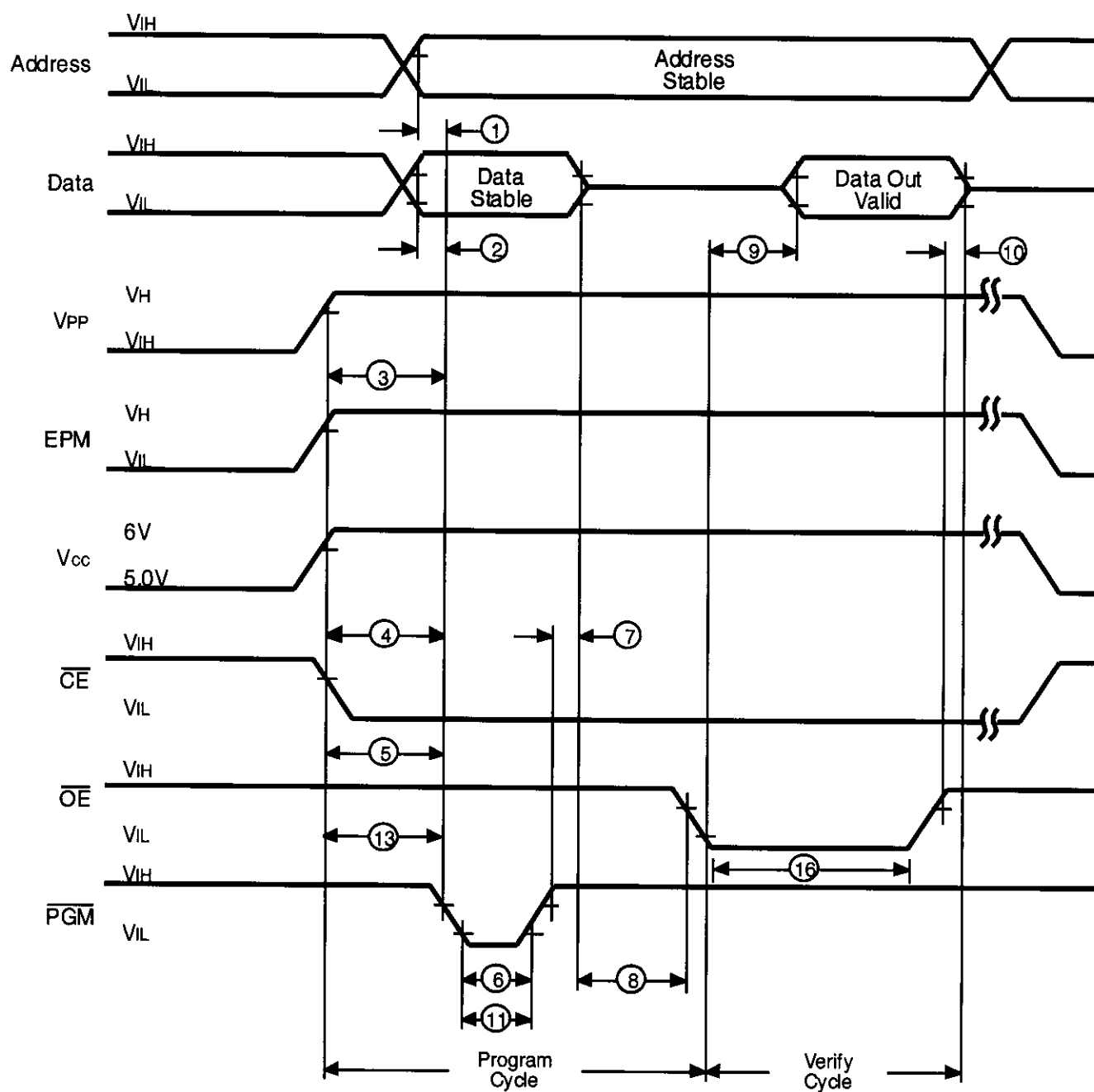


Figure 20. Z86E04/E08 Programming Waveform  
(Program and Verify)

# FUNCTIONAL DESCRIPTION (Continued)

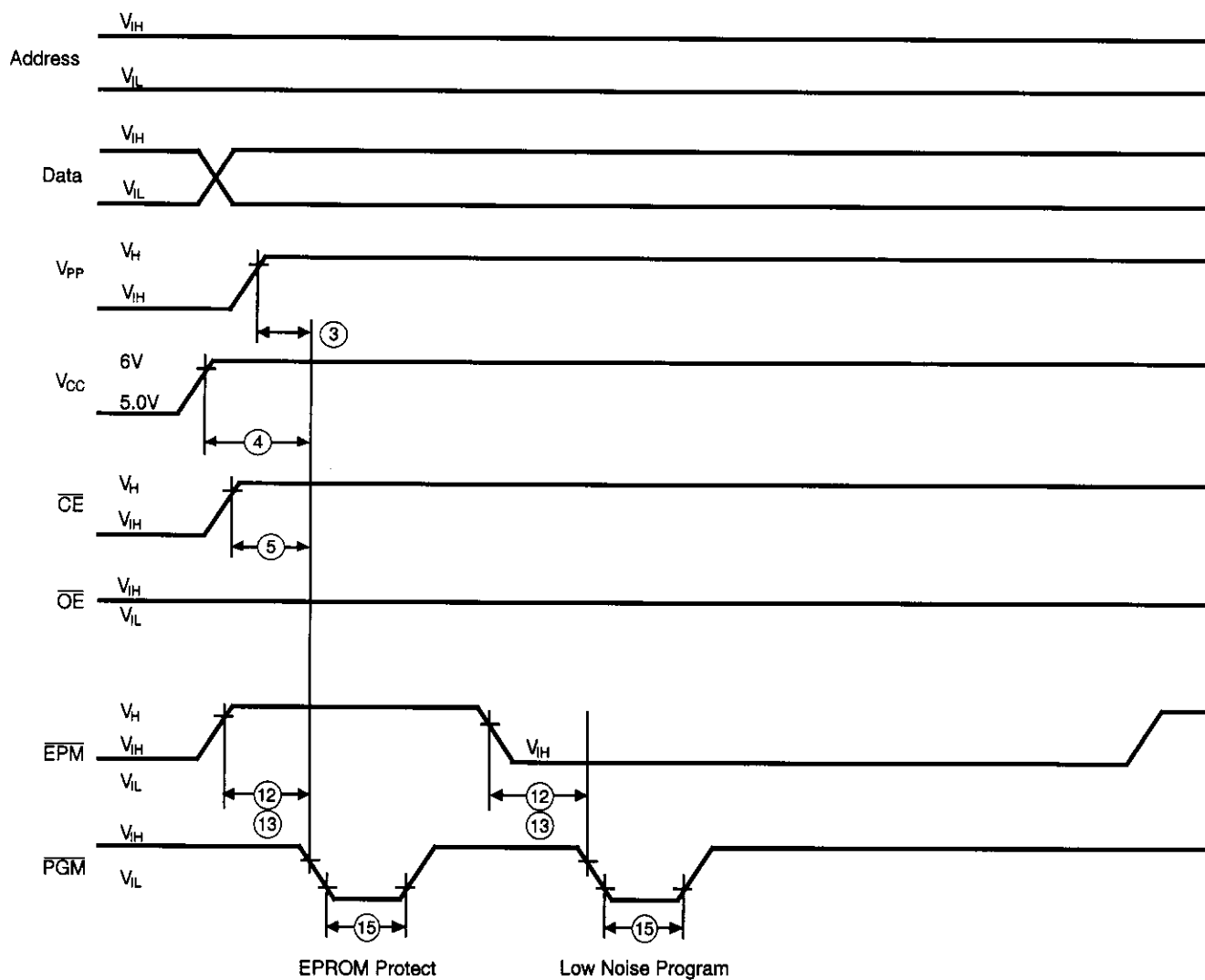
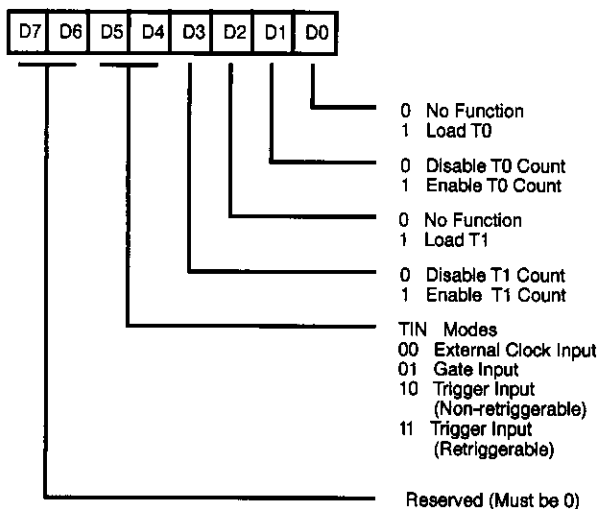


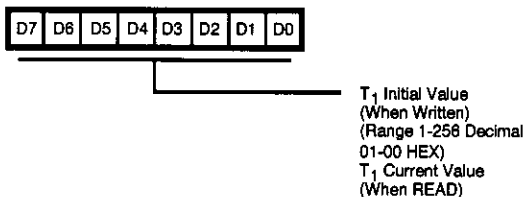
Figure 21. Z86E04/E08 Programming Options Waveform  
(EPROM Protect and Low Noise Program)

## Z8 CONTROL REGISTERS

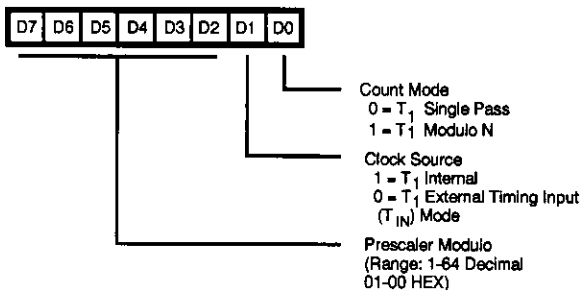
R241 TMR

Figure 24. Timer Mode Register (F1<sub>H</sub>: Read/Write)

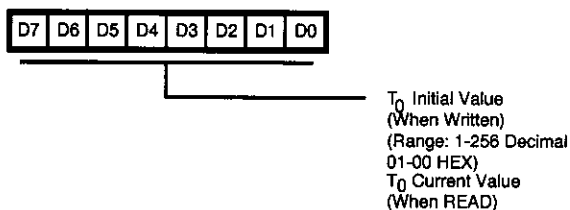
R242 T1

Figure 25. Counter Timer 1 Register (F2<sub>H</sub>: Read/Write)

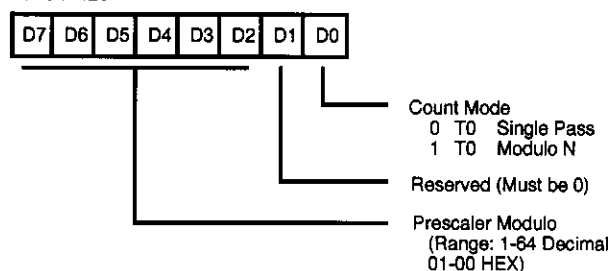
R243 PRE1

Figure 26. Prescaler 1 Register (F3<sub>H</sub>: Write Only)

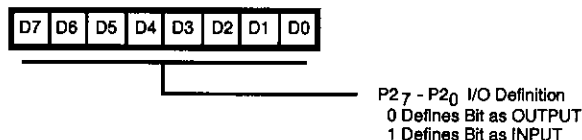
R244 T0

Figure 27. Counter/Timer 0 Register (F4<sub>H</sub>: Read/Write)

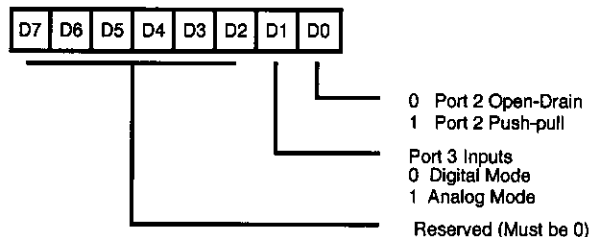
R245 PRE0

Figure 28. Prescaler 0 Register (F5<sub>H</sub>: Write Only)

R246 P2M

Figure 29. Port 2 Mode Register (F6<sub>H</sub>: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7<sub>H</sub>: Write Only)