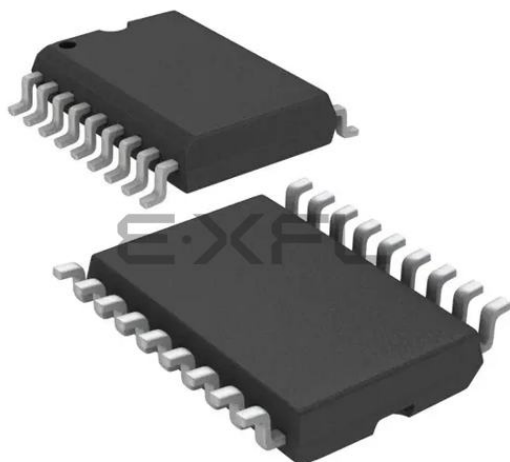




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812ssc1903tr

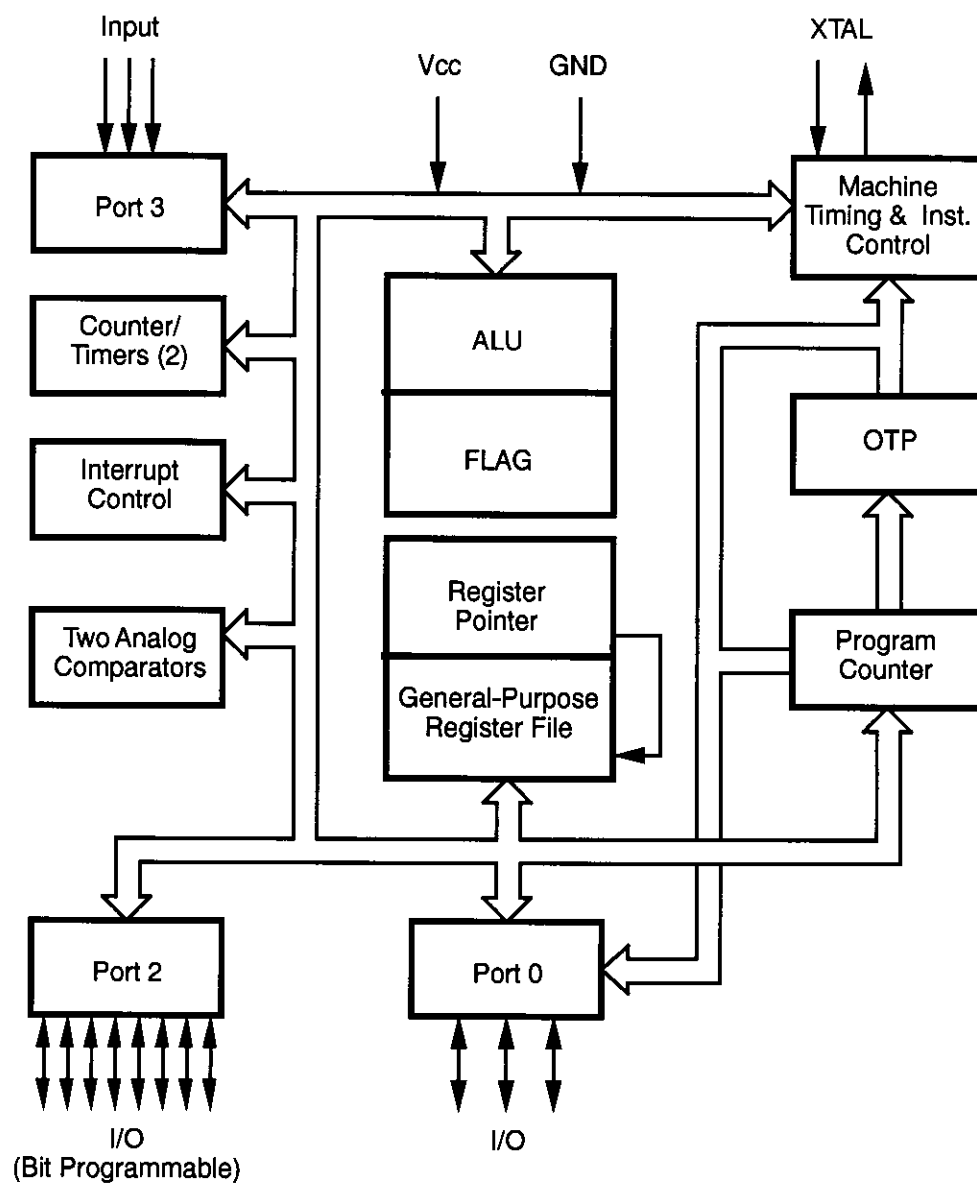


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION (Continued)

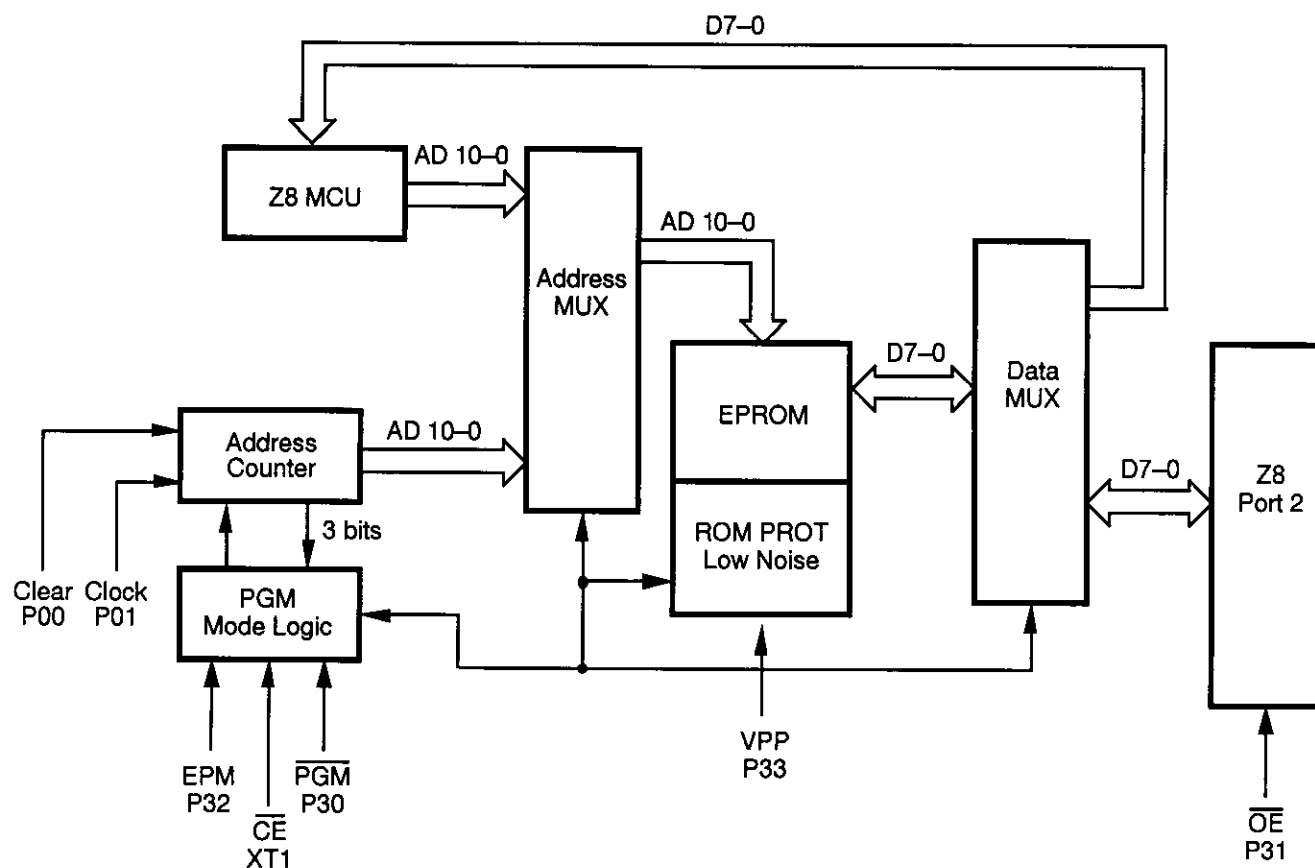


Figure 2. EPROM Programming Mode Block Diagram

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

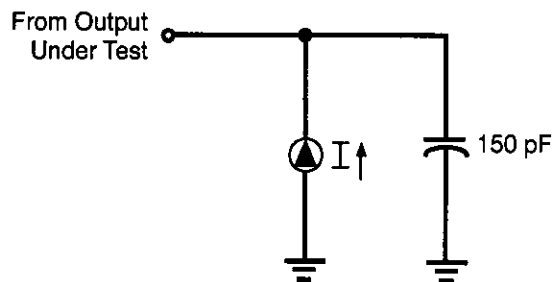


Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS

Standard Temperature

Sym	Parameter	V _{CC} [4]	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V _{INMAX}	Max Input Voltage	4.5V		12		V	I _{in} < 250 μA	1
		5.5V		12		V	I _{in} < 250 μA	1
V _{CH}	Clock Input High Voltage	4.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
V _{IL}	Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage	4.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		4.5V	V _{CC} -0.4		4.8	V	Low Noise @ I _{OH} = -0.5 mA	
		5.5V	V _{CC} -0.4		4.8	V	Low Noise @ I _{OH} = -0.5 mA	
V _{OL1}	Output Low Voltage	4.5V		0.8	0.1	V	I _{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
V _{OL2}	Output Low Voltage	4.5V		0.8	0.8	V	I _{OL} = +12 mA,	5
		5.5V		0.8	0.8	V	I _{OL} = +12 mA,	5
V _{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V _{LV}	V _{CC} Low Voltage Auto Reset		2.2	3.0	2.8	V	@ 6 MHz Max. Int. CLK Freq.	
I _{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	4.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range		0	V _{CC} -1.0		V		

DC ELECTRICAL CHARACTERISTICS

Extended Temperature

Sym	Parameter	V _{CC} [4]	T _A = -40°C to +105°C		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V _{INMAX}	Max Input Voltage	4.5V		12.0		V	I _{IN} < 250 µA	1
		5.5V		12.0		V	I _{IN} < 250 µA	1
V _{CH}	Clock Input High Voltage	4.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8 V _{CC}	V _{CC} +0.3	2.8	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.7	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	4.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	2.8	V		
V _{IL}	Input Low Voltage	4.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
		5.5V	V _{SS} -0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage	4.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	5
		4.5V	V _{CC} -0.4			V	Low Noise @ I _{OH} = -0.5 mA	
		5.5V	V _{CC} -0.4			V	Low Noise @ I _{OH} = -0.5 mA	
V _{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I _{OL} = +4.0 mA	5
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	5
		4.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
		5.5V		0.4	0.1	V	Low Noise @ I _{OL} = 1.0 mA	
V _{OL2}	Output Low Voltage	4.5V		1.0	0.3	V	I _{OL} = +12 mA,	5
		5.5V		1.0	0.3	V	I _{OL} = +12 mA,	5
V _{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
V _{LV}	V _{CC} Low Voltage Auto Reset		1.8	3.8	2.8	V	@ 6 MHz Max. Int. CLK Freq.	3
I _{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
		5.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	4.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
		5.5V		-1.0	1.0	µA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range		0	V _{CC} -1.5		V		

AC ELECTRICAL CHARACTERISTICS

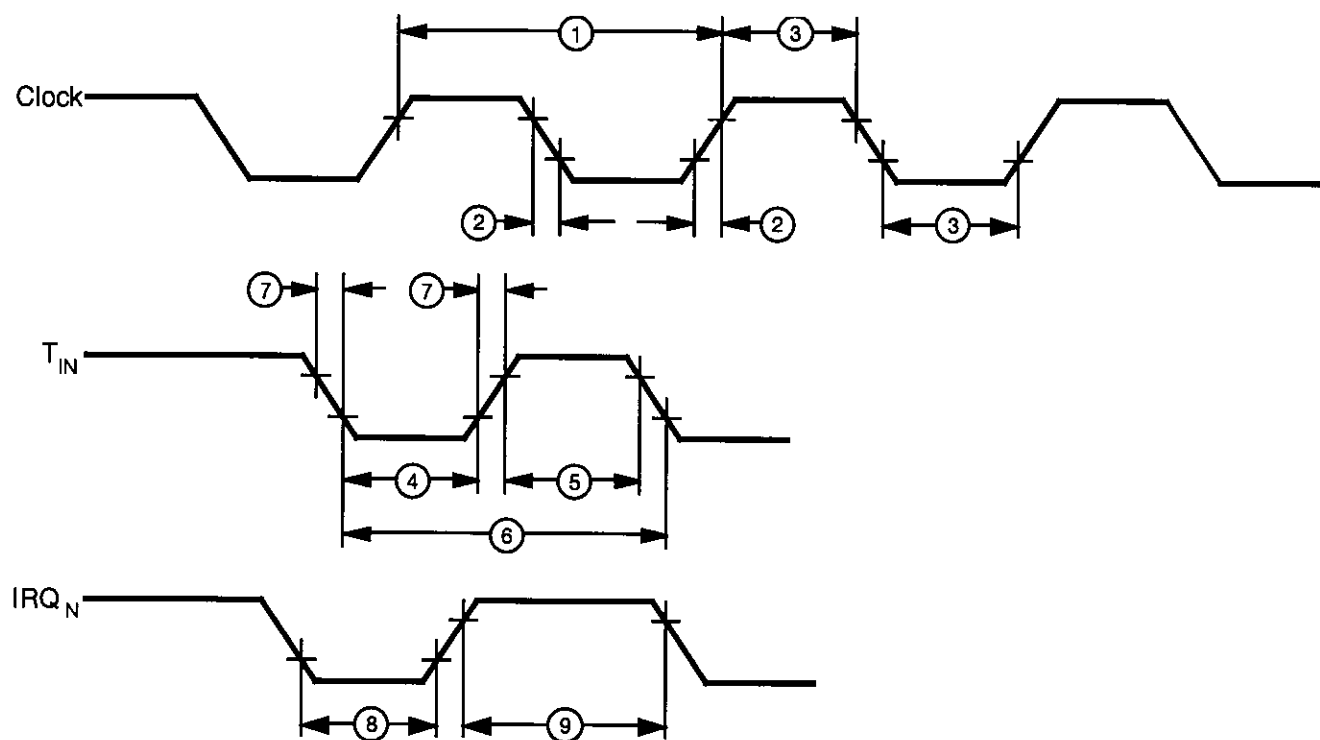


Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode, Standard Temperature

No	Symbol	Parameter	V _{CC}	T _A = 0 °C to +70 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V		25		25	ns	1
			5.5V		25		25	ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	TwIL Low Time	Int. Request Input	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH High Time	Int. Request Input	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	12		12		ms	1
			5.5V	12		12		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

No	Symbol	Parameter	V _{CC}	T _A = −40 °C to +105 °C				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	1
			5.5V	1000	DC	250	DC	ns	1
2	TrC TfC	Clock Input Rise and Fall Times	4.5V	25		25		ns	1
			5.5V	25		25		ns	1
3	TwC	Input Clock Width	4.5V	500		125		ns	1
			5.5V	500		125		ns	1
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			1
			5.5V	2.5TpC		2.5TpC			1
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			1
			5.5V	4TpC		4TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	4.5V	100		100		ns	1
			5.5V	100		100		ns	1
8	TwIL	Int. Request Input Low Time	4.5V	70		70		ns	1,2
			5.5V	70		70		ns	1,2
9	TwIH	Int. Request Input High Time	4.5V	2.5TpC		2.5TpC			1,2
			5.5V	2.5TpC		2.5TpC			1,2
10	Twdt	Watch-Dog Timer Delay Time for Timeout	4.5V	10		10		ms	1
			5.5V	10		10		ms	1

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software

control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

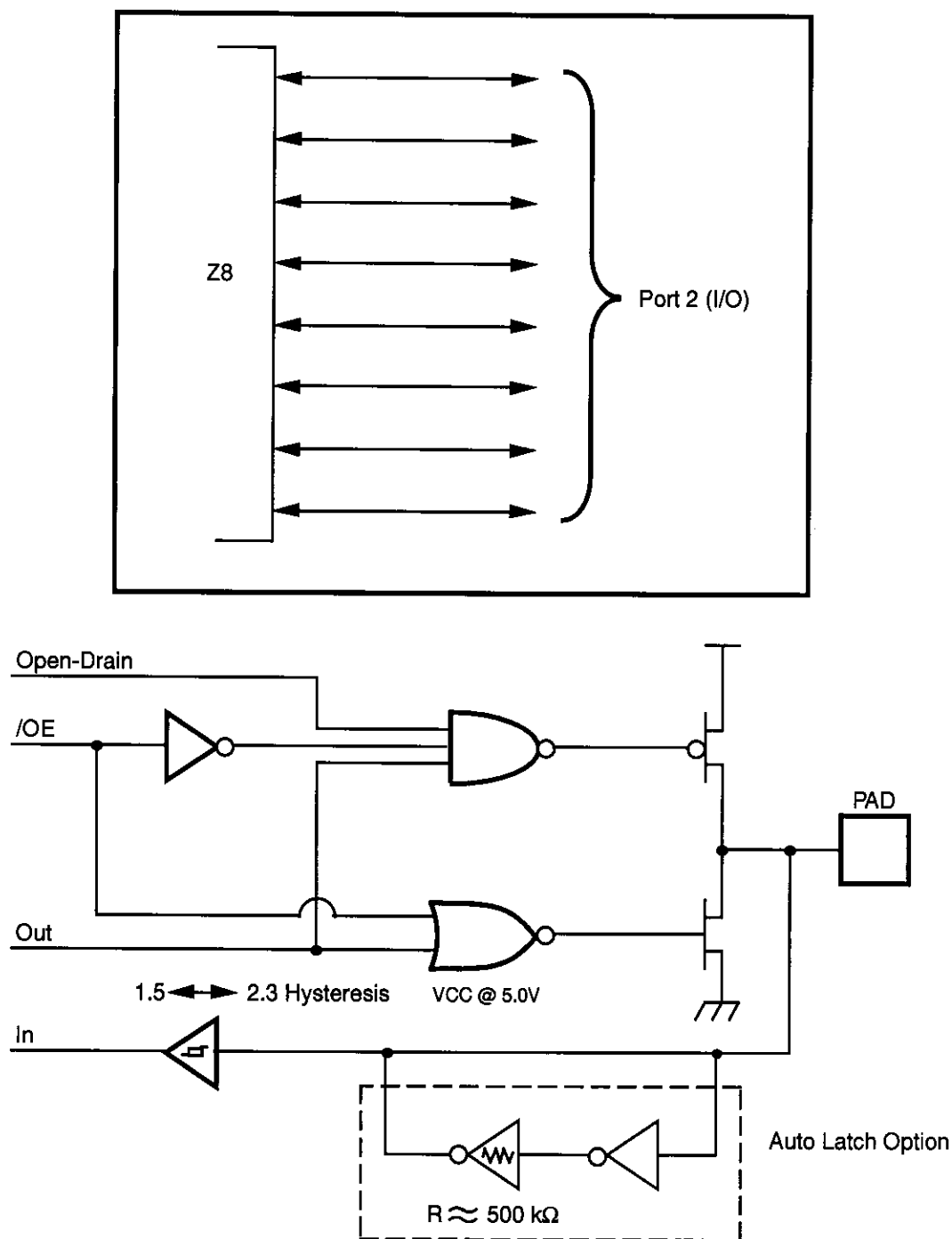


Figure 8. Port 2 Configuration

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

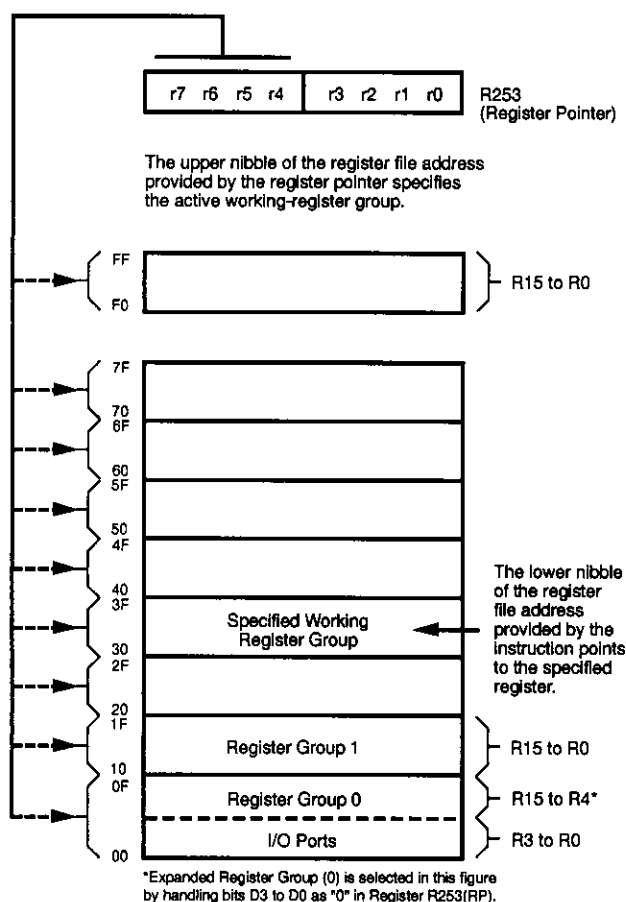


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

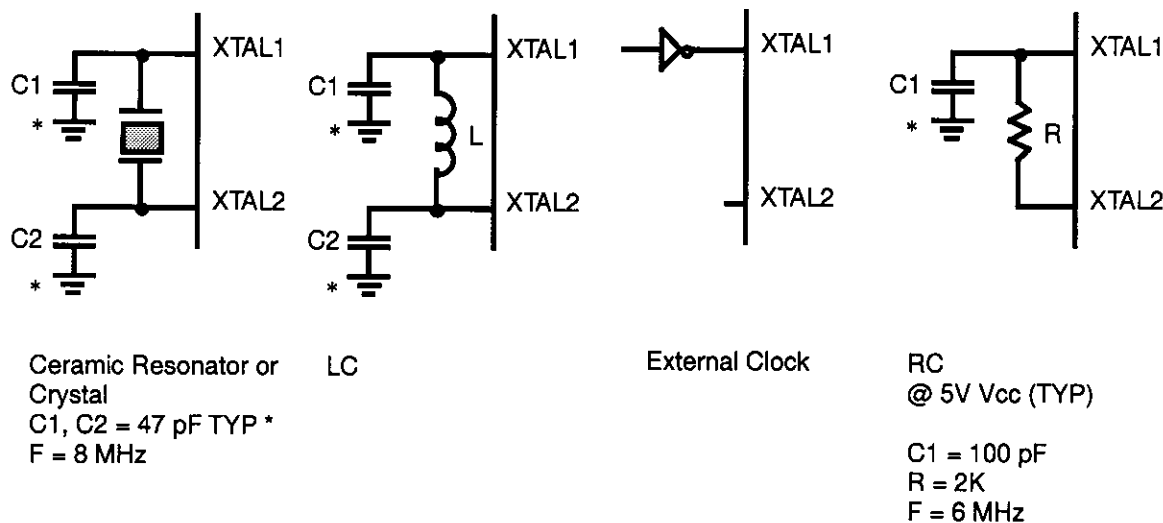
The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



* Typical value including pin parasitics

Figure 16. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μ A. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT} ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR} , plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV} .

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

FUNCTIONAL DESCRIPTION (Continued)

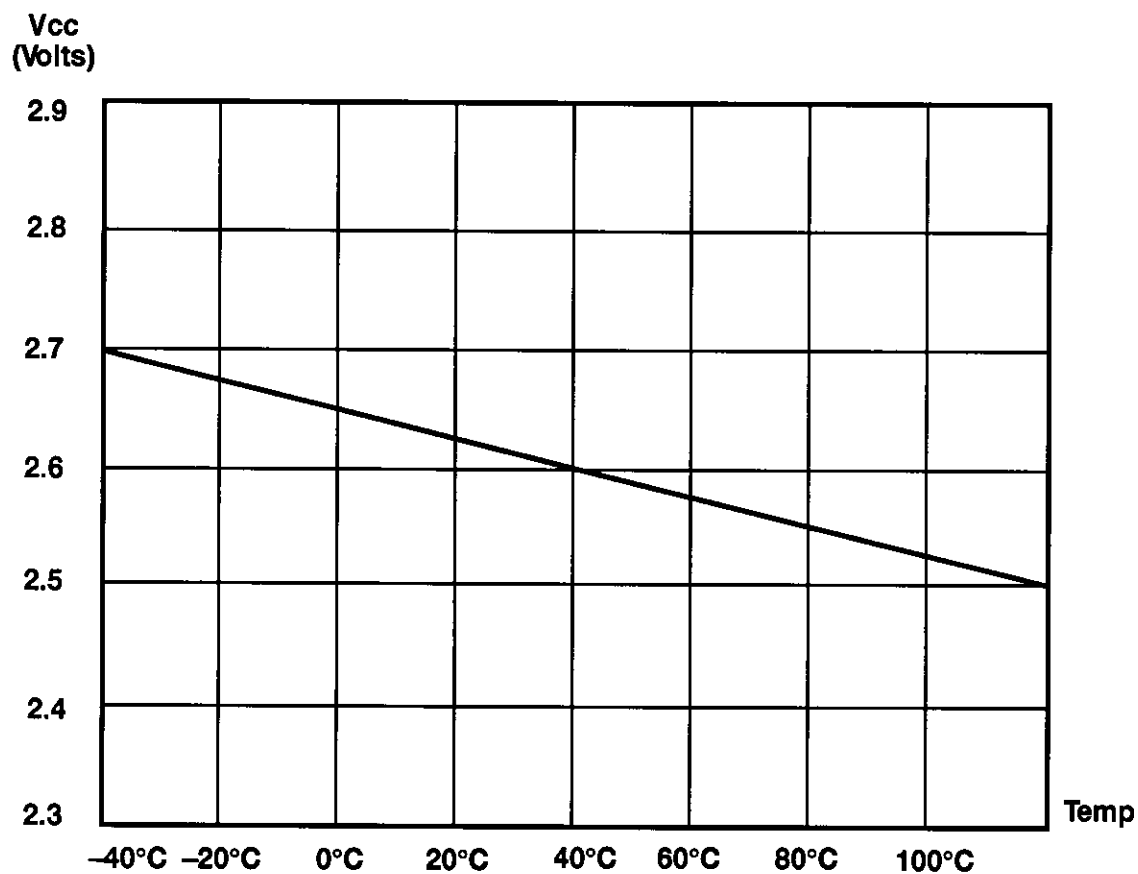
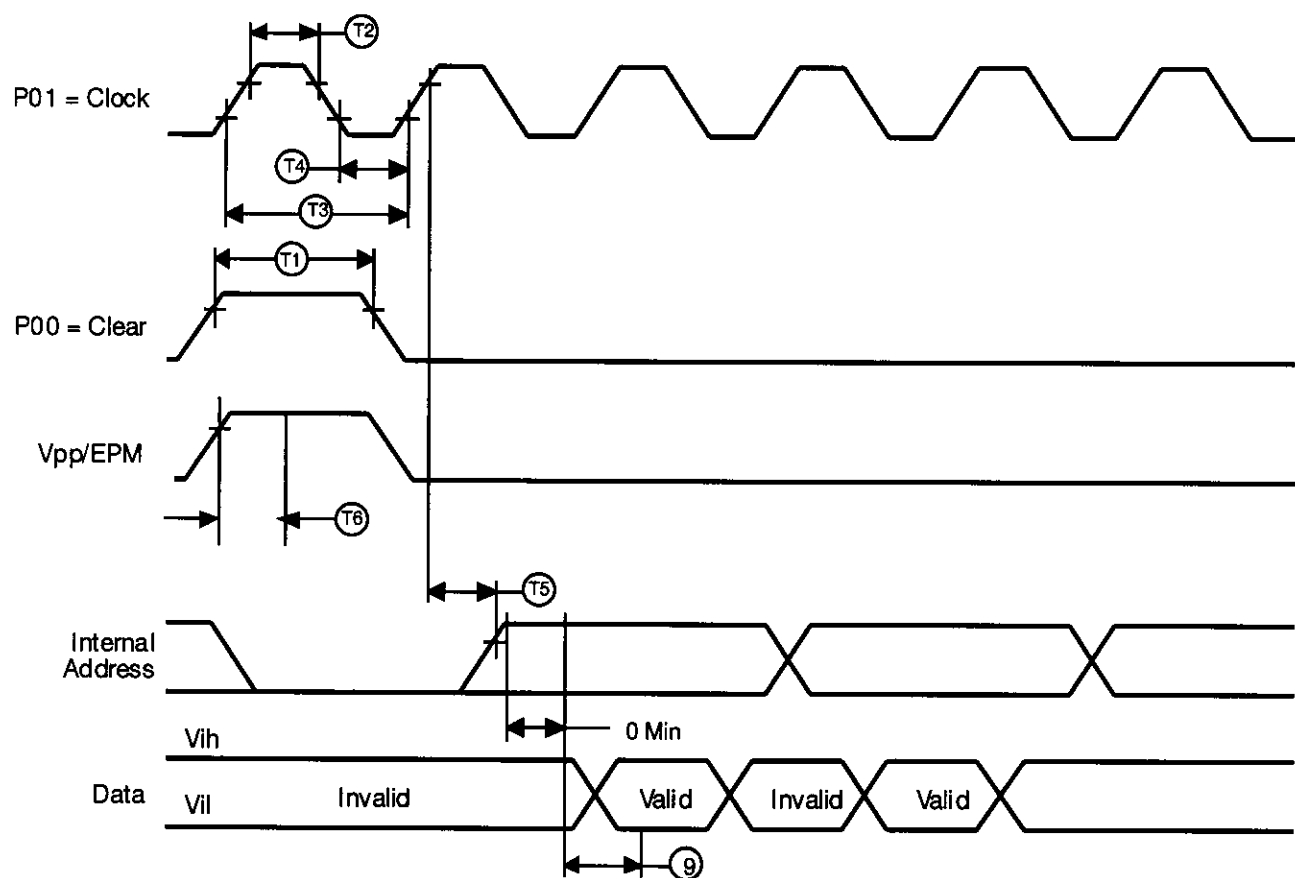


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 μ s Min

Figure 18. Z86E04/E08 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

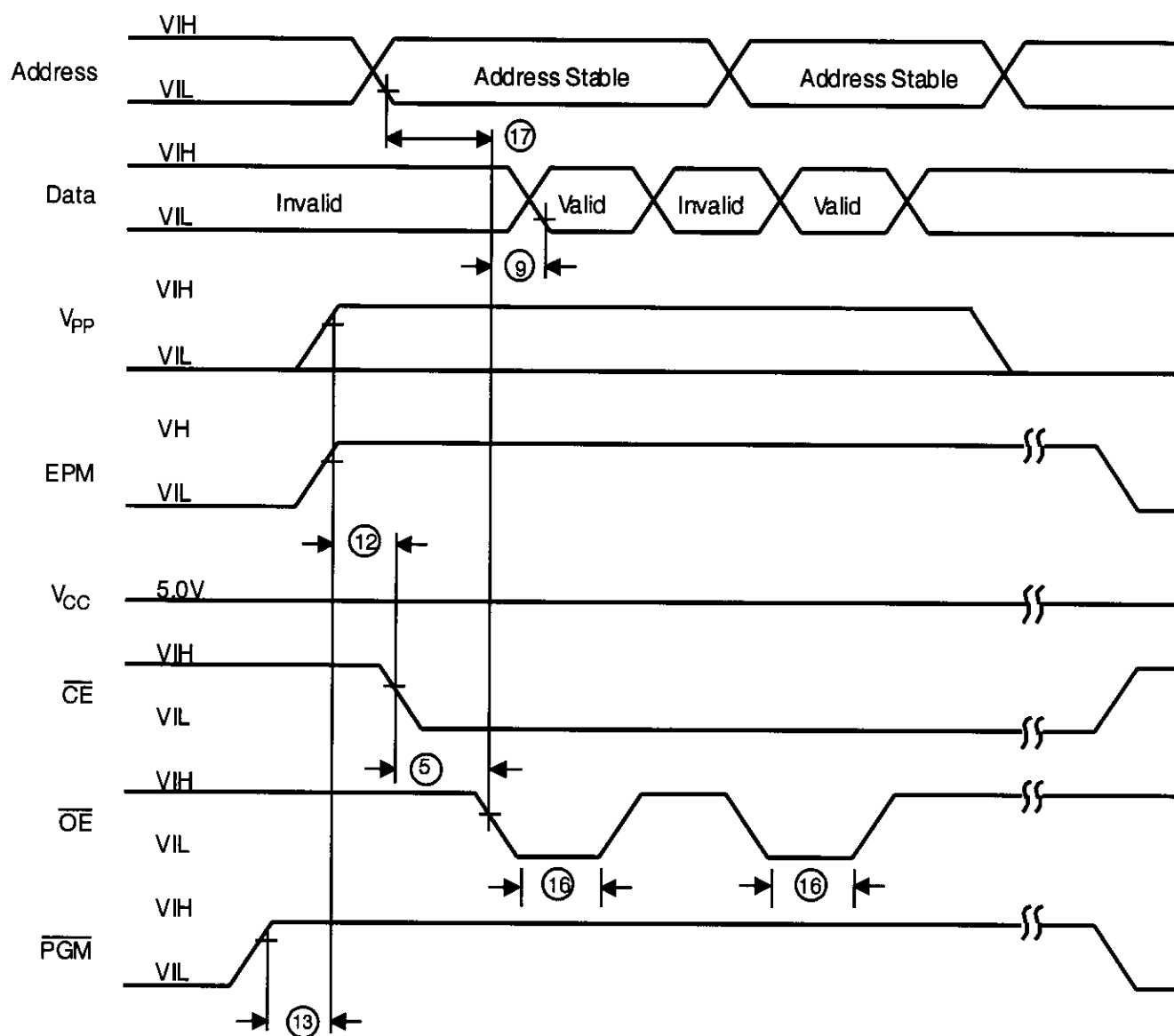


Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)

FUNCTIONAL DESCRIPTION (Continued)

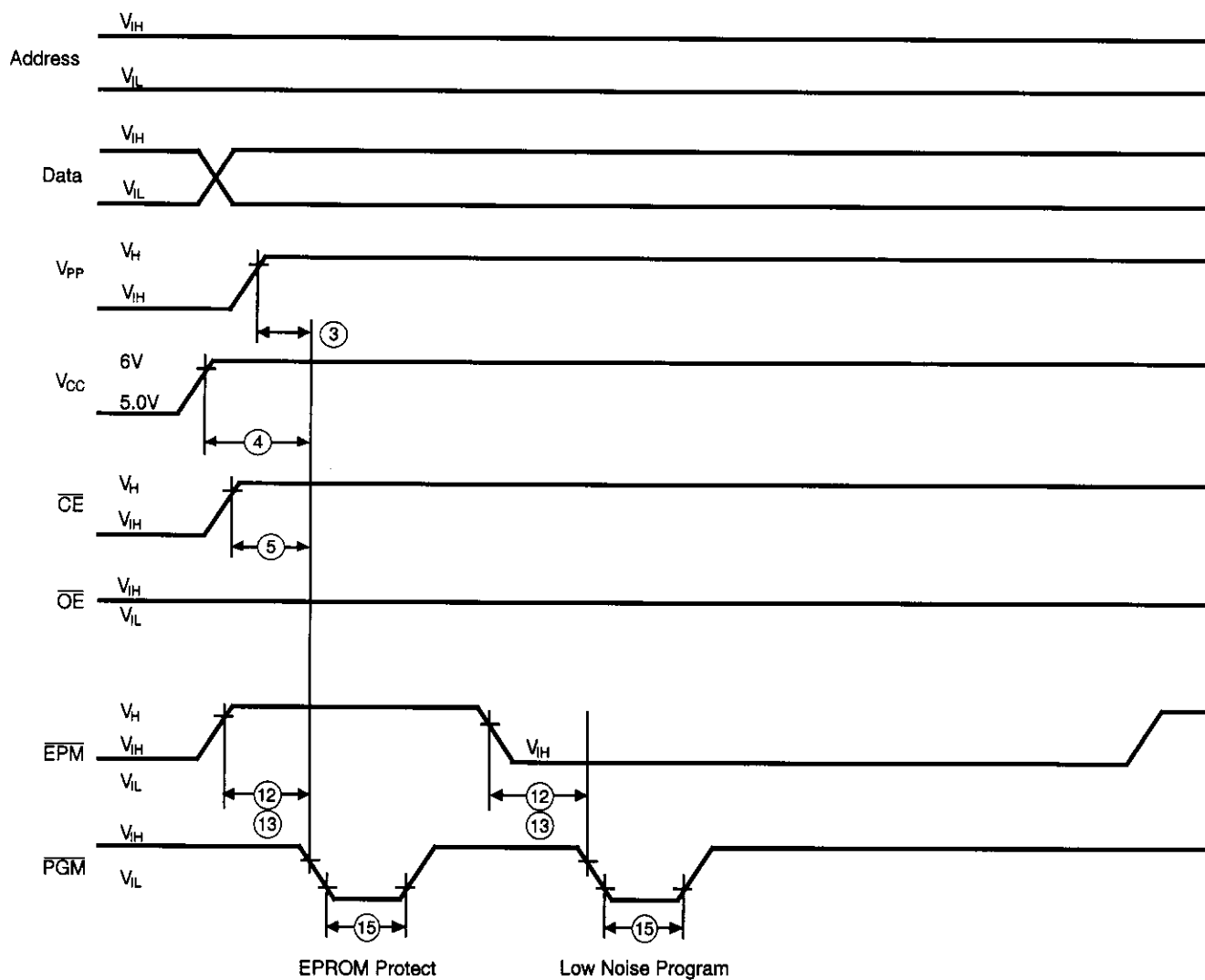
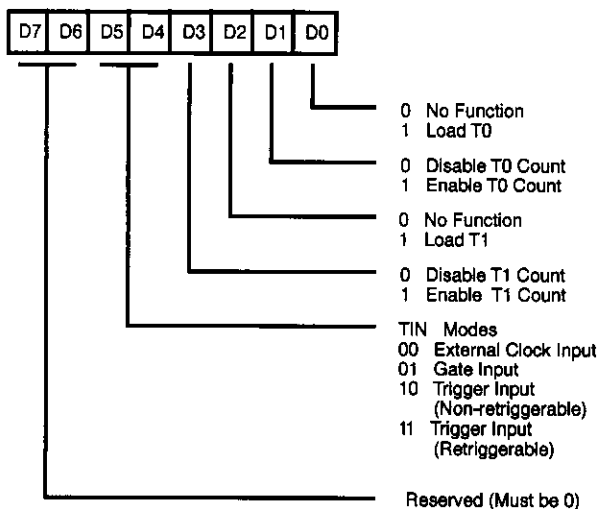


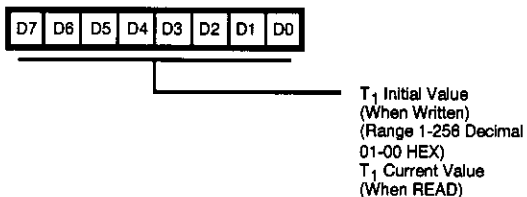
Figure 21. Z86E04/E08 Programming Options Waveform
(EPROM Protect and Low Noise Program)

Z8 CONTROL REGISTERS

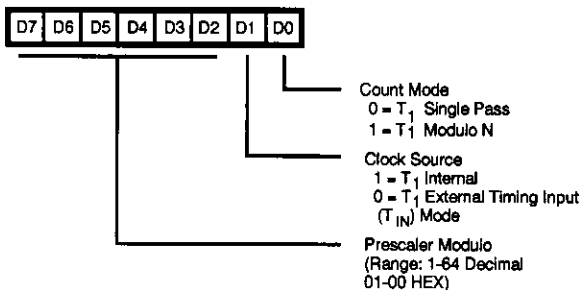
R241 TMR

Figure 24. Timer Mode Register (F1_H: Read/Write)

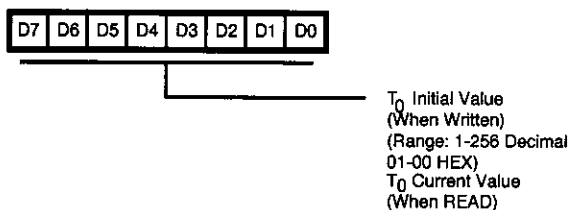
R242 T1

Figure 25. Counter Timer 1 Register (F2_H: Read/Write)

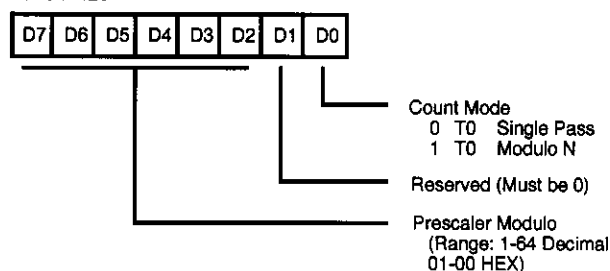
R243 PRE1

Figure 26. Prescaler 1 Register (F3_H: Write Only)

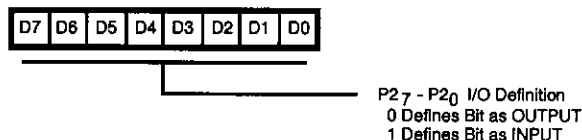
R244 T0

Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

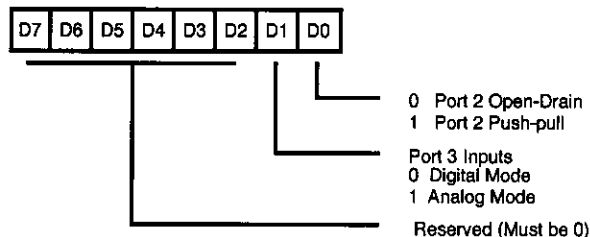
R245 PRE0

Figure 28. Prescaler 0 Register (F5_H: Write Only)

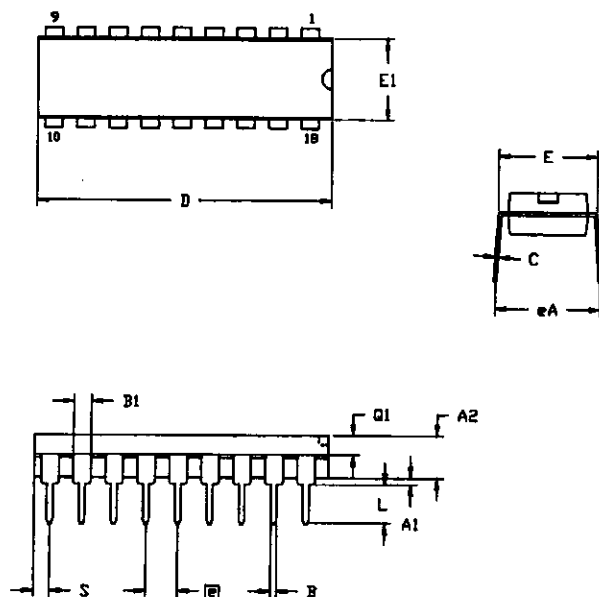
R246 P2M

Figure 29. Port 2 Mode Register (F6_H: Write Only)

R247 P3M

Figure 30. Port 3 Mode Register (F7_H: Write Only)

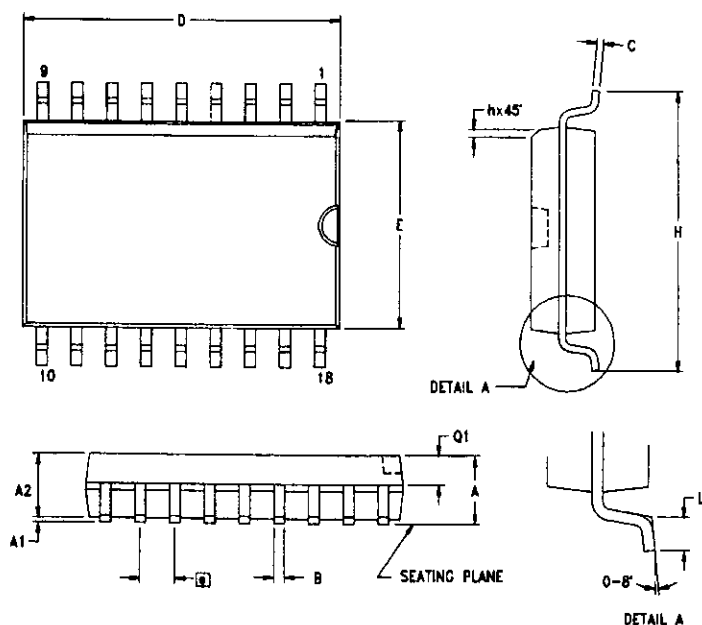
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
□	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
□	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E04

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86E0412PSC	Z86E0412SSC
Z86E0412PEC	Z86E0412SEC

Z86E08

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86E0812PSC	Z86E0812SSC
Z86E0812PEC	Z86E0812SEC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

Codes

Preferred Package

P = Plastic DIP

Speeds

12 = 12 MHz

Longer Lead Time

S = SOIC

Environmental

C = Plastic Standard

Preferred Temperature

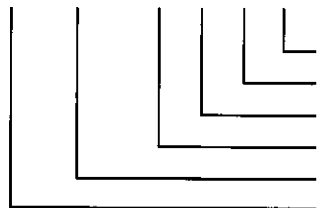
S = 0°C to +70°C

E = -40°C to +105°C

Example:

Z 86E04 12 P S C

is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Environmental Flow
Temperature
Package
Speed
Product Number
Zilog Prefix

Pre-Characterization Product:

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