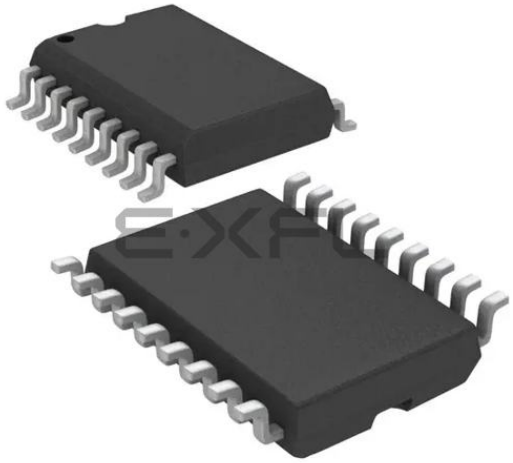

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	125 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e0812ssg1903

FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
  - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1µs @ 12 MHz)
- RAM Bytes (125)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8® MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All Signals with an overline, "‾", are active Low, for example: B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

PIN DESCRIPTION

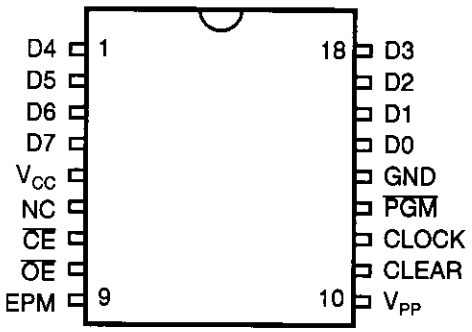


Figure 3. 18-Pin EPROM Mode Configuration

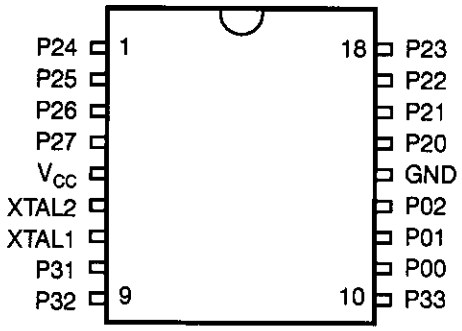


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	D4–D7	Data 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	NC	No Connection	
7	$\overline{CE}$	Chip Enable	Input
8	$\overline{OE}$	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	V_{PP}	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	$\overline{PGM}$	Prog Mode	Input
14	GND	Ground	
15–18	D0–D3	Data 0,1, 2, 3	In/Output

Table 2. 18-Pin DIP/SOIC Pin Identification

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	P24–P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11–13	P00–P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15–18	P20–P23	Port 2, Pins 0,1,2,3	In/Output

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

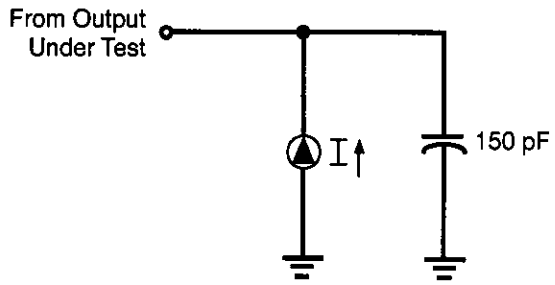


Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	10 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 2 MHz	5,7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 8 MHz	5,7
		4.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @ 12 MHz	5,7
I_{CC1}	Standby Current	4.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		5.5V		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	5,7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	5,7
		4.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
		5.5V		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	5,7
I_{CC}	Supply Current (Low Noise Mode)	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @ 1 MHz	7
		4.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @ 2 MHz	7
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @ 4 MHz	7

Sym	Parameter	V_{CC} [4]	T_A = –40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		5.5V		4.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 1 MHz	7
		4.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		5.5V		4.5	2.8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz	7
		4.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
		5.5V		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 4 MHz	7
I_{CC2}	Standby Current	4.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	7,8
I_{ALL}	Auto Latch Low Current	4.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		40	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	4.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	
		5.5V		–20.0	–8.0	µA	$0V < V_{IN} < V_{CC}$	

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS

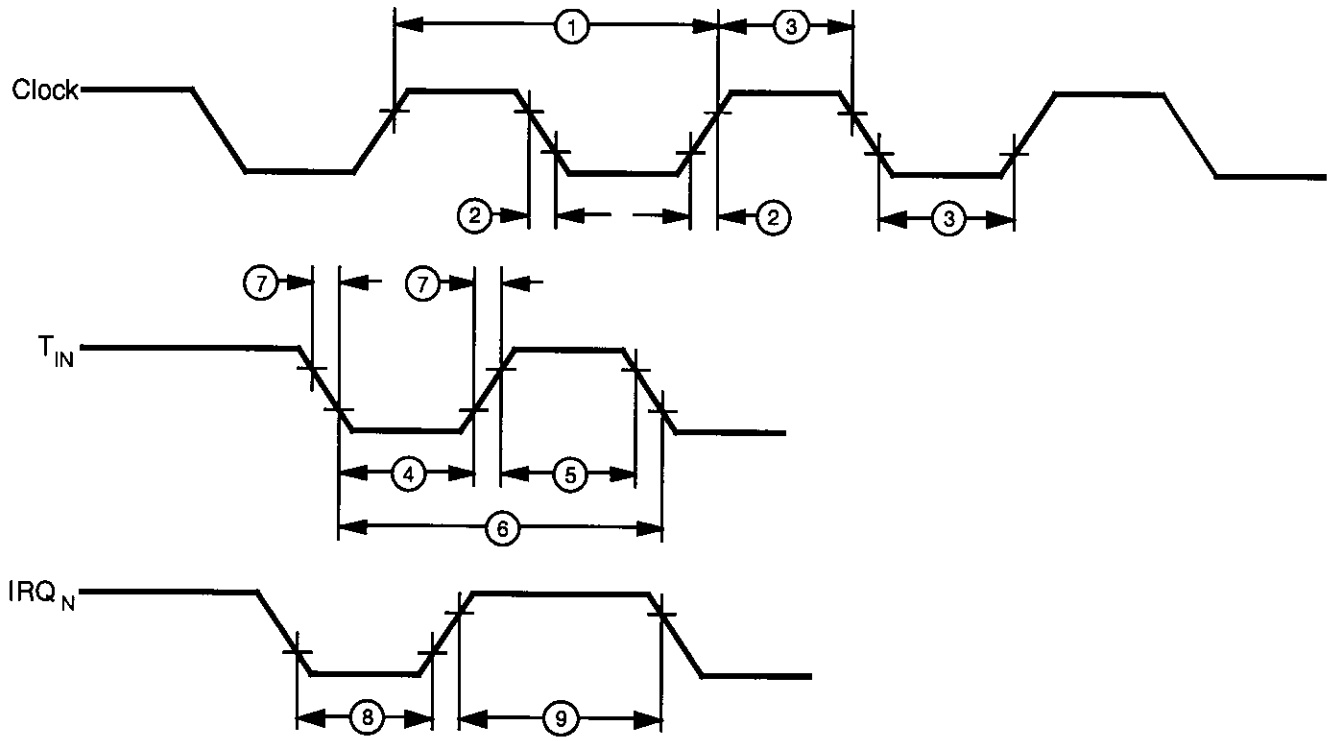


Figure 6. AC Electrical Timing Diagram

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 *Data Bus.* Data can be read from, or written to, the EPROM through this data bus.

V_{CC} *Power Supply.* It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

$\overline{CE}$ *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

$\overline{OE}$ *Output Enable* (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

Clear *Clear* (active High). This pin resets the internal address counter at the High Level.

Clock *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock cycle.

$\overline{PGM}$ *Program Mode* (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise*** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by ***excessive noise*** surges on the V_{PP}, $\overline{CE}$, EPM, $\overline{OE}$ pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).

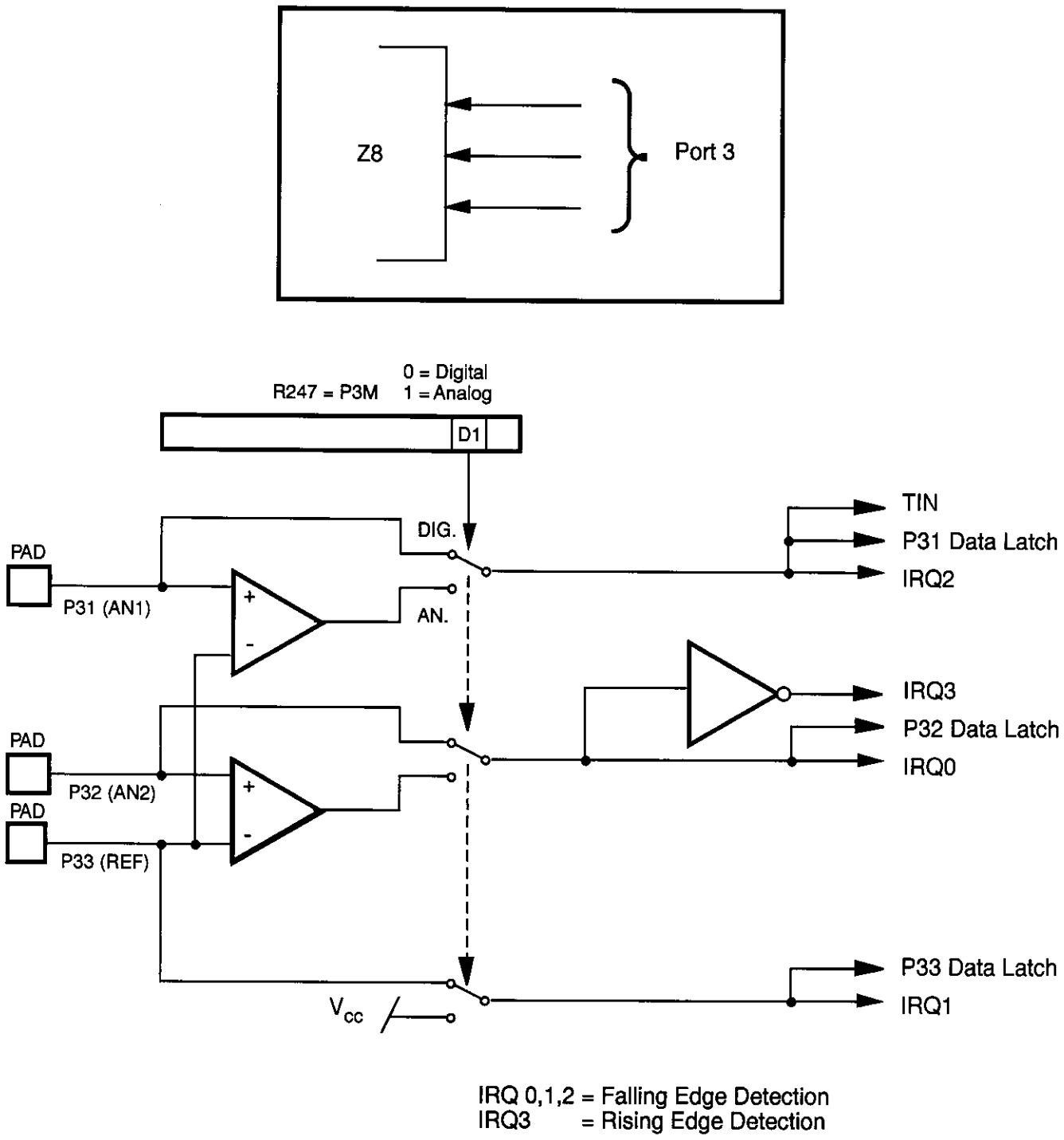


Figure 9. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

		Reset Condition								
Addr.	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

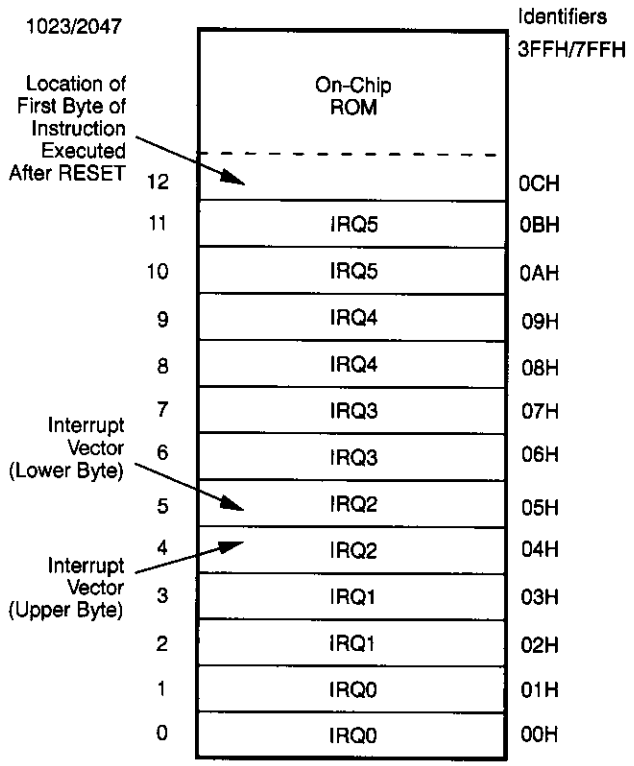


Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

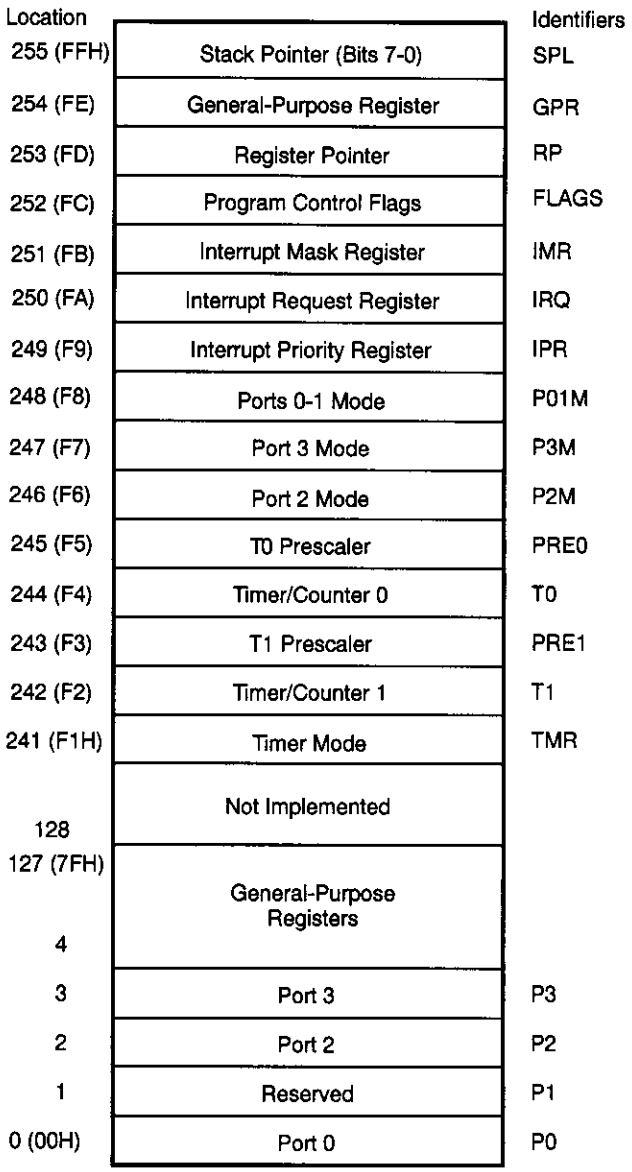
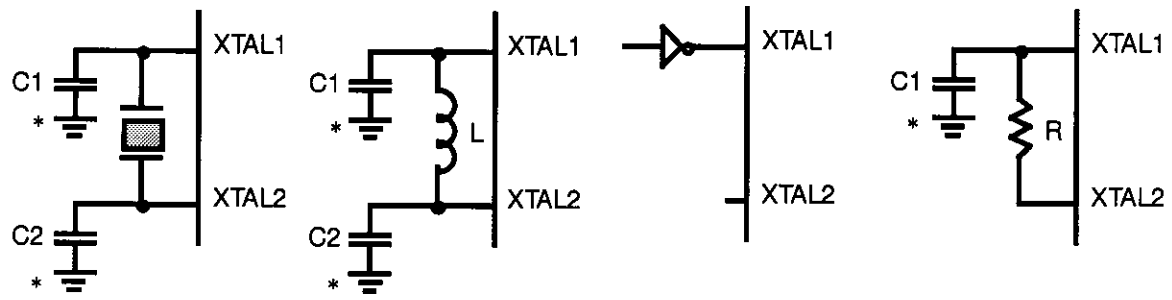


Figure 12. Register File

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC

External Clock

RC
@ 5V Vcc (TYP)

C1 = 100 pF
R = 2K
F = 6 MHz

* Typical value including pin parasitics

Figure 16. Oscillator Configuration

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
            or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}.

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

FUNCTIONAL DESCRIPTION (Continued)

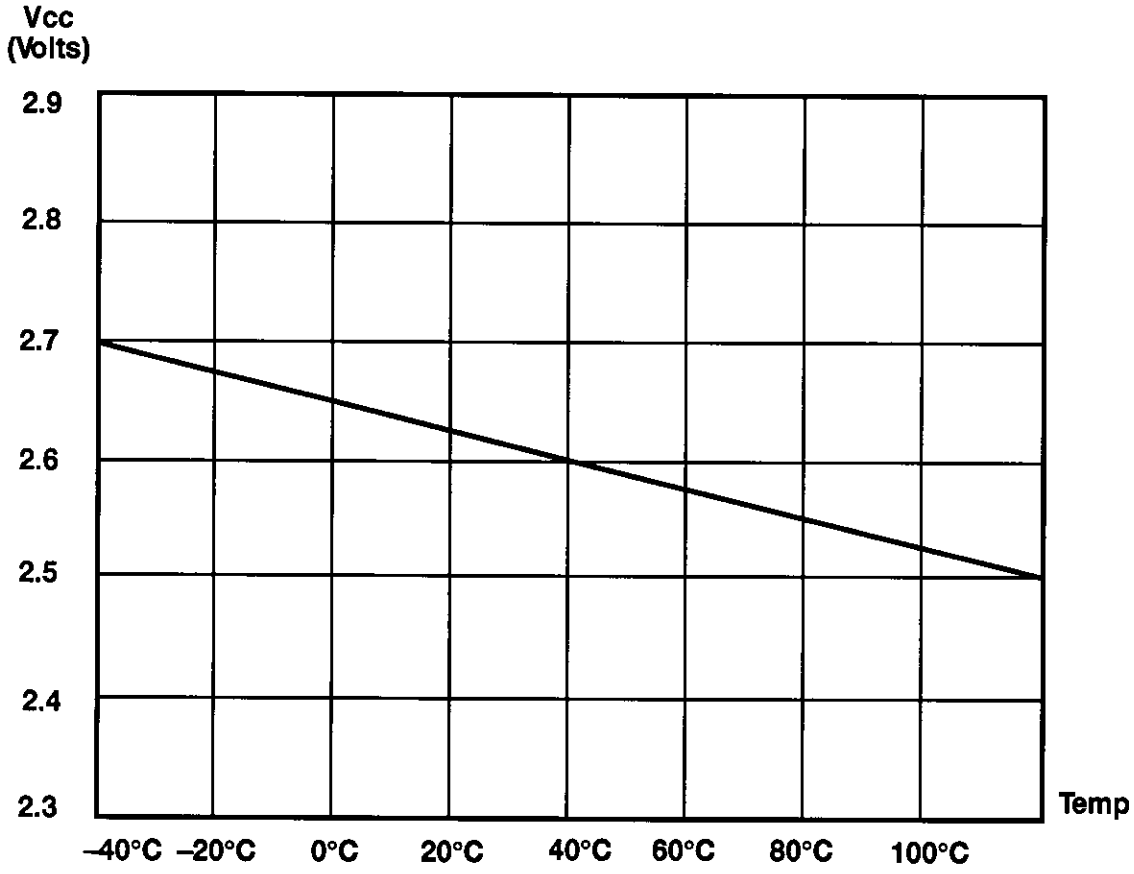


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

Low EMI Emission

The Z8 can be programmed to operate in a low EMI Emission (Low Noise) Mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT Mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM Mode. XTAL2 has no function, XTAL1 functions as $\overline{CE}$, P31 functions as $\overline{OE}$, P32 functions as EPM, P33 functions as V_{PP}, and P02 functions as $\overline{PGM}$.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI **are supported** (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will not automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and $\overline{CE}$ pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP Mode. The V_{PP} requires both a diode and a 100 pF capacitor.

Auto Latch Disable. Auto Latch Disable option bit when programmed will globally disable all Auto Latches.

WDT Enable. The WDT Enable option bit, when programmed, will have the hardware enabled Permanent WDT enabled after exiting reset and can not be stopped in Halt or Stop Mode.

EPROM/Test Mode Disable. The EPROM/Test Mode Disable option bit, when programmed, will disable the EPROM Mode and the Factory Test Mode. Reading, verifying, and programming the Z8 will be disabled. To fully verify that this mode is disabled, the device must be power cycled.

User Modes. Table 7 shows the programming voltage of each mode.

Table 7. OTP Programming Table

Programming Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	DATA	V_{CC}*
EPROM READ	NU	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.0V
PROGRAM	V_H	V_{IH}	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.4V
PROGRAM VERIFY	V_H	V_{IH}	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.4V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
LOW NOISE SELECT	V_H	V_{IH}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
AUTO LATCH DISABLE	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V
WDT ENABLE	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.4V
EPROM/TEST MODE	V_H	V_{IL}	V_H	V_{IL}	V_{IL}	NU	NU	6.4V

Notes:

1. V_H =12.75V ± 0.25 V_{DC} .
2. V_{IH} = As per specific Z8 DC specification.
3. V_{IL} = As per specific Z8 DC specification.
4. X = Not used, but must be set to V_H or V_{IH} level.
5. NU = Not used, but must be set to either V_{IH} or V_{IL} level.
6. I_{PP} during programming = 40 mA maximum.
7. I_{CC} during programming, verify, or read = 40 mA maximum.
8. * V_{CC} has a tolerance of ±0.25V.

FUNCTIONAL DESCRIPTION (Continued)

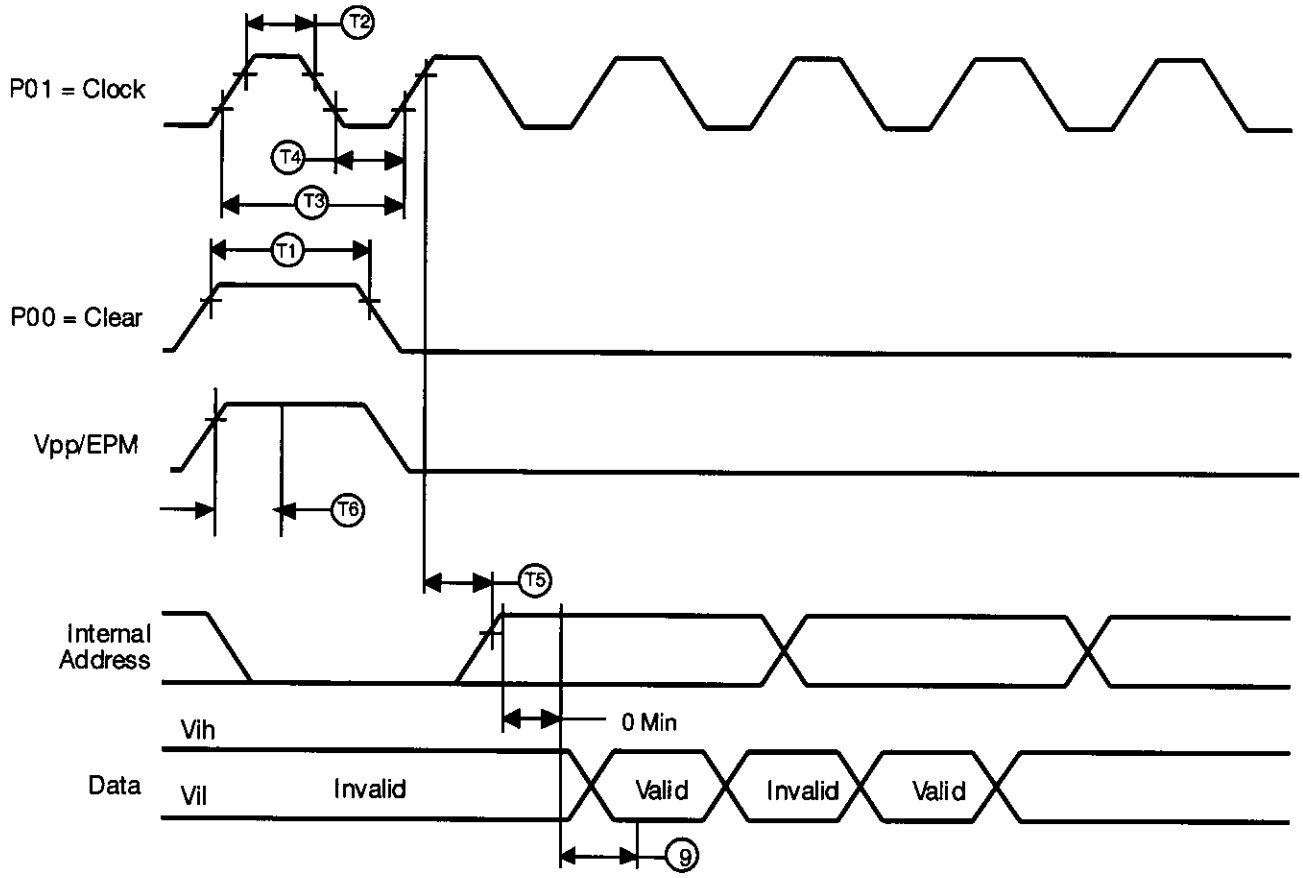
Internal Address Counter. The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

Programming Waveform. Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

Programming Algorithm. Figure 23 shows the flow chart of the Z8 programming algorithm.

Table 8. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time	188		ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms
16	$\overline{OE}$ Width	250		ns
17	Address Valid to $\overline{OE}$ Low	125		ns



Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	100 ns Min
T3 Input Clock Period	200 ns Min
T4 Input Clock Low	100 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max
T6 Epm/Vpp Set up Time	40 µs Min

Figure 18. Z86E04/E08 Address Counter Waveform

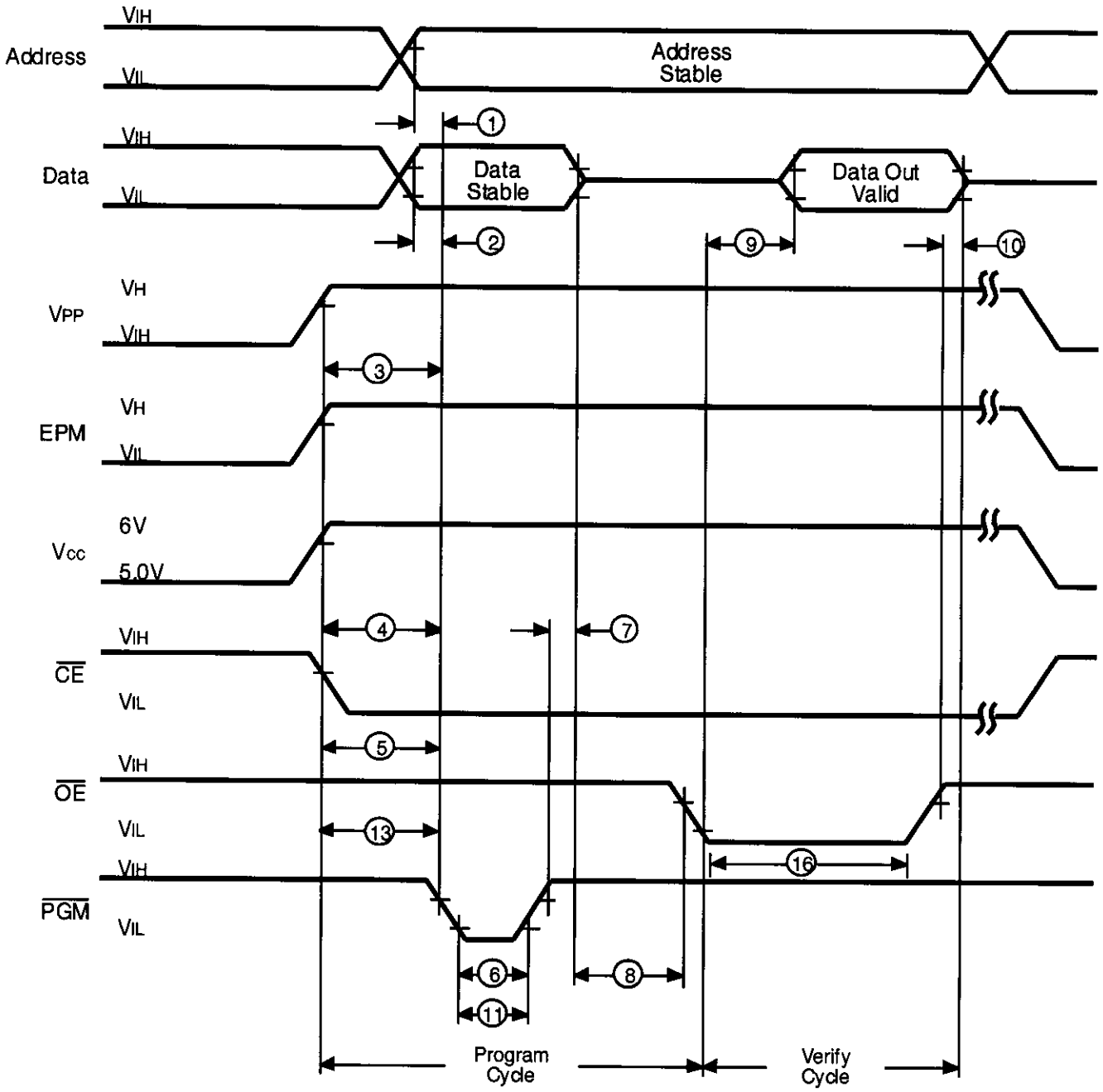


Figure 20. Z86E04/E08 Programming Waveform (Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)

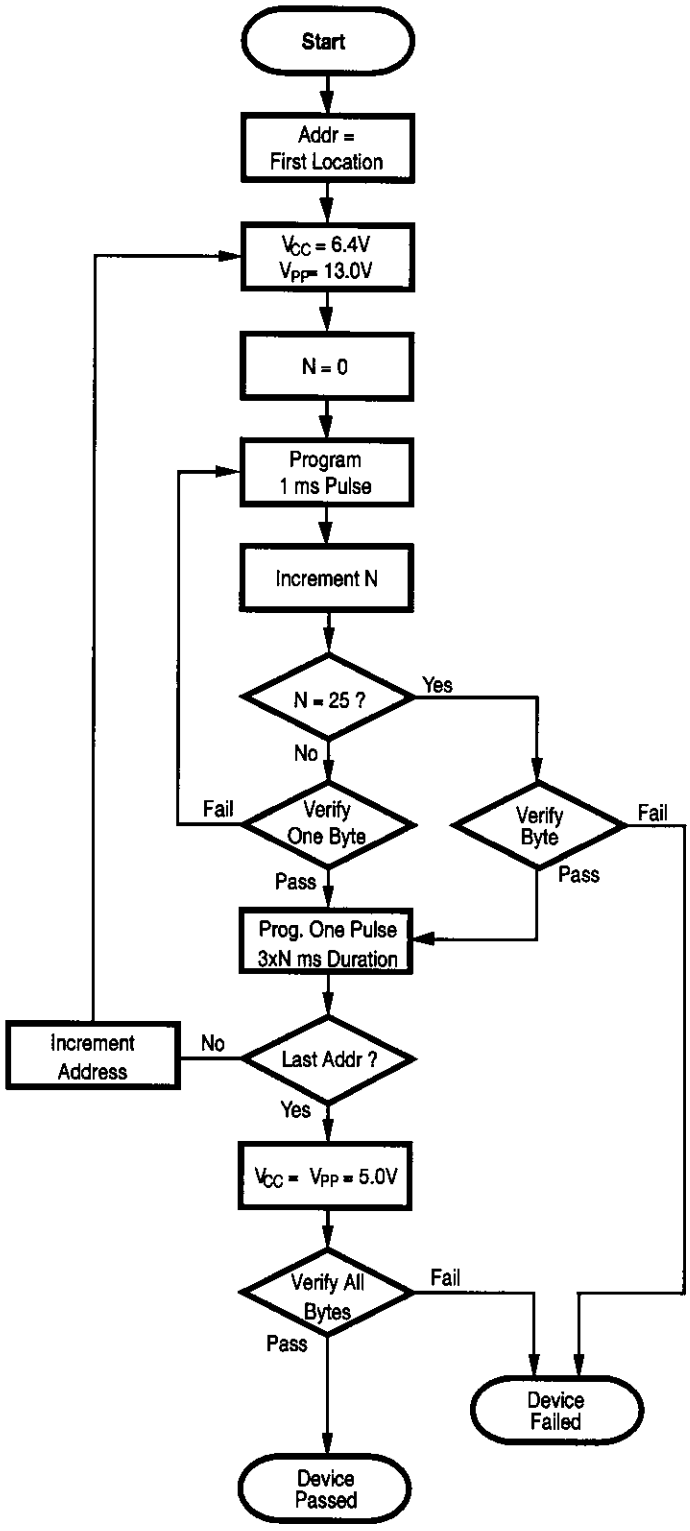
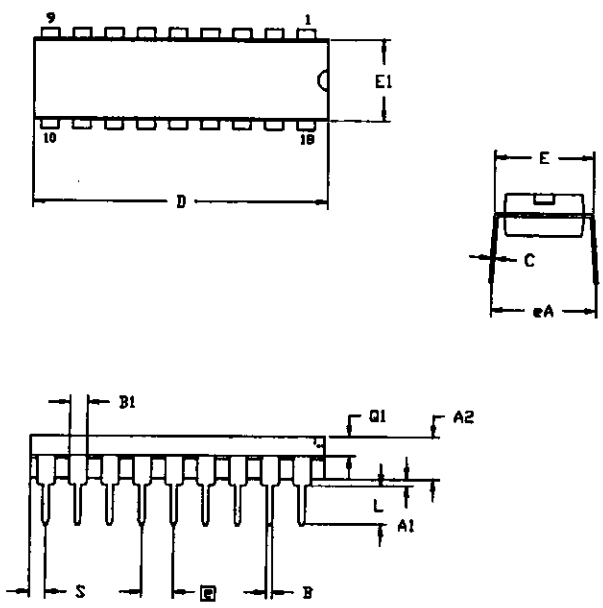


Figure 23. Z86E04/E08 Programming Algorithm

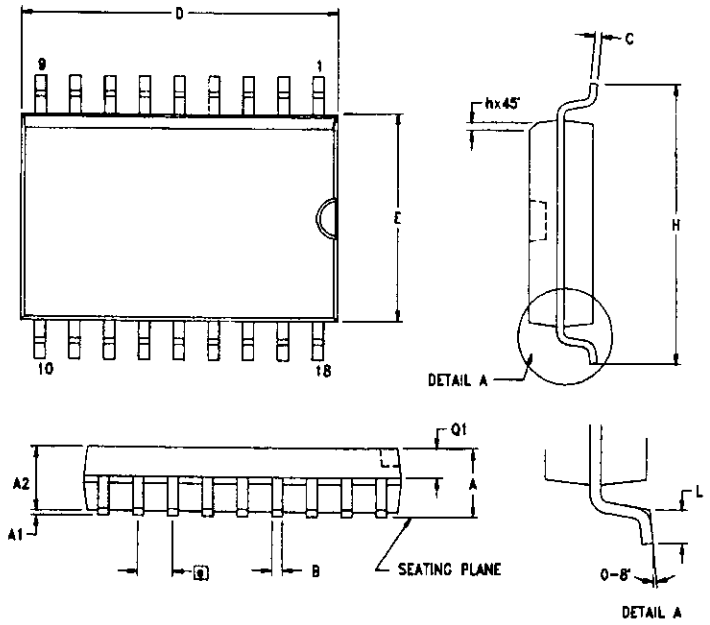
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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