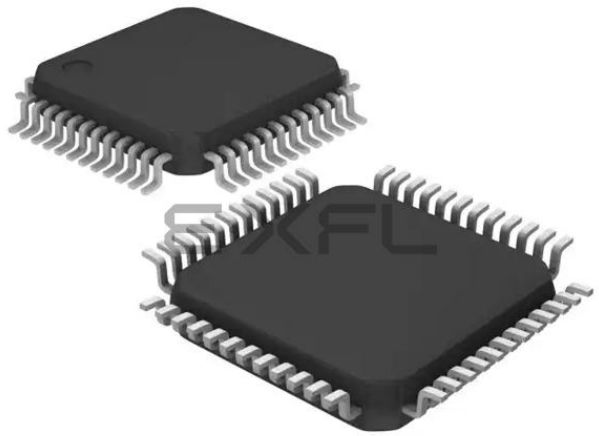

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101cbt6

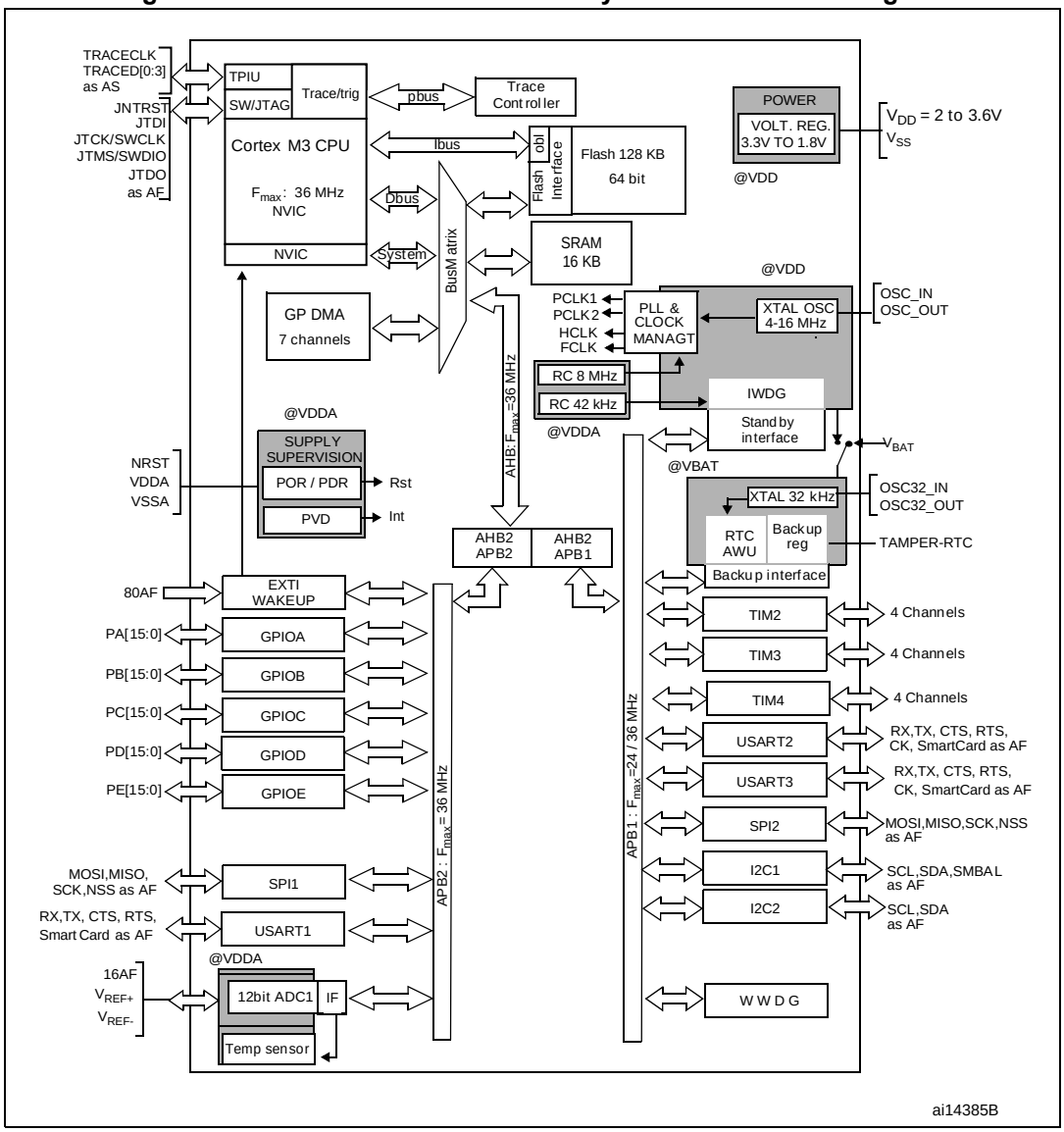
1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x8 and STM32F101xB medium-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F101xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex® -M3 core please refer to the Cortex® -M3 Technical Reference Manual, available from the www.arm.com website.

Figure 1. STM32F101xx medium-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

2.3 Overview

2.3.1 ARM® Cortex® -M3 core with embedded Flash and SRAM

The ARM® Cortex® -M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex® -M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xx medium-density access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F101xx medium-density access line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex® -M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

Figure 4. STM32F101xx medium-density access line LQFP64 pinout

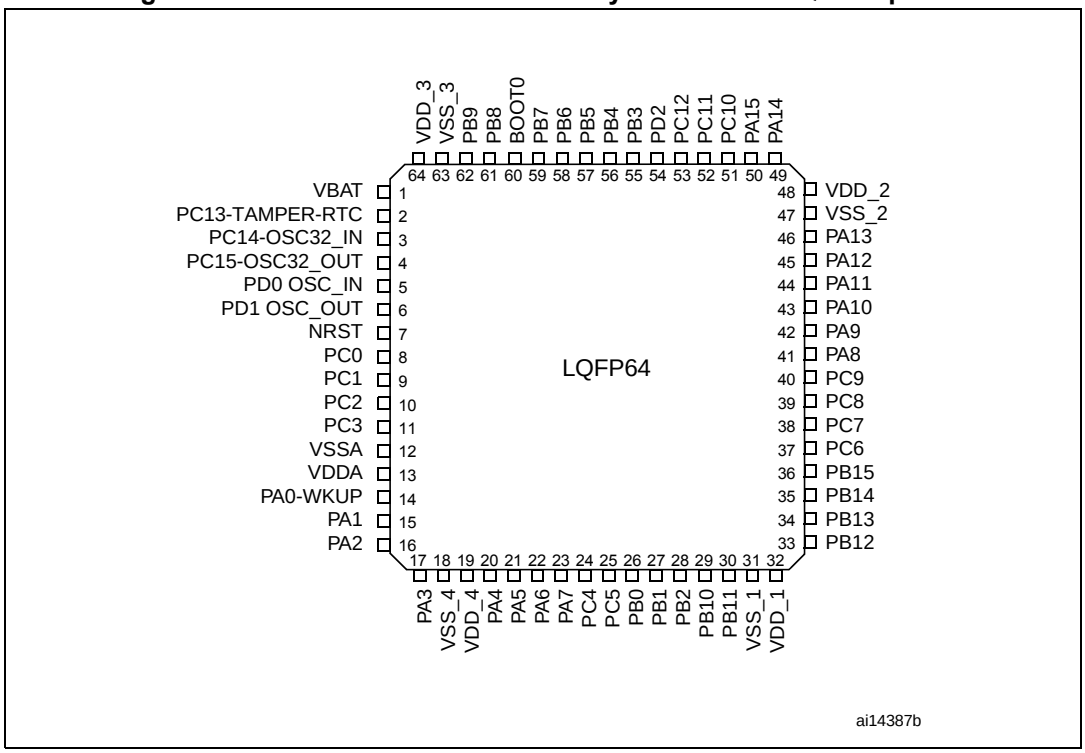


Figure 5. STM32F101xx medium-density access line LQFP48 pinout

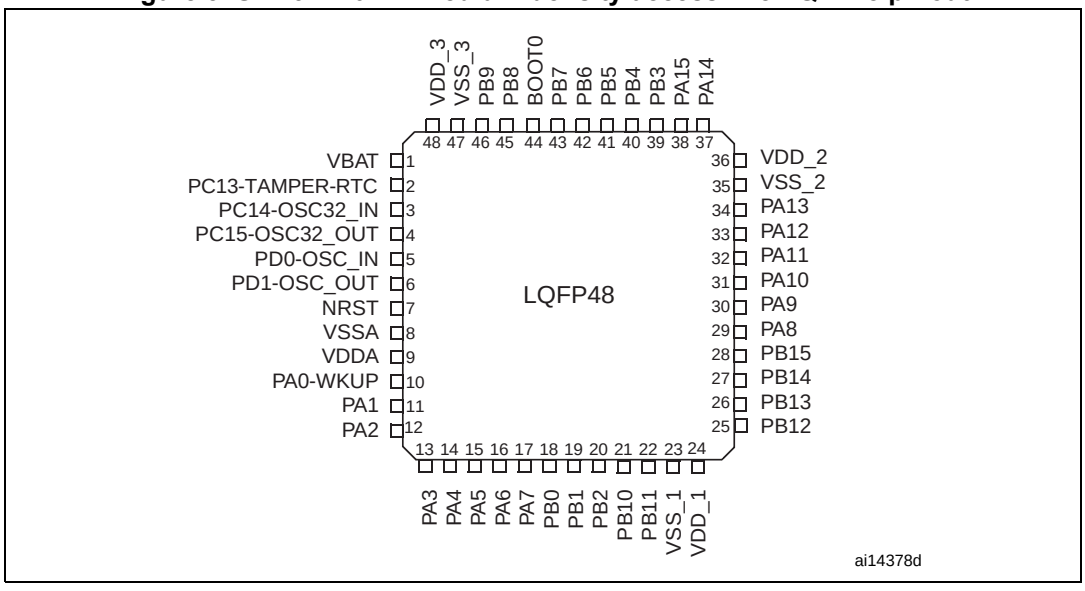


Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
35	47	74	26	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	75	27	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	76	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	77	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15/ SPI1_NSS
-	51	78	-	PC10	I/O	FT	PC10	-	USART3_TX
-	52	79	-	PC11	I/O	FT	PC11	-	USART3_RX
-	53	80	-	PC12	I/O	FT	PC12	-	USART3_CK
-	-	81	2	PD0	I/O	FT	PD0	-	-
-	-	82	3	PD1	I/O	FT	PD1	-	-
-	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	-
-	-	84	-	PD3	I/O	FT	PD3	-	USART2_CTS
-	-	85	-	PD4	I/O	FT	PD4	-	USART2_RTS
-	-	86	-	PD5	I/O	FT	PD5	-	USART2_TX
-	-	87	-	PD6	I/O	FT	PD6	-	USART2_RX
-	-	88	-	PD7	I/O	FT	PD7	-	USART2_CK
39	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK
40	56	90	31	PB4	I/O	FT	JNTRST	-	PB4 / TIM3_CH1 SPI1_MISO
41	57	91	32	PB5	I/O	-	PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL(8)/ TIM4_CH1 (8)	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA(8)/ TIM4_CH2 (8)	USART1_RX
44	60	94	35	BOOT0	I	-	BOOT0	-	-
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3 (8)	I2C1_SCL

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	36	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	36	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	

Figure 17. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

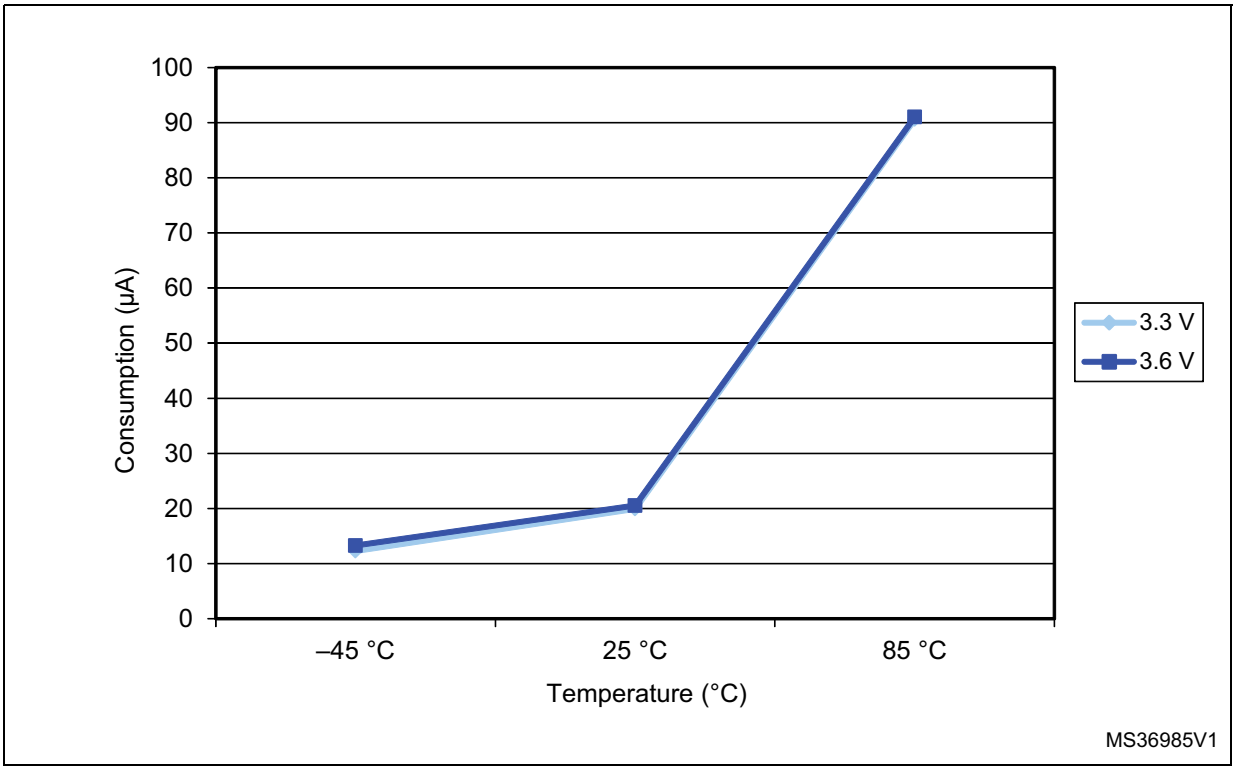


Figure 18. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V

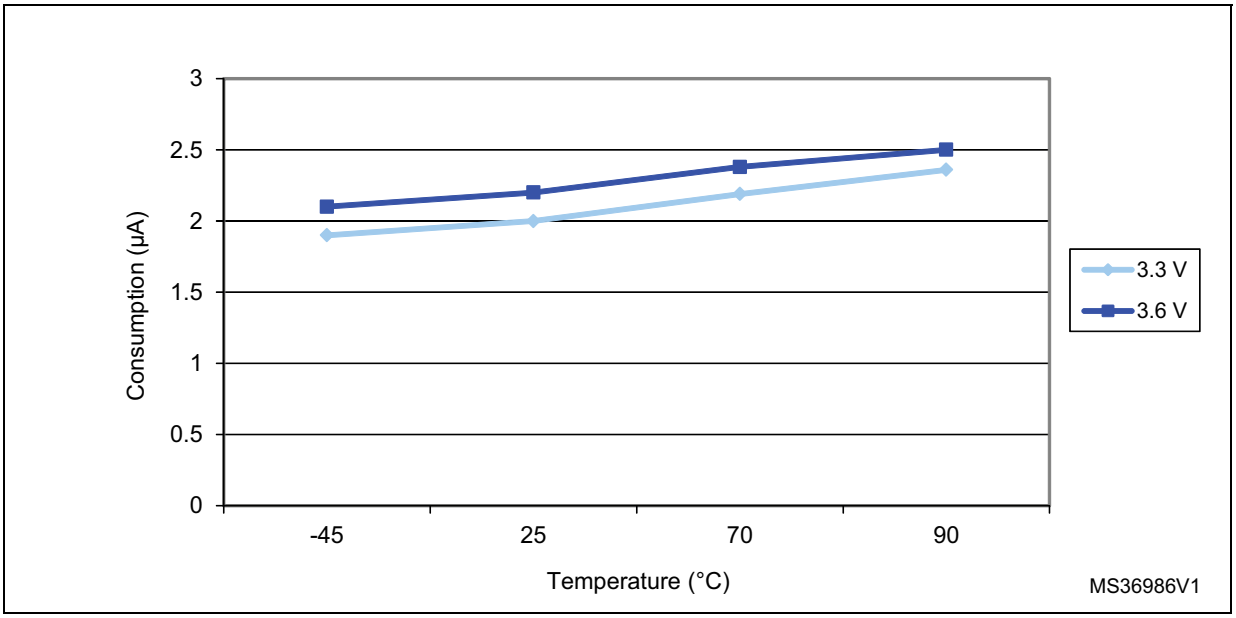


Table 26. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 28*. They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
		IO FT(3) input low level voltage	-	-	0.32*(V_{DD}-2 V)+0.75 V(1)	
		All I/Os except BOOT0	-	-	0.35V_{DD}(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	0.41*(V_{DD}-2 V)+1.3 V(1)	-	-	
		IO FT(3) input high level voltage	0.42*(V_{DD}-2 V)+1 V(1)	-	-	
		All I/Os except BOOT0	0.65V_{DD}(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Output voltage levels

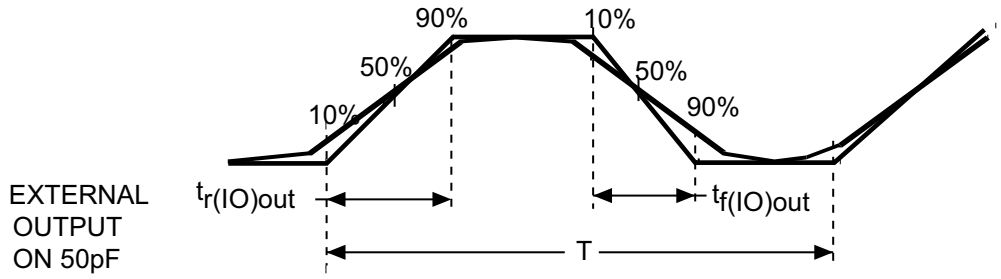
Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2),, I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Figure 27. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 33*).

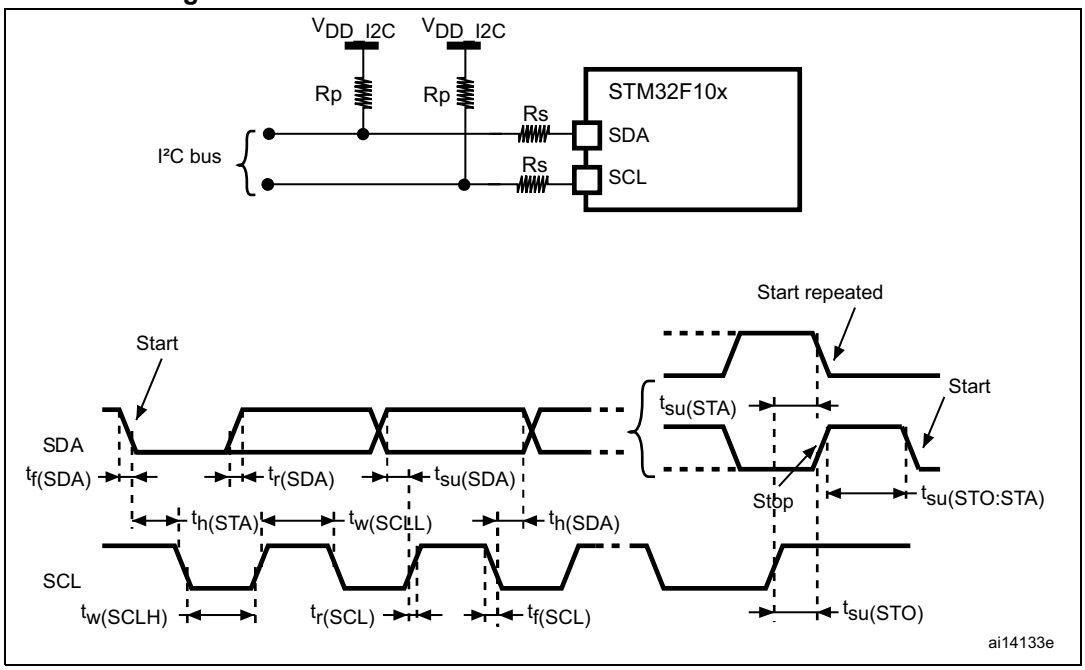
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 29. I²C bus AC waveforms and measurement circuit(1)



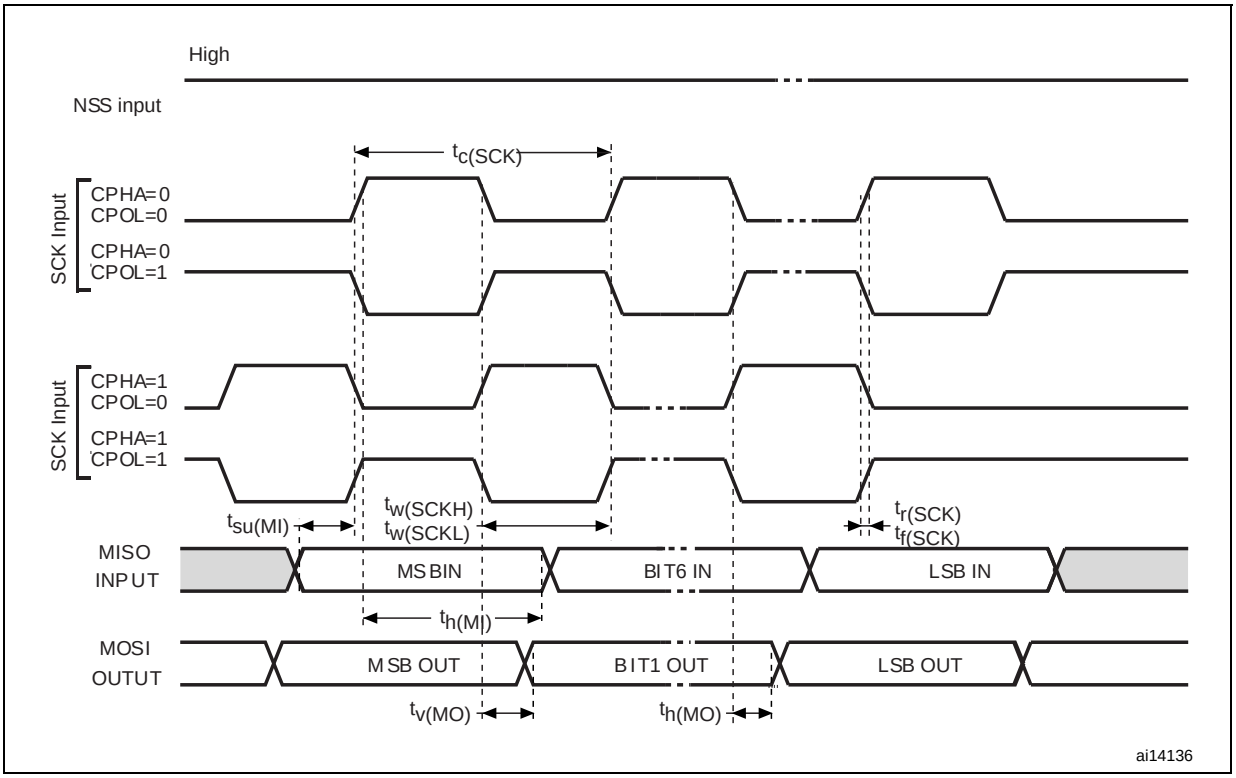
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 39. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 32. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 42. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

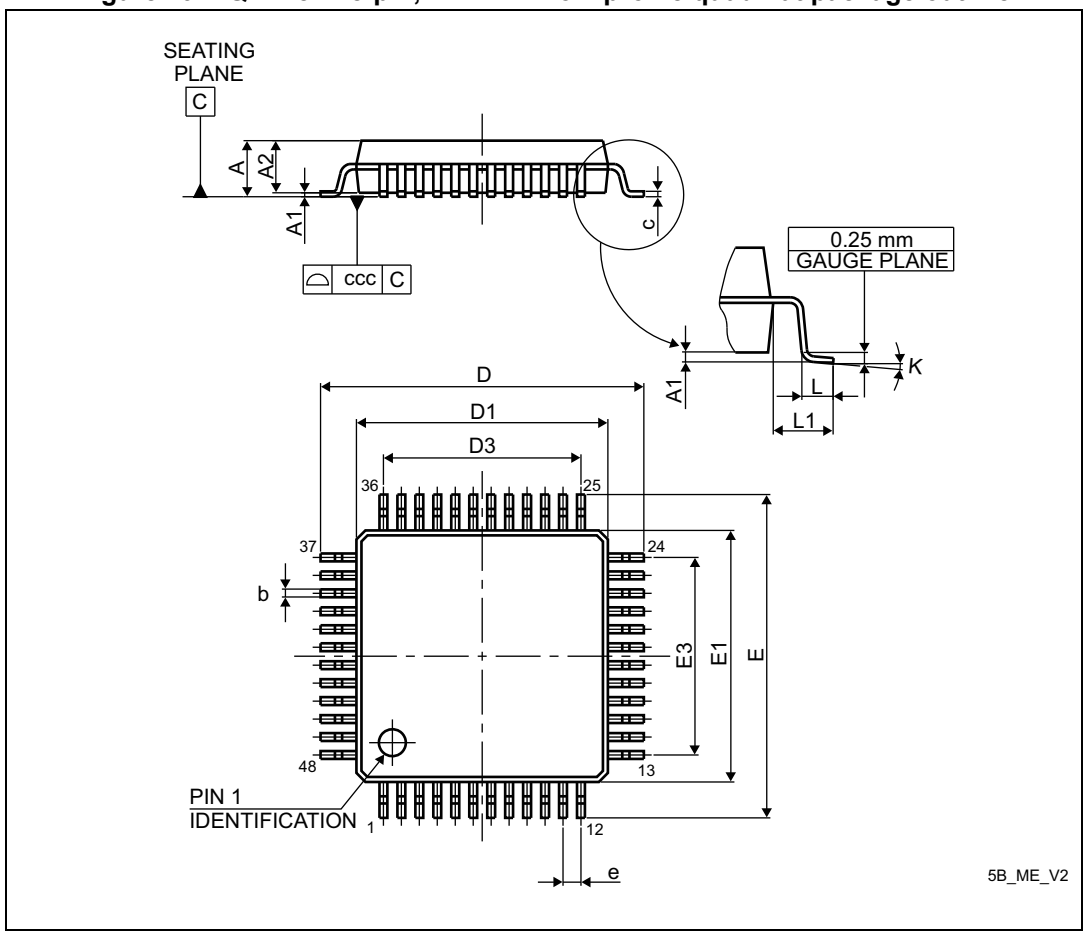
Table 43. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

6.6 LQFP48 package information

Figure 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	$V_{ESD(CDM)}$ value added to *Table 30: ESD absolute maximum ratings*. Note added below *Table 10: Embedded reset and power control block characteristics*. and below *Table 21: HSE 4-16 MHz oscillator characteristics*. Note added below *Table 34: Output voltage characteristics* and V_{OH} parameter description modified. *Table 41: ADC characteristics* and *Table 43: ADC accuracy - limited test conditions* modified. *Figure 33: ADC accuracy characteristics* modified. Packages are ECOPACK® compliant. Tables modified in *Section 5.3.5: Supply current characteristics*. ADC and ANTI_TAMPER signal names modified (see *Table 4: Medium-density STM32F101xx pin definitions*). *Table 4: Medium-density STM32F101xx pin definitions* modified. Note 4 removed and values updated in *Table 21: Typical current consumption in Standby mode*. V_{hys} modified in *Table 33: I/O static characteristics*. Updated: *Table 28: EMS characteristics* and *Table 29: EMI characteristics*. t_{VDD} modified in *Table 9: Operating conditions at power-up / power-down*. Typical values modified, note 2 modified and note 3 removed in *Table 25: Low-power mode wakeup timings*. Maximum current consumption *Table 12*, *Table 13* and *Table 14* updated. Values added and notes added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *On-chip peripheral current consumption on page 43* added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). V_{prog} added to *Table 27: Flash memory characteristics*. T_{S_temp} added to *Table 45: TS characteristics*. $T_{S\_vrefint}$ added to *Table 11: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 55*. All I/Os are CMOS and TTL compliant. *Table 4: Medium-density STM32F101xx pin definitions*: table clarified and *Note 7* modified. Internal LSI RC frequency changed from 32 to 40 kHz (see *Table 24: LSI oscillator characteristics*). Values added to *Table 25: Low-power mode wakeup timings*. N_{END} modified in *Table 27: Flash memory characteristics*. Option byte addresses corrected in *Figure 8: Memory map*. ACC_{HSI} modified in *Table 23: HSI oscillator characteristics*. t_{JITTER} removed from *Table 26: PLL characteristics*. *Appendix A: Important notes on page 71* added. Added: *Figure 13*, *Figure 14*, *Figure 16* and *Figure 18*.

Table 53. Document revision history (continued)

Date	Revision	Changes
22-Nov-2007	4	Document status promoted from preliminary data to datasheet. Small text changes. STM32F101CB part number corrected in *Table 1: Device summary*. Number of communication peripherals corrected for STM32F101Tx in *Table 2: Device features and peripheral counts (STM32F101xx medium-density access line)* and Number of GPIOs corrected for LQFP package. *Power supply schemes on page 16* modified. Main function and default alternate function modified for PC14 and PC15 in *Table 4: Medium-density STM32F101xx pin definitions*, *Note 6* added, Remap column added. *Figure 11: Power supply scheme* modified. $V_{DD} – V_{SS}$ ratings modified and *Note 1* modified in *Table 5: Voltage characteristics*. *Note 1* modified in *Table 6: Current characteristics*. *Note 2* added in *Table 10: Embedded reset and power control block characteristics*. 48 and 72 MHz frequencies removed from *Table 12*, *Table 13* and *Table 14*. MCU ‘s operating conditions modified in *Typical current consumption on page 42*. I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. Note added in *Table 16 on page 42* and *Table 17 on page 43*. *Table 18: Peripheral current consumption* modified. *Figure 17: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* added. Note removed below *Figure 30: SPI timing diagram - slave mode and CPHA = 0*. Note added below *Figure 31: SPI timing diagram - slave mode and CPHA = 1(1)*. *Figure 34: Typical connection diagram using the ADC* modified. $t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in *Table 21* and *Table 22*, respectively. Maximum values removed from *Table 25: Low-power mode wakeup timings*. t_{RET} conditions modified in *Table 27: Flash memory characteristics*. Conditions modified in *Table 28: EMS characteristics*. Impedance size specified in *A.4: Voltage glitch on ADC input 0 on page 71*. Small text changes in *Table 34: Output voltage characteristics*. *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)* updated. Details on unused pins removed from *General input/output characteristics on page 55*. *Table 40: SPI characteristics* updated. Notes added and I_{lkg} removed in *Table 41: ADC characteristics*. Note added in *Table 42* and *Table 45*. *Note 3* and *Note 2* added below *Table 43: ADC accuracy - limited test conditions*. Avg_Slope and V_{25} modified in *Table 45: TS characteristics*. Θ_{JA}value for VFQFPN36 package added in *Table 51: Package thermal characteristics*. *I2C interface characteristics on page 62* modified. Order codes replaced by *Section 7: Ordering information scheme*.

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	8	Small text changes. *Power supply supervisor on page 16* modified and V_{DDA} added to *Table 8: General operating conditions on page 33*. Capacitance modified in *Figure 11: Power supply scheme on page 31*. Table notes revised in *Section 5: Electrical characteristics*. Maximum value of $t_{RSTTEMPO}$ modified in *Table 10: Embedded reset and power control block characteristics on page 35*. Values added to *Table 15: Typical and maximum current consumptions in Stop and Standby modes* and *Table 21: Typical current consumption in Standby mode* removed. f_{HSE_ext} modified in *Table 19: High-speed external user clock characteristics on page 45*. f_{PLL_IN} modified in *Table 26: PLL characteristics on page 50*. f_{HCLK} corrected in *Table 28: EMS characteristics*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 38: I2C characteristics on page 63*, note 1 modified. $t_{h(NSS)}$ modified in *Table 40: SPI characteristics on page 65* and *Figure 30: SPI timing diagram - slave mode and CPHA = 0 on page 66*. C_{ADC} modified in *Table 41: ADC characteristics on page 68* and *Figure 34: Typical connection diagram using the ADC* modified. f_{PCLK2} corrected in *Table 43: ADC accuracy - limited test conditions* and *Table 44: ADC accuracy*. Typical T_{S_temp} value removed from *Table 45: TS characteristics on page 72*. LQFP48 package specifications updated (see *Table 50*, *Table 49* and *Table 50*). Axx option removed from *Table 52: Ordering information scheme on page 92*.
24-Jul-2008	9	First page modified: “Up to 2 x I²C interfaces” instead of “1 x I²C interface”
23-Sep-2008	10	STM32F101xx devices with 32 Kbyte Flash memory capacity removed, document updated accordingly. *Section 2.2: Full compatibility throughout the family on page 14* updated. Notes modified in *Table 4: Medium-density STM32F101xx pin definitions on page 24*. *Note 2* modified below *Table 5: Voltage characteristics on page 32*, $\lvert\Delta V_{DDx}\rvert$ min and $\lvert\Delta V_{DDx}\rvert$ min removed. *Note 2* added to *Table 8: General operating conditions on page 33*. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 36*. I_{DD} in standby mode at 85 °C modified in *Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 39*. *General input/output characteristics on page 55* modified. Note added below *Table 52: Ordering information scheme*. *Section 7.1: Future family enhancements* removed. Small text changes.