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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101r8t6

List of Figures

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Device features and peripheral counts (STM32F101xx medium-density access line)

Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx		STM32F101Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		10	16	10	16	10	16	10	16
Timers	General -purpose	3		3		3		3	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
12-bit synchronized ADC number of channels		110 channels		110 channels		116 channels		116 channels	
GPIOs		26		37		51		80	
CPU frequency		36 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64		LQFP100	

Figure 6. STM32F101xx medium-density access line UFQPFN48 pinout

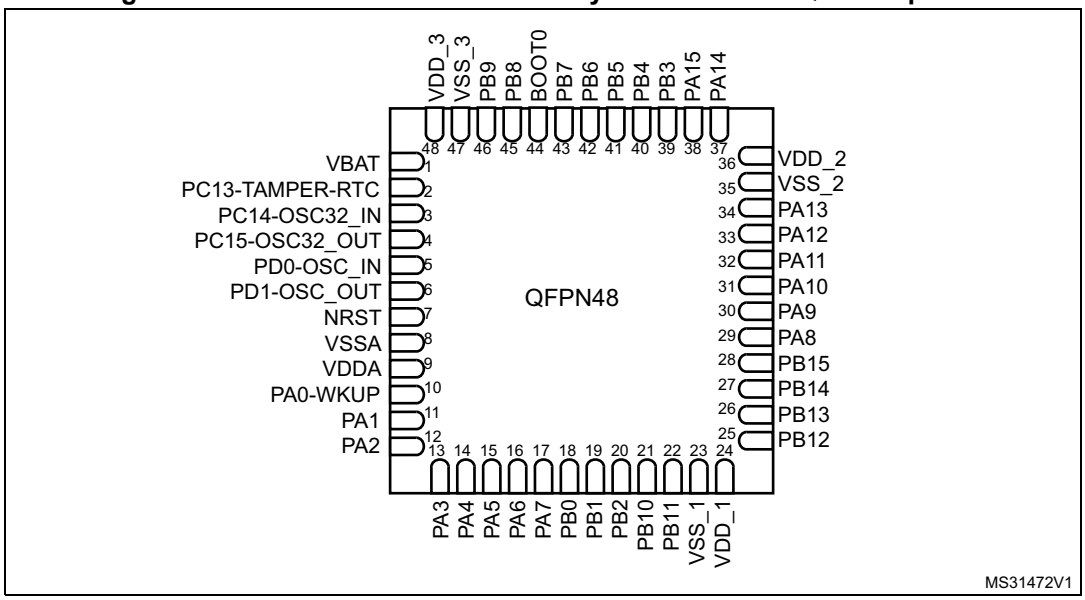


Figure 7. STM32F101xx medium-density access line VFQPFN36 pinout

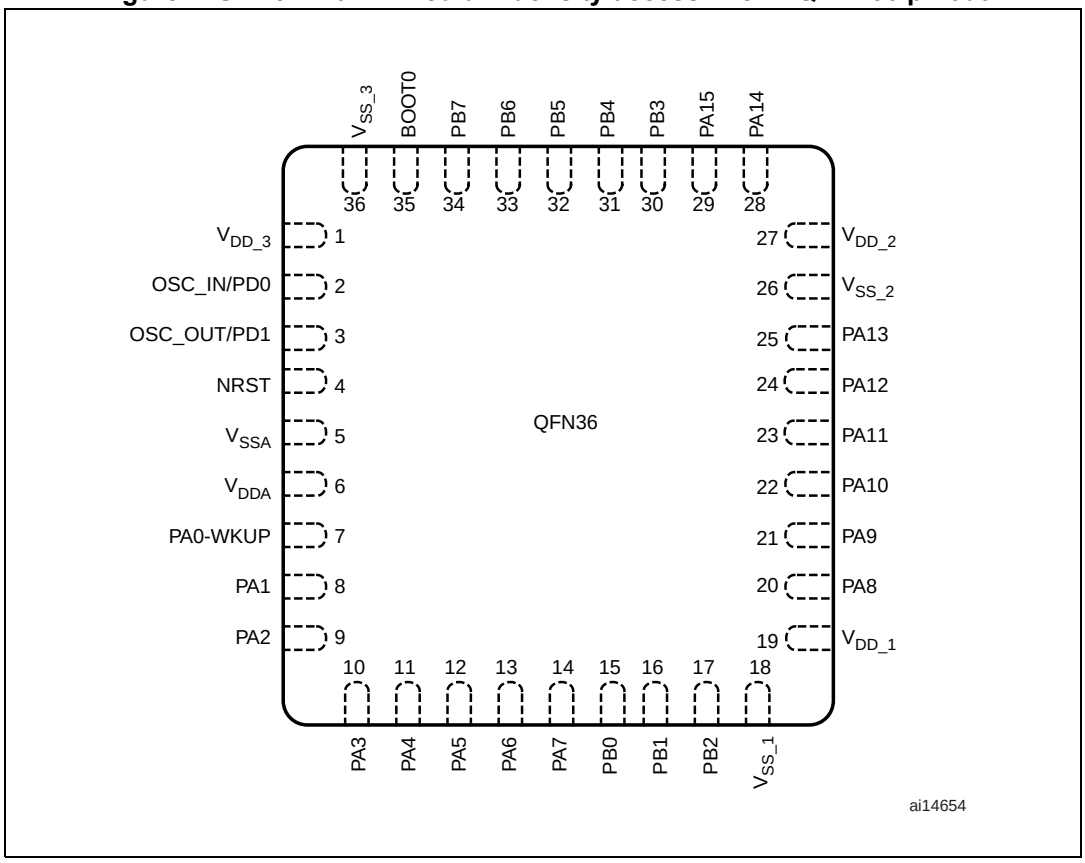


Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
23	31	49	18	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	50	19	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA / USART3_CK (8)	-
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(8)	-
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(8)	-
28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	-	55	-	PD8	I/O	FT	PD8	-	USART3_TX
-	-	56	-	PD9	I/O	FT	PD9	-	USART3_RX
-	-	57	-	PD10	I/O	FT	PD10	-	USART3_CK
-	-	58	-	PD11	I/O	FT	PD11	-	USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13	-	TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14	-	TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15	-	TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	64	-	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	65	-	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS	-
33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS	-
34	46	72	25	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	-	73	-	Not connected					-

Figure 9. Pin loading conditions

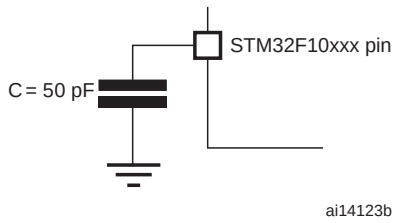
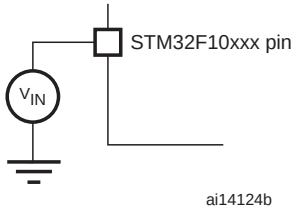
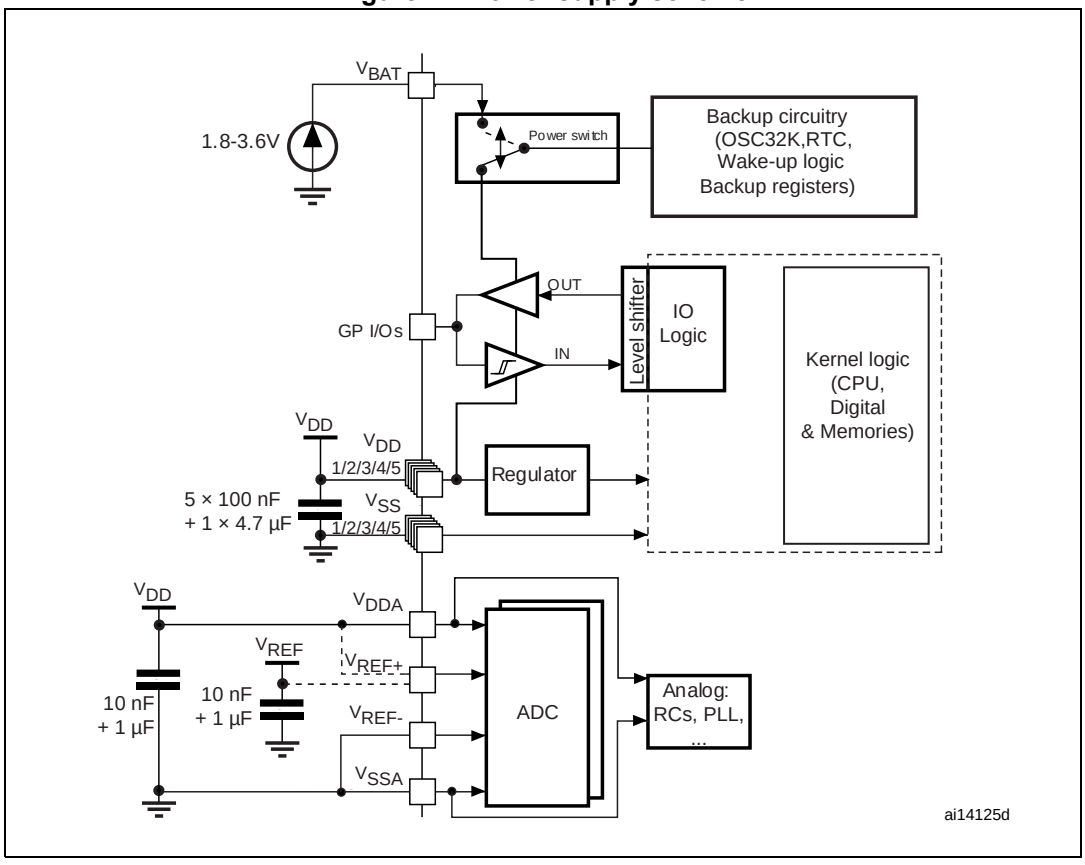


Figure 10. Pin input voltage



5.1.6 Power supply scheme

Figure 11. Power supply scheme



Caution: In *Figure 11*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
AHB (up to 36 MHz)	DMA1	16.53	µA/MHz
	BusMatrix(2)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	10.28	
	TIM2	32.50	
	TIM3	31.39	
	TIM4	31.94	
	SPI2	4.17	
	USART2	12.22	
	USART3	12.22	
	I2C1	10.00	
	I2C2	10.00	
	WWDG	2.50	
	PWR	1.67	
	BKP	2.50	
	IWDG	11.67	
APB2 (up to 36 MHz)	APB2-Bridge	3.75	
	GPIO A	6.67	
	GPIO B	6.53	
	GPIO C	6.53	
	GPIO D	6.53	
	GPIO E	6.39	
	ADC1(3)	17.50	
	SPI1	4.72	
	USART1	11.94	

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, the consumption added is equal to 0.65 mA. When the ADC is enabled, a current consumption is added equal to 0.05 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

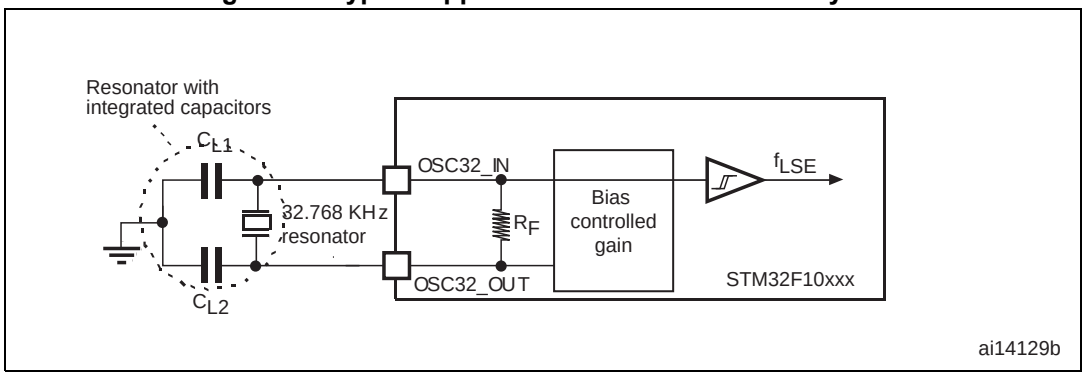
The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 22. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated (4) (5)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

The test results are given in *Table 28*. They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 23* and *Figure 24* for standard I/Os, and in *Figure 25* and *Figure 26* for 5 V tolerant I/Os.

Figure 23. Standard I/O input characteristics - CMOS port

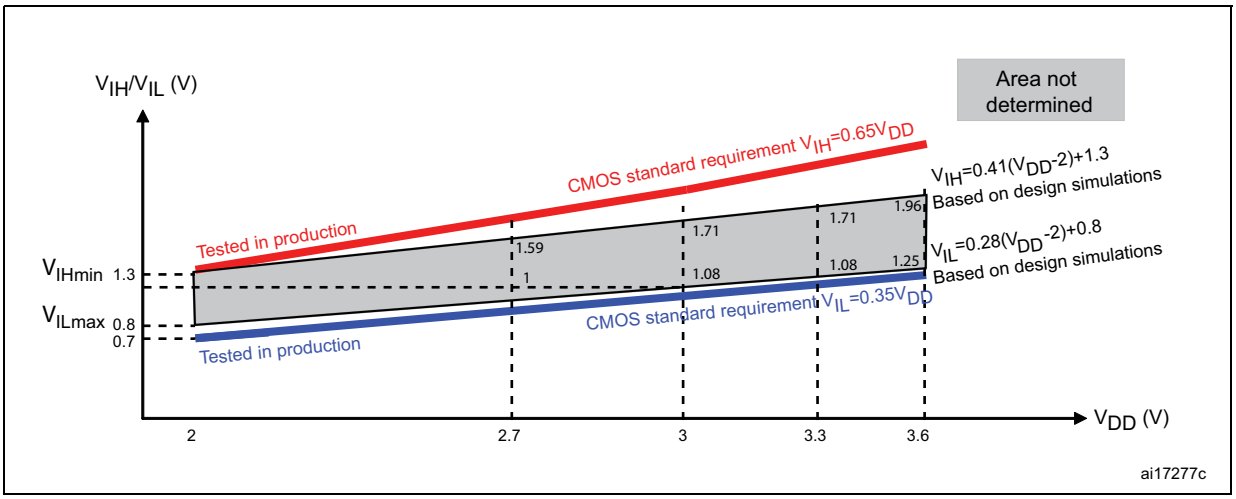


Figure 24. Standard I/O input characteristics - TTL port

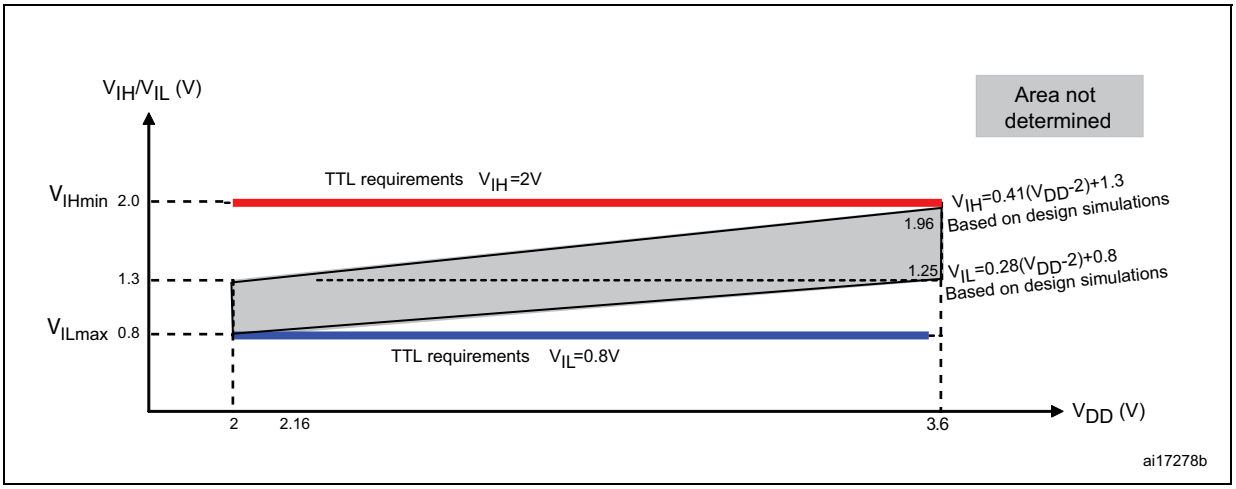
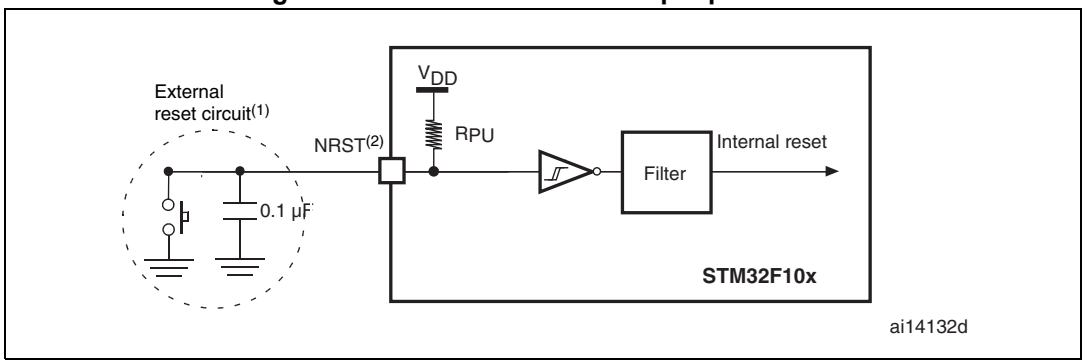


Figure 28. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

Figure 30. SPI timing diagram - slave mode and CPHA = 0

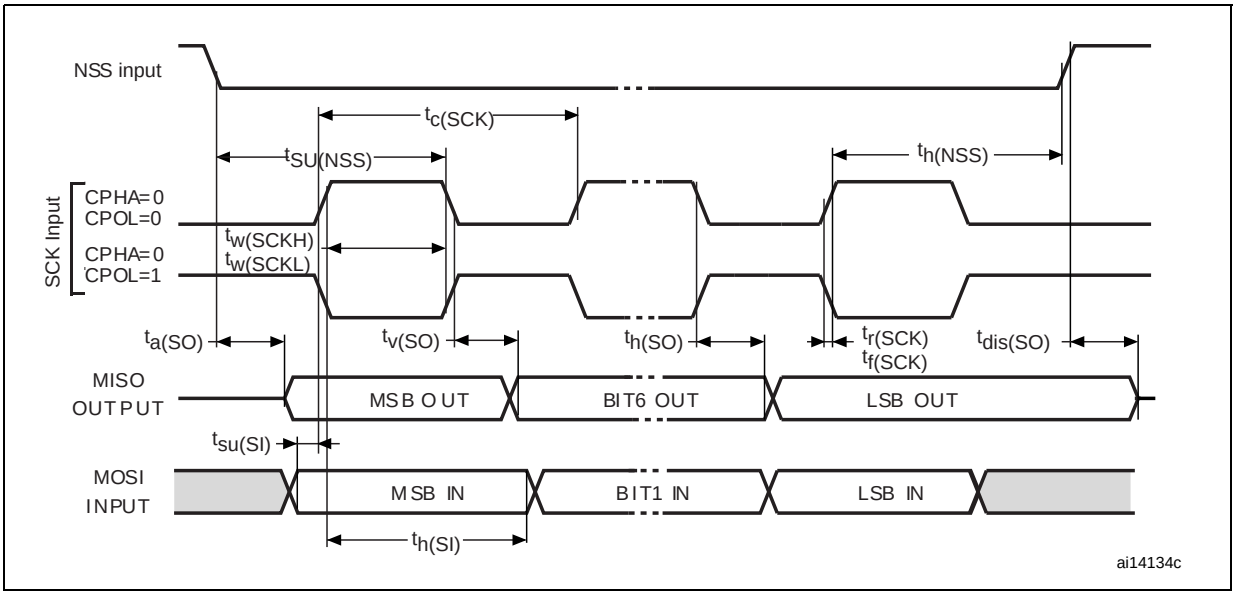
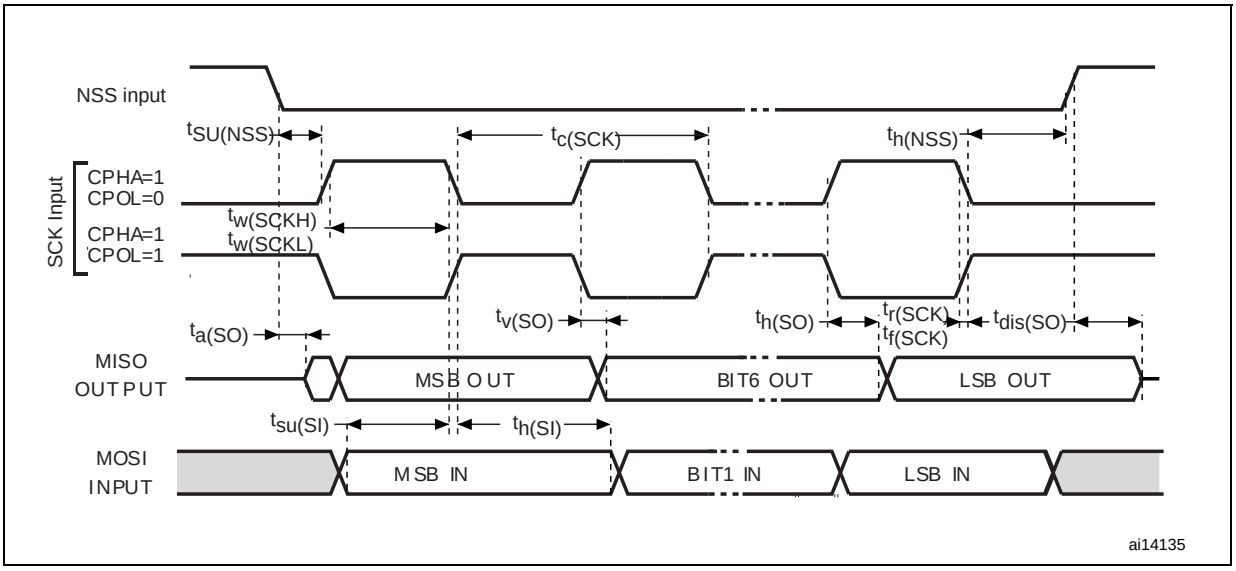


Figure 31. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 42. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

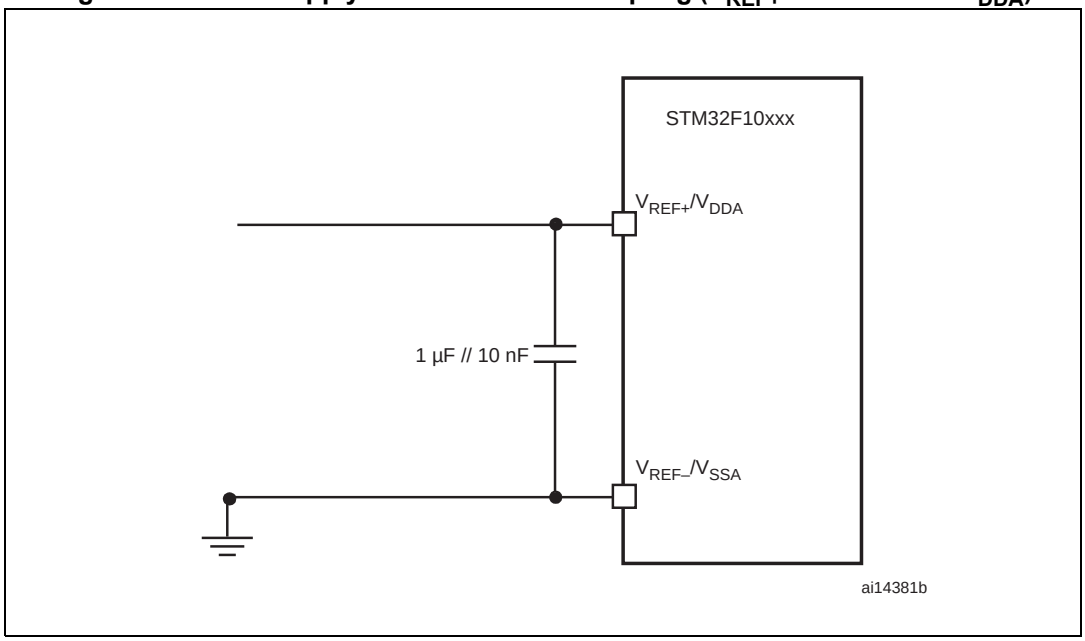
1. Guaranteed by design, not tested in production.

Table 43. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 45. TS characteristics

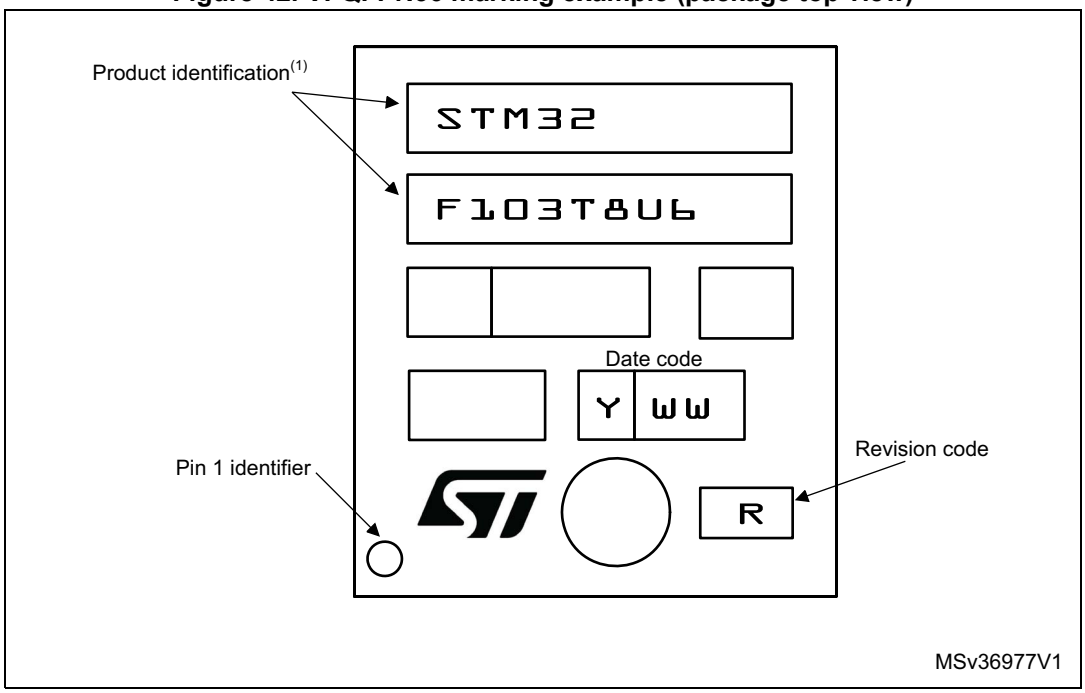
Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. VFQFPN36 marking example (package top view)

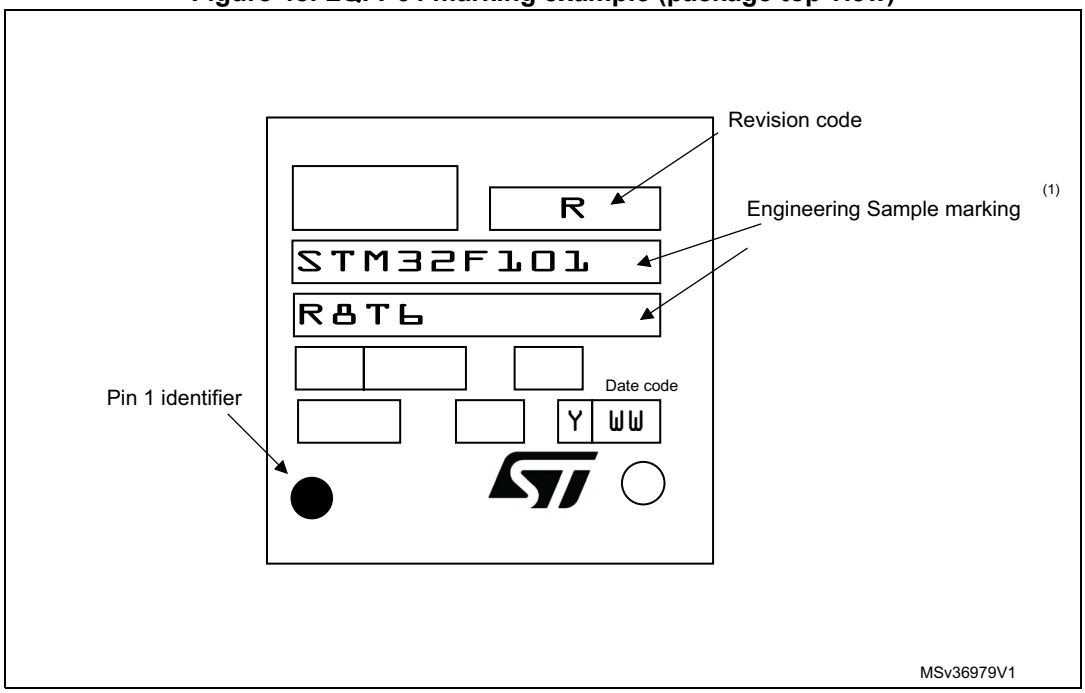


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device Marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 48. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Ordering information scheme

Table 52. Ordering information scheme

Example: STM32 F 101 C 8 T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size(1)

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

T = LQFP

U = VFQFPN or UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Options

xxx = programmed parts

TR = tape and real

1. Although STM32F101x6 devices are not described in this datasheet, orderable part numbers that do not show the A internal code after temperature range code 6 should be referred to this datasheet for the electrical characteristics. The low-density datasheet only covers STM32F101x6 devices that feature the A code.

Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	$V_{ESD(CDM)}$ value added to *Table 30: ESD absolute maximum ratings*. Note added below *Table 10: Embedded reset and power control block characteristics*. and below *Table 21: HSE 4-16 MHz oscillator characteristics*. Note added below *Table 34: Output voltage characteristics* and V_{OH} parameter description modified. *Table 41: ADC characteristics* and *Table 43: ADC accuracy - limited test conditions* modified. *Figure 33: ADC accuracy characteristics* modified. Packages are ECOPACK® compliant. Tables modified in *Section 5.3.5: Supply current characteristics*. ADC and ANTI_TAMPER signal names modified (see *Table 4: Medium-density STM32F101xx pin definitions*). *Table 4: Medium-density STM32F101xx pin definitions* modified. Note 4 removed and values updated in *Table 21: Typical current consumption in Standby mode*. V_{hys} modified in *Table 33: I/O static characteristics*. Updated: *Table 28: EMS characteristics* and *Table 29: EMI characteristics*. t_{VDD} modified in *Table 9: Operating conditions at power-up / power-down*. Typical values modified, note 2 modified and note 3 removed in *Table 25: Low-power mode wakeup timings*. Maximum current consumption *Table 12*, *Table 13* and *Table 14* updated. Values added and notes added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *On-chip peripheral current consumption on page 43* added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). V_{prog} added to *Table 27: Flash memory characteristics*. T_{S_temp} added to *Table 45: TS characteristics*. $T_{S\_vrefint}$ added to *Table 11: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 55*. All I/Os are CMOS and TTL compliant. *Table 4: Medium-density STM32F101xx pin definitions*: table clarified and *Note 7* modified. Internal LSI RC frequency changed from 32 to 40 kHz (see *Table 24: LSI oscillator characteristics*). Values added to *Table 25: Low-power mode wakeup timings*. N_{END} modified in *Table 27: Flash memory characteristics*. Option byte addresses corrected in *Figure 8: Memory map*. ACC_{HSI} modified in *Table 23: HSI oscillator characteristics*. t_{JITTER} removed from *Table 26: PLL characteristics*. *Appendix A: Important notes on page 71* added. Added: *Figure 13*, *Figure 14*, *Figure 16* and *Figure 18*.

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Apr-2009	11	I/O information clarified *on page 1*. *Figure 8: Memory map* modified. In *Table 4: Medium-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 16*, *Figure 17* and *Figure 18* show typical curves. *Table 19: High-speed external user clock characteristics* and *Table 20: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 23: HSI oscillator characteristics*. Small text changes.
22-Sep-2009	12	*Note 5* updated and *Note 4* added in *Table 4: Medium-density STM32F101xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 11: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 15: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 19: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*. *Figure 28: Recommended NRST pin protection* modified. *Note 1* modified below *Figure 21: Typical application with an 8 MHz crystal*. *Figure 28: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 51*. Jitter added to *Table 26: PLL characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 41: ADC characteristics*. R_{AIN} max values modified in *Table 42: RAIN max for fADC = 14 MHz*. Small text changes.
20-May-2010	13	Added STM32F101TB devices. Added VFQFPN48 package. Updated note 2 below *Table 38: I2C characteristics* Updated *Figure 29: I2C bus AC waveforms and measurement circuit(1)* Updated *Figure 28: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*