Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101r8t6tr

2 Description

The STM32F101xB and STM32F101x8 medium-density access line family incorporates the high-performance ARM® Cortex® -M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I^2Cs, two SPIs, and up to three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F101xx medium-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx medium-density access line family includes devices in four different packages ranging from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx medium-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Device features and peripheral counts (STM32F101xx medium-density access line)

Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx		STM32F101Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		10	16	10	16	10	16	10	16
Timers	General -purpose	3		3		3		3	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
12-bit synchronized ADC number of channels		110 channels		110 channels		116 channels		116 channels	
GPIOs		26		37		51		80	
CPU frequency		36 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64		LQFP100	

Figure 6. STM32F101xx medium-density access line UFQPFN48 pinout

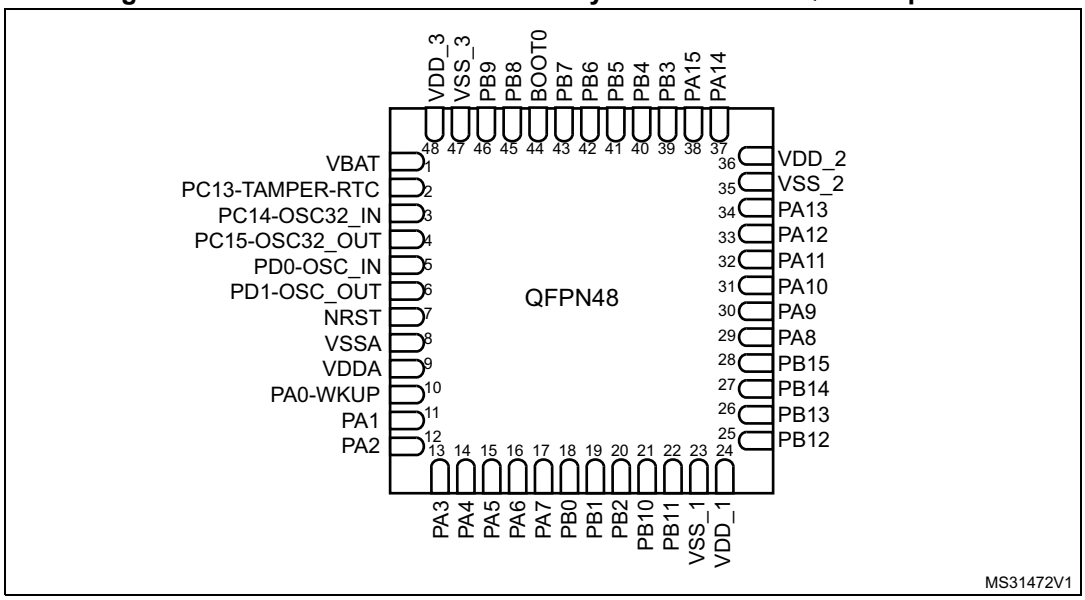


Figure 7. STM32F101xx medium-density access line VFQPFN36 pinout

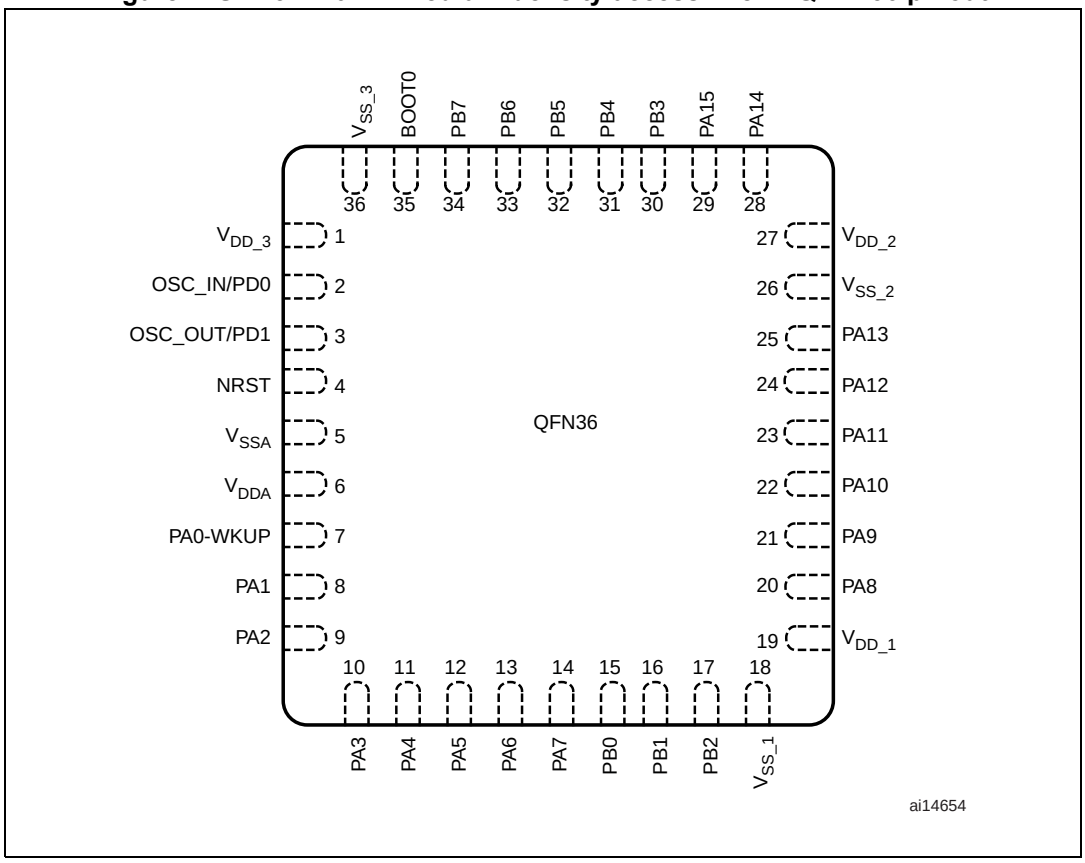


Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
23	31	49	18	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	50	19	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA / USART3_CK (8)	-
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(8)	-
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(8)	-
28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	-	55	-	PD8	I/O	FT	PD8	-	USART3_TX
-	-	56	-	PD9	I/O	FT	PD9	-	USART3_RX
-	-	57	-	PD10	I/O	FT	PD10	-	USART3_CK
-	-	58	-	PD11	I/O	FT	PD11	-	USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13	-	TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14	-	TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15	-	TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	64	-	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	65	-	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS	-
33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS	-
34	46	72	25	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	-	73	-	Not connected					-

Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
35	47	74	26	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	75	27	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	76	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	77	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15/ SPI1_NSS
-	51	78	-	PC10	I/O	FT	PC10	-	USART3_TX
-	52	79	-	PC11	I/O	FT	PC11	-	USART3_RX
-	53	80	-	PC12	I/O	FT	PC12	-	USART3_CK
-	-	81	2	PD0	I/O	FT	PD0	-	-
-	-	82	3	PD1	I/O	FT	PD1	-	-
-	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	-
-	-	84	-	PD3	I/O	FT	PD3	-	USART2_CTS
-	-	85	-	PD4	I/O	FT	PD4	-	USART2_RTS
-	-	86	-	PD5	I/O	FT	PD5	-	USART2_TX
-	-	87	-	PD6	I/O	FT	PD6	-	USART2_RX
-	-	88	-	PD7	I/O	FT	PD7	-	USART2_CK
39	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK
40	56	90	31	PB4	I/O	FT	JNTRST	-	PB4 / TIM3_CH1 SPI1_MISO
41	57	91	32	PB5	I/O	-	PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL(8)/ TIM4_CH1 (8)	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA(8)/ TIM4_CH2 (8)	USART1_RX
44	60	94	35	BOOT0	I	-	BOOT0	-	-
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3 (8)	I2C1_SCL

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	28.6	mA
			24 MHz	19.9	
			16 MHz	14.7	
			8 MHz	8.6	
		External clock (2), all peripherals Disabled	36 MHz	19.8	
			24 MHz	13.9	
			16 MHz	10.7	
			8 MHz	6.8	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	24	mA
			24 MHz	17.5	
			16 MHz	12.5	
			8 MHz	7.5	
		External clock(2) all peripherals disabled	36 MHz	16	
			24 MHz	11.5	
			16 MHz	8.5	
			8 MHz	5.5	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 15. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

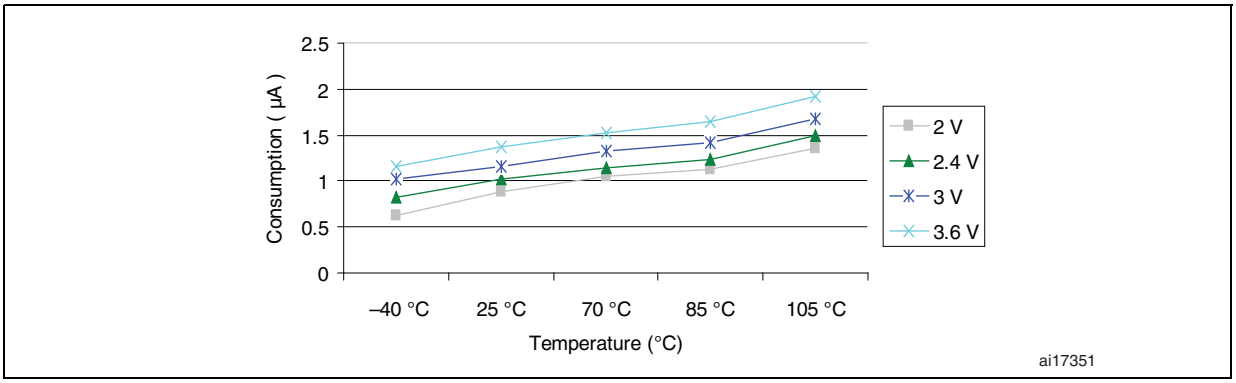


Figure 16. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

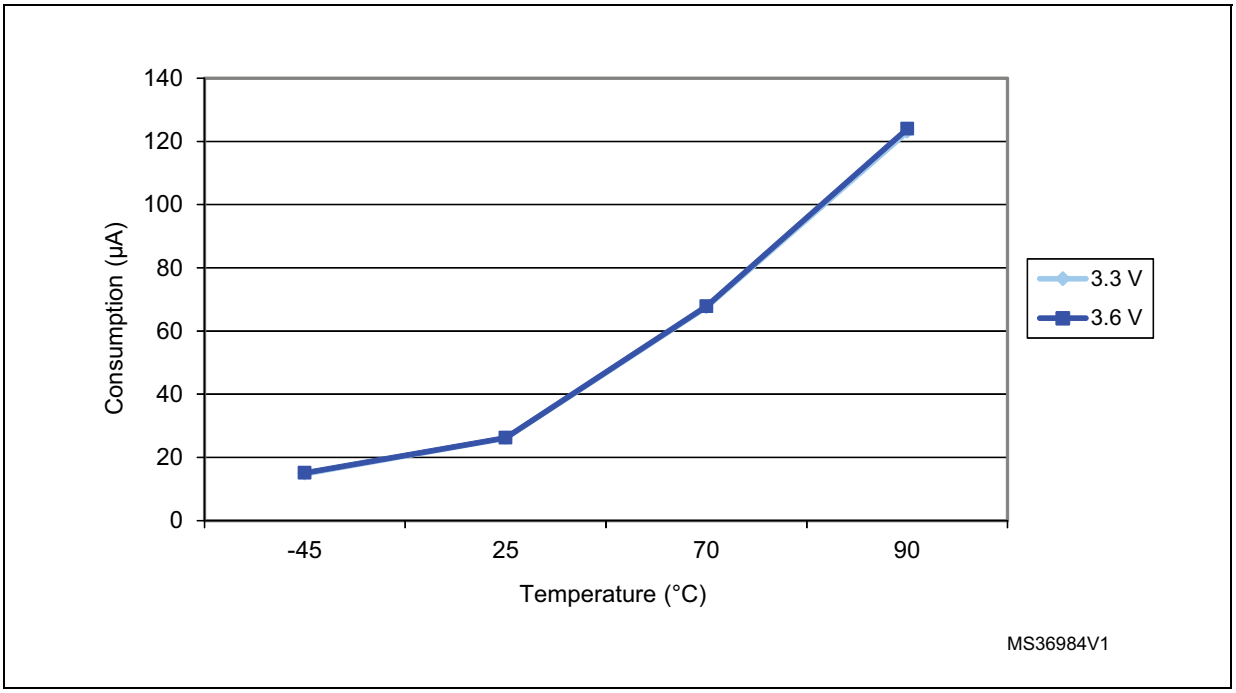


Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
AHB (up to 36 MHz)	DMA1	16.53	µA/MHz
	BusMatrix(2)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	10.28	
	TIM2	32.50	
	TIM3	31.39	
	TIM4	31.94	
	SPI2	4.17	
	USART2	12.22	
	USART3	12.22	
	I2C1	10.00	
	I2C2	10.00	
	WWDG	2.50	
	PWR	1.67	
	BKP	2.50	
	IWDG	11.67	
APB2 (up to 36 MHz)	APB2-Bridge	3.75	
	GPIO A	6.67	
	GPIO B	6.53	
	GPIO C	6.53	
	GPIO D	6.53	
	GPIO E	6.39	
	ADC1(3)	17.50	
	SPI1	4.72	
	USART1	11.94	

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, the consumption added is equal to 0.65 mA. When the ADC is enabled, a current consumption is added equal to 0.05 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Figure 19. High-speed external clock source AC timing diagram

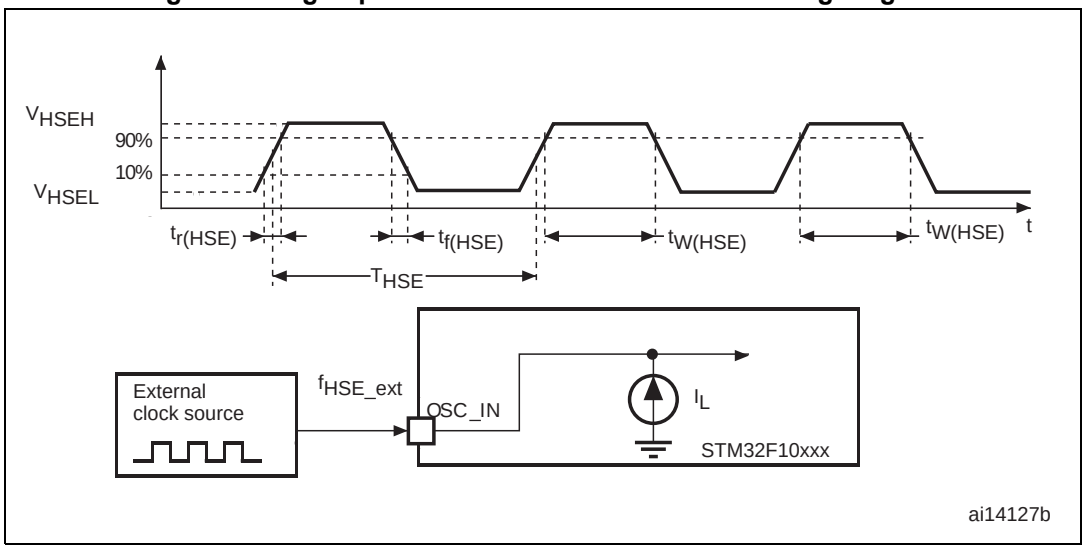
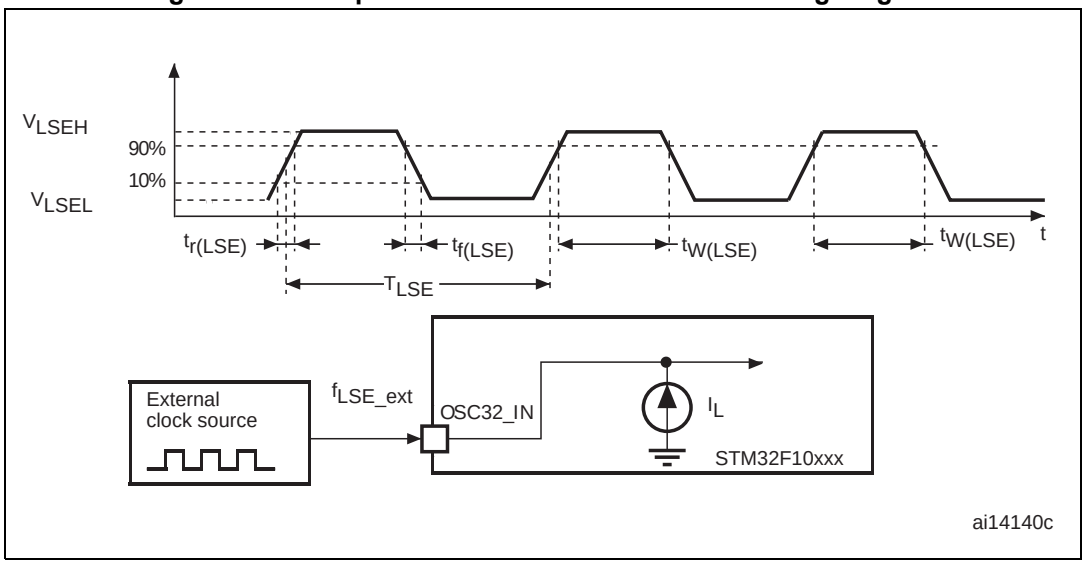


Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

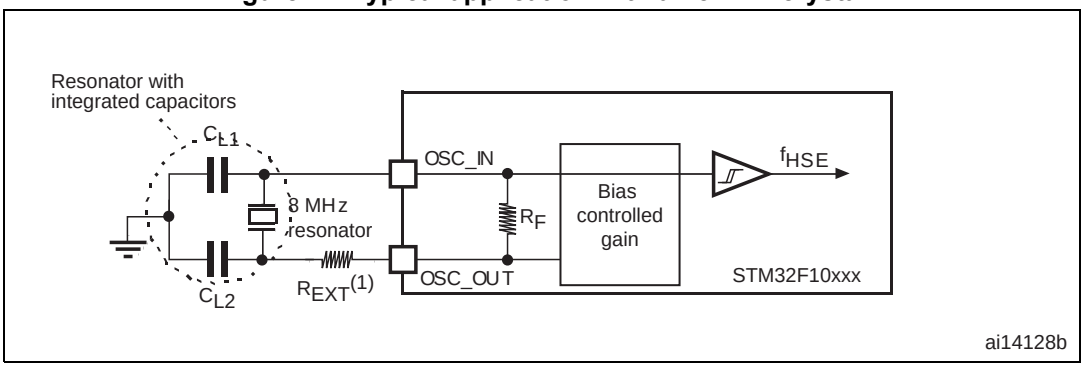
Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	0.28*(V_{DD}-2 V)+0.8 V(1)	V
		IO FT(3) input low level voltage	-	-	0.32*(V_{DD}-2 V)+0.75 V(1)	
		All I/Os except BOOT0	-	-	0.35V_{DD}(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	0.41*(V_{DD}-2 V)+1.3 V(1)	-	-	
		IO FT(3) input high level voltage	0.42*(V_{DD}-2 V)+1 V(1)	-	-	
		All I/Os except BOOT0	0.65V_{DD}(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

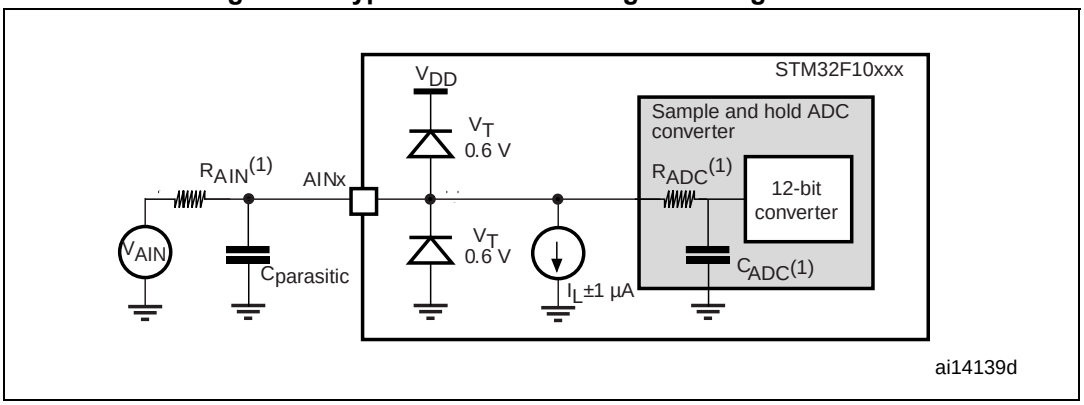
Note: It is recommended to perform a calibration after each power-up.

Table 41. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 42* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin description* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 41*.

Figure 34. Typical connection diagram using the ADC

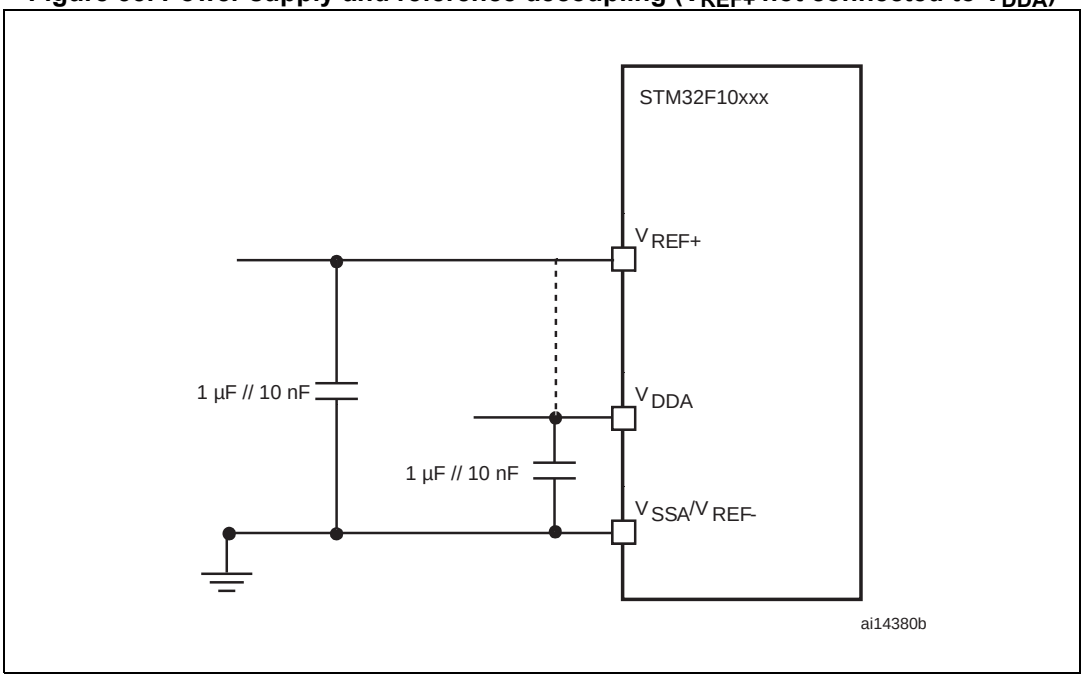


1. Refer to *Table 41* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 35* or *Figure 36*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

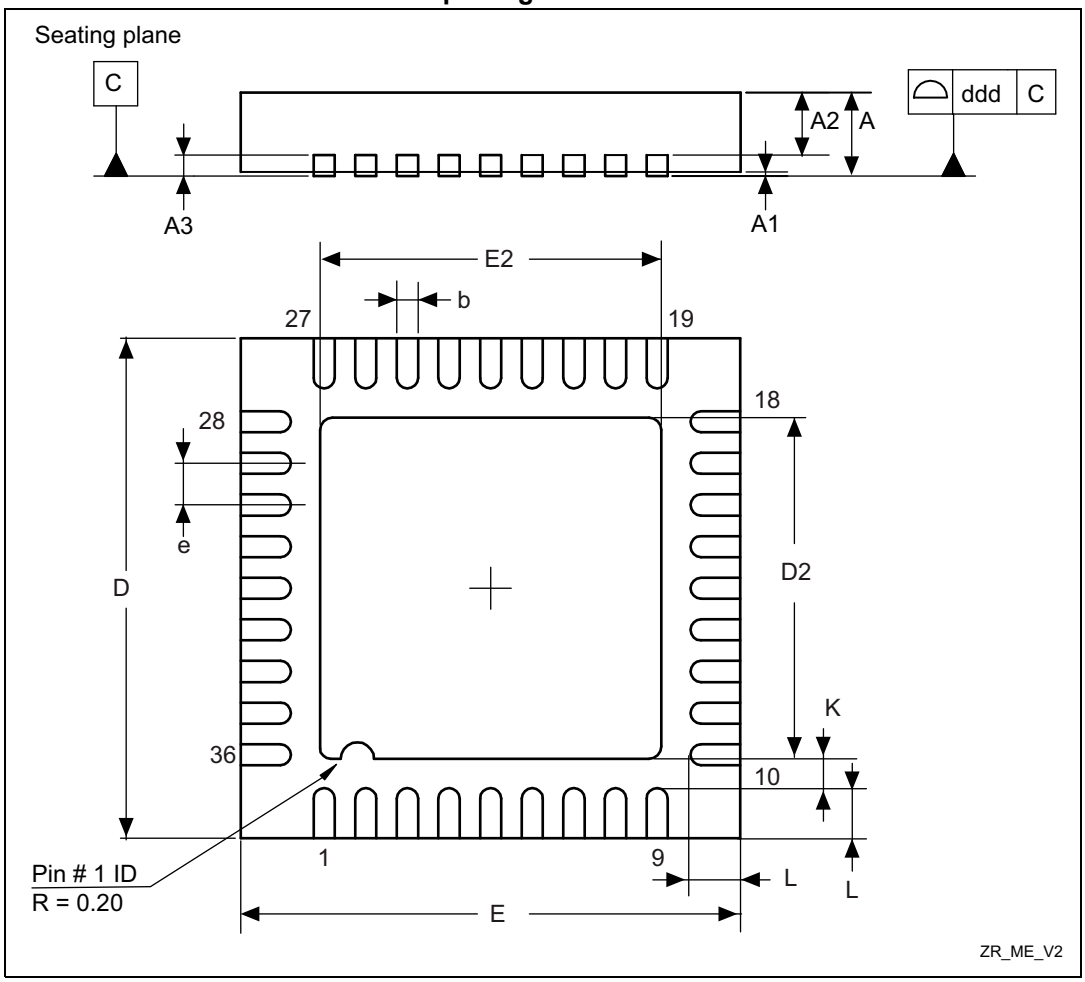
Figure 35. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

6.3 VFQFPN36 package information

Figure 40. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline

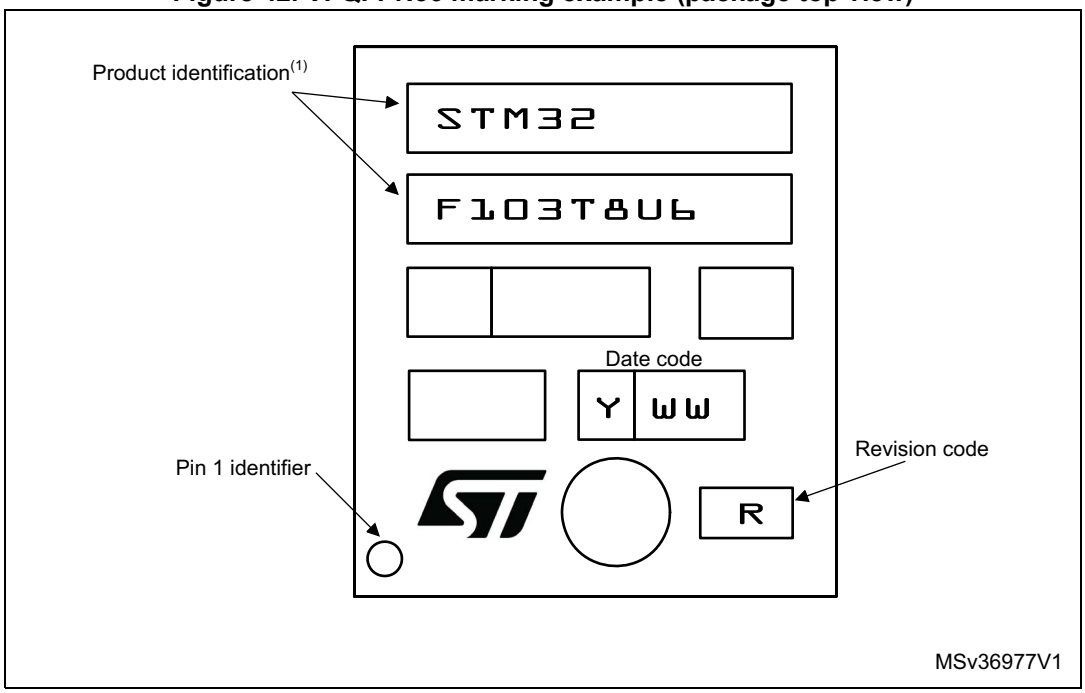


1. Drawing is not to scale.

Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. VFQFPN36 marking example (package top view)

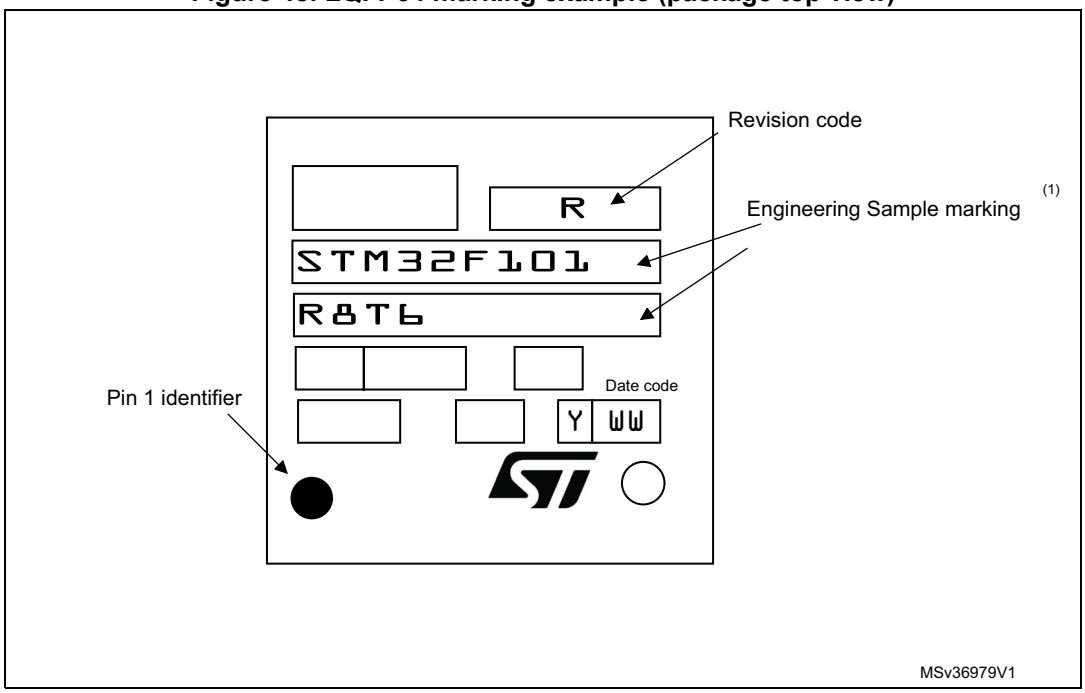


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device Marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 48. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Apr-2009	11	I/O information clarified *on page 1*. *Figure 8: Memory map* modified. In *Table 4: Medium-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 16*, *Figure 17* and *Figure 18* show typical curves. *Table 19: High-speed external user clock characteristics* and *Table 20: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 23: HSI oscillator characteristics*. Small text changes.
22-Sep-2009	12	*Note 5* updated and *Note 4* added in *Table 4: Medium-density STM32F101xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 11: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 15: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 19: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*. *Figure 28: Recommended NRST pin protection* modified. *Note 1* modified below *Figure 21: Typical application with an 8 MHz crystal*. *Figure 28: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 51*. Jitter added to *Table 26: PLL characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 41: ADC characteristics*. R_{AIN} max values modified in *Table 42: RAIN max for fADC = 14 MHz*. Small text changes.
20-May-2010	13	Added STM32F101TB devices. Added VFQFPN48 package. Updated note 2 below *Table 38: I2C characteristics* Updated *Figure 29: I2C bus AC waveforms and measurement circuit(1)* Updated *Figure 28: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*