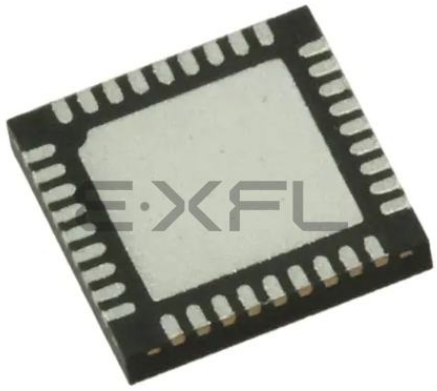

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-VFQFPN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101t8u6tr

Contents

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There are three synchronizable general-purpose timers embedded in the STM32F101xx medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
23	31	49	18	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	50	19	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA / USART3_CK (8)	-
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(8)	-
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(8)	-
28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	-	55	-	PD8	I/O	FT	PD8	-	USART3_TX
-	-	56	-	PD9	I/O	FT	PD9	-	USART3_RX
-	-	57	-	PD10	I/O	FT	PD10	-	USART3_CK
-	-	58	-	PD11	I/O	FT	PD11	-	USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13	-	TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14	-	TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15	-	TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	64	-	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	65	-	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS	-
33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS	-
34	46	72	25	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	-	73	-	Not connected					-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	36	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	36	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	

Figure 15. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

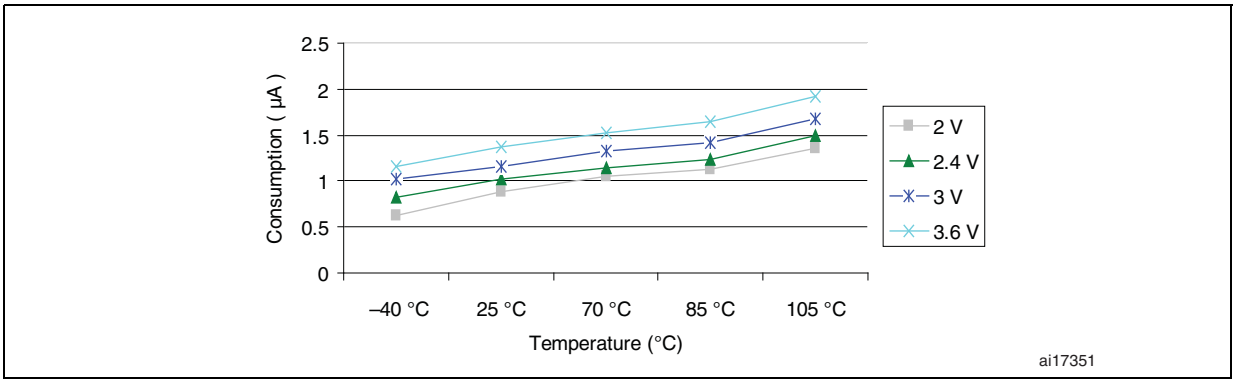


Figure 16. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

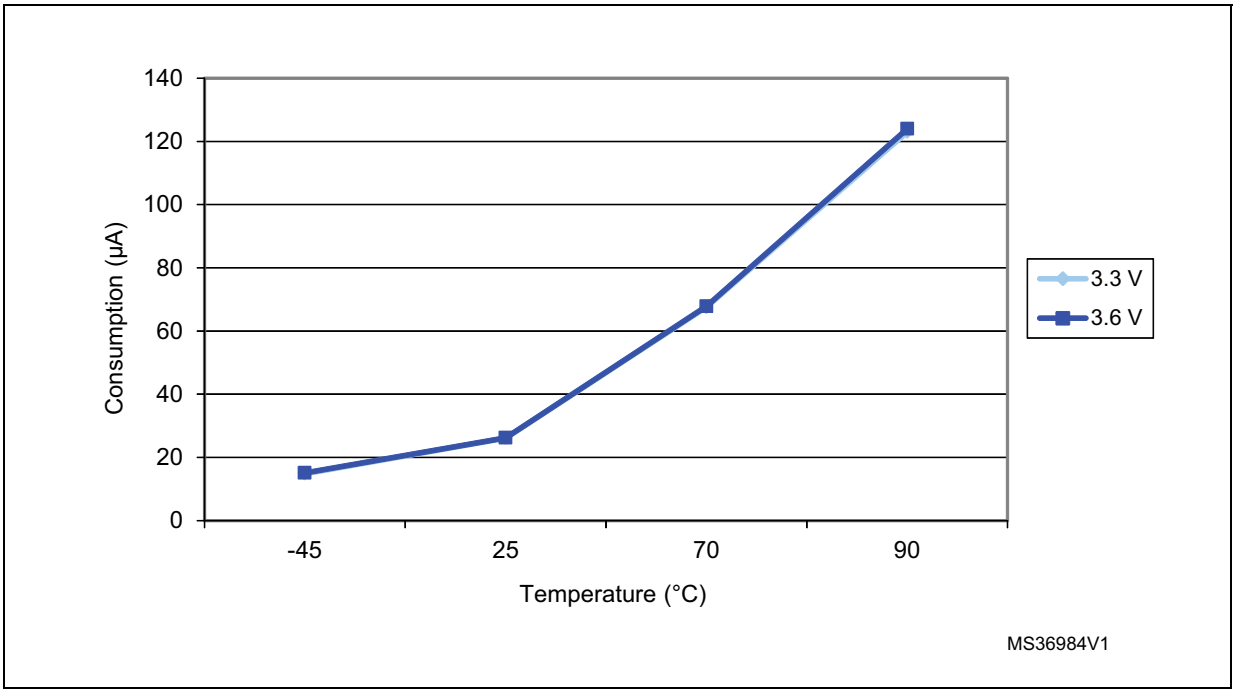


Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
AHB (up to 36 MHz)	DMA1	16.53	µA/MHz
	BusMatrix(2)	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	10.28	
	TIM2	32.50	
	TIM3	31.39	
	TIM4	31.94	
	SPI2	4.17	
	USART2	12.22	
	USART3	12.22	
	I2C1	10.00	
	I2C2	10.00	
	WWDG	2.50	
	PWR	1.67	
	BKP	2.50	
	IWDG	11.67	
APB2 (up to 36 MHz)	APB2-Bridge	3.75	
	GPIO A	6.67	
	GPIO B	6.53	
	GPIO C	6.53	
	GPIO D	6.53	
	GPIO E	6.39	
	ADC1(3)	17.50	
	SPI1	4.72	
	USART1	11.94	

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, the consumption added is equal to 0.65 mA. When the ADC is enabled, a current consumption is added equal to 0.05 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Figure 19. High-speed external clock source AC timing diagram

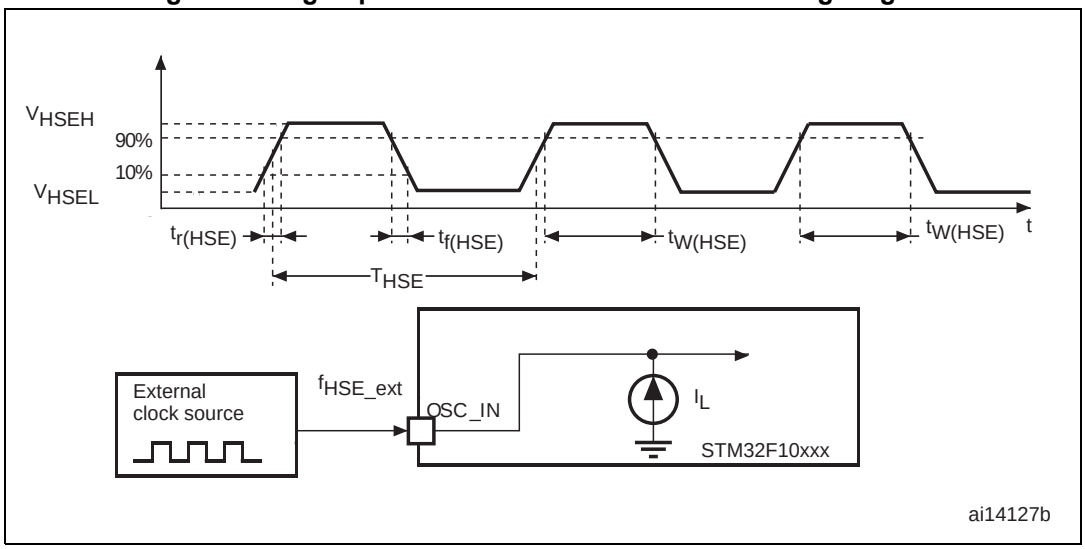
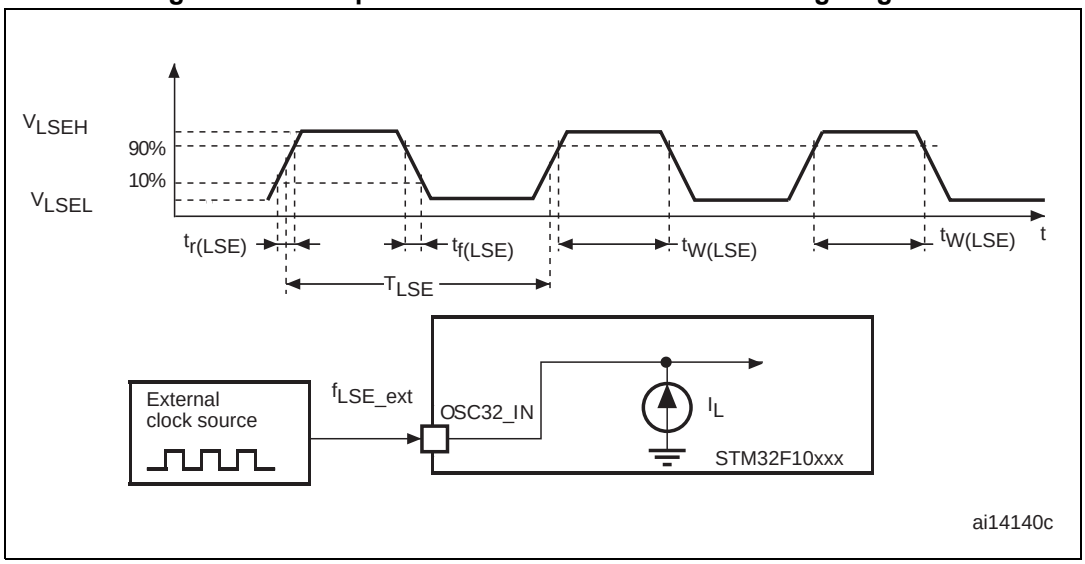


Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

5.3.15 TIM timer characteristics

The parameters given in *Table 37* are guaranteed by design.

Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 37. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	27.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 36 MHz	0	18	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	0.0278	1820	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	-	119.2	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

The STM32F101xx medium-density access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

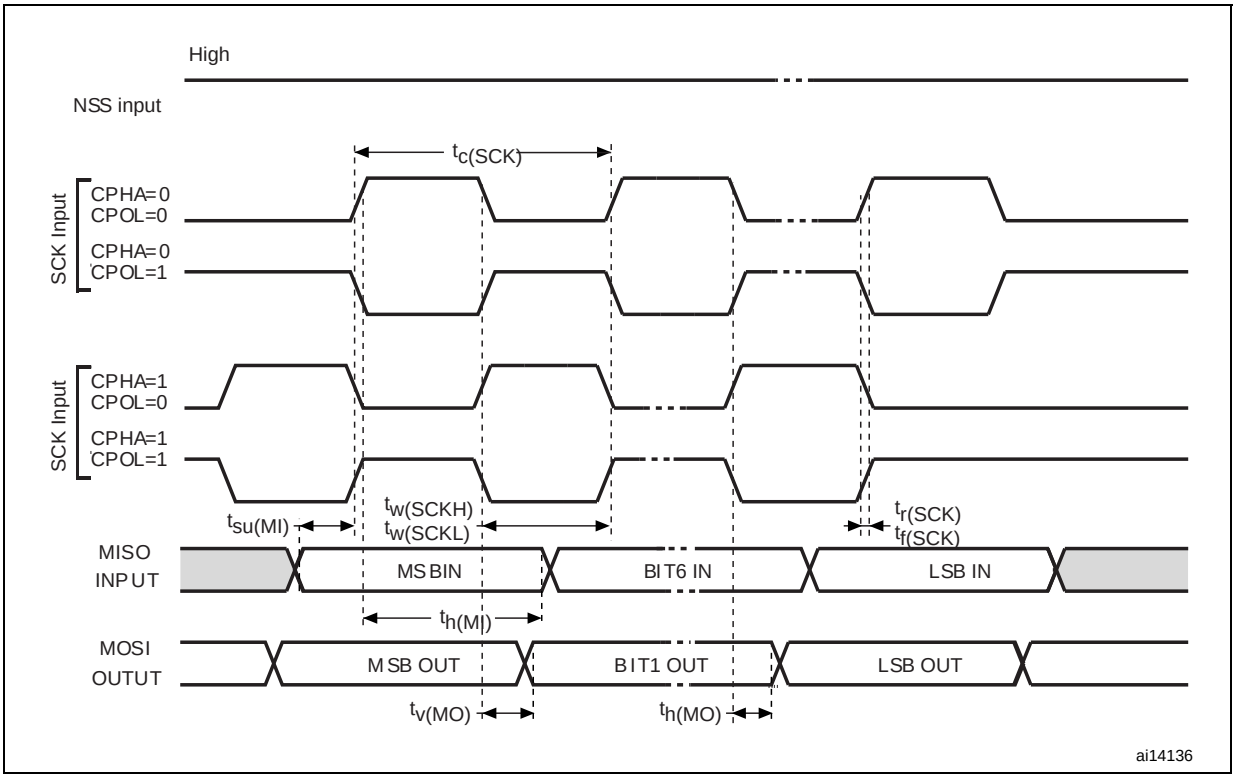
The I²C characteristics are described in *Table 38*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 38. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

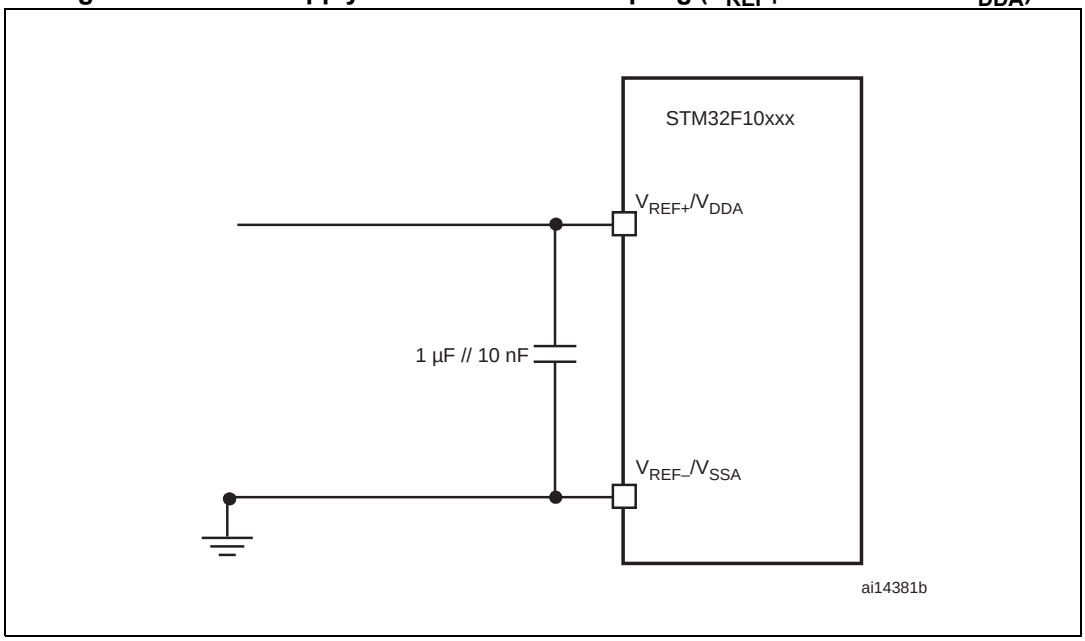
1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Figure 32. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Table 47. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	-	0.020	0.050	-	0.0008	0.0020
A2	-	0.650	1.000	-	0.0256	0.0394
A3	-	0.200	-	-	0.0079	-
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
K	0.250	-	-	0.0098	-	-
ddd	-	-	0.080	-	-	0.0031

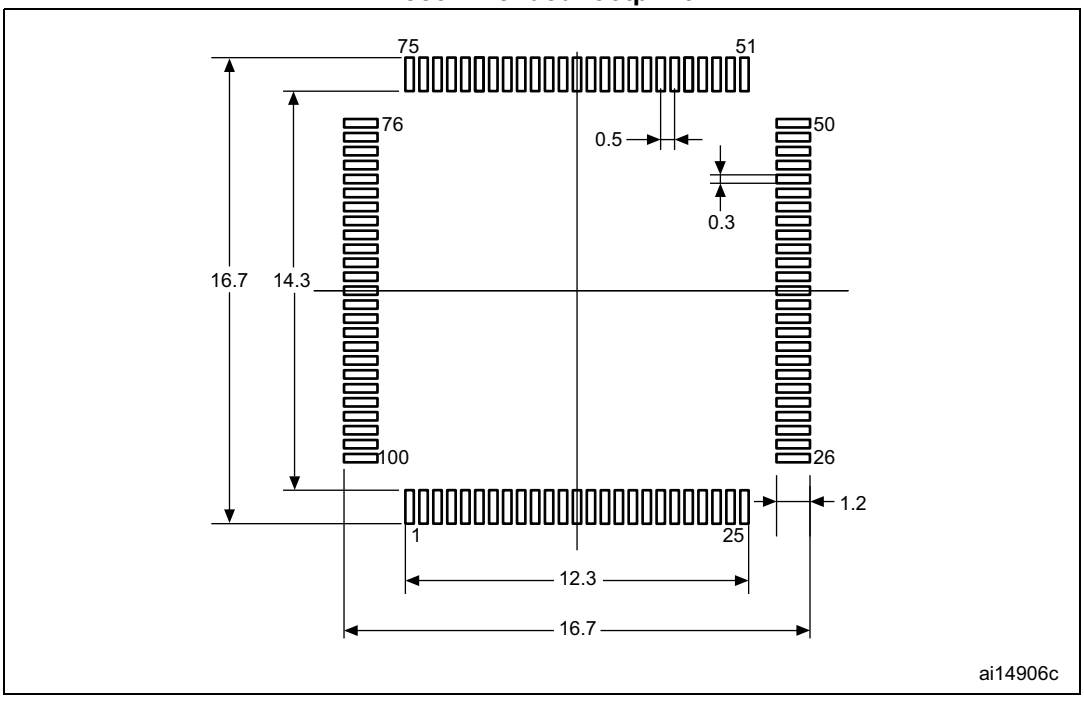
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 48. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

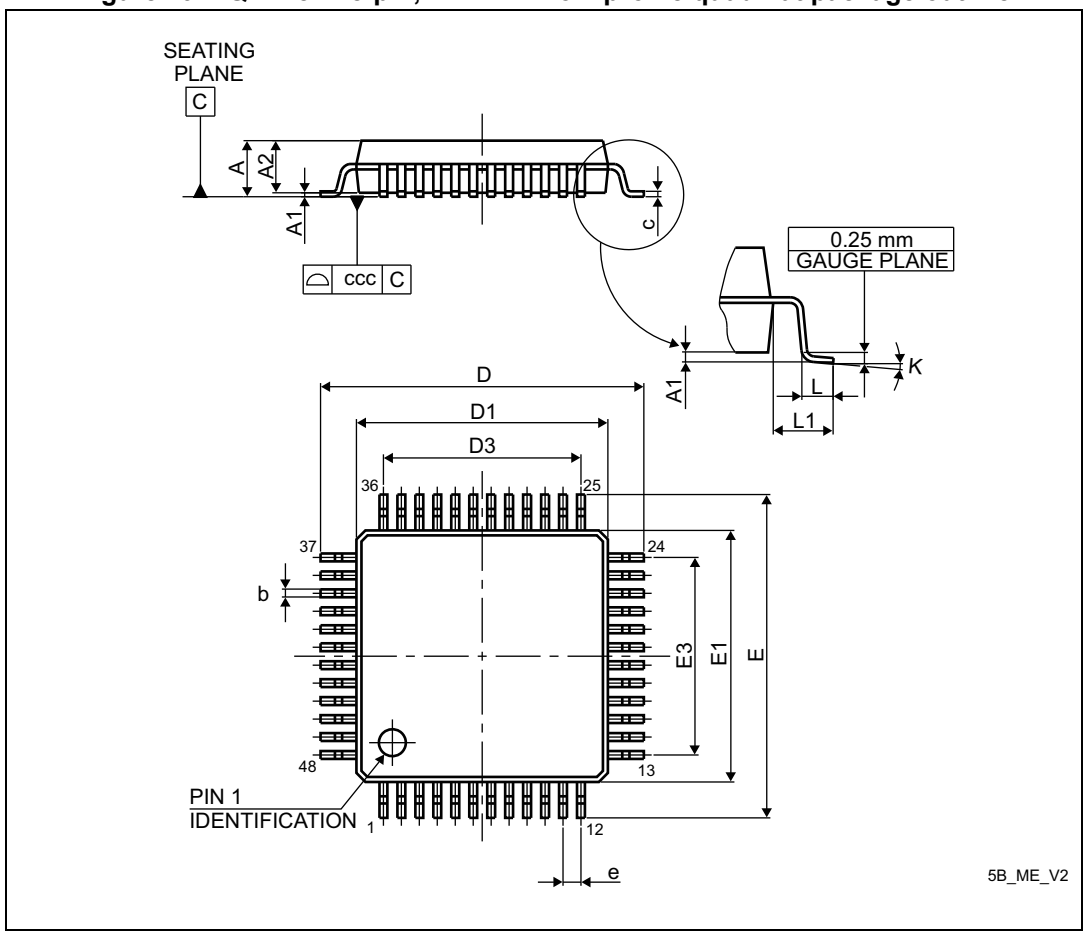
Figure 44. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

6.6 LQFP48 package information

Figure 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

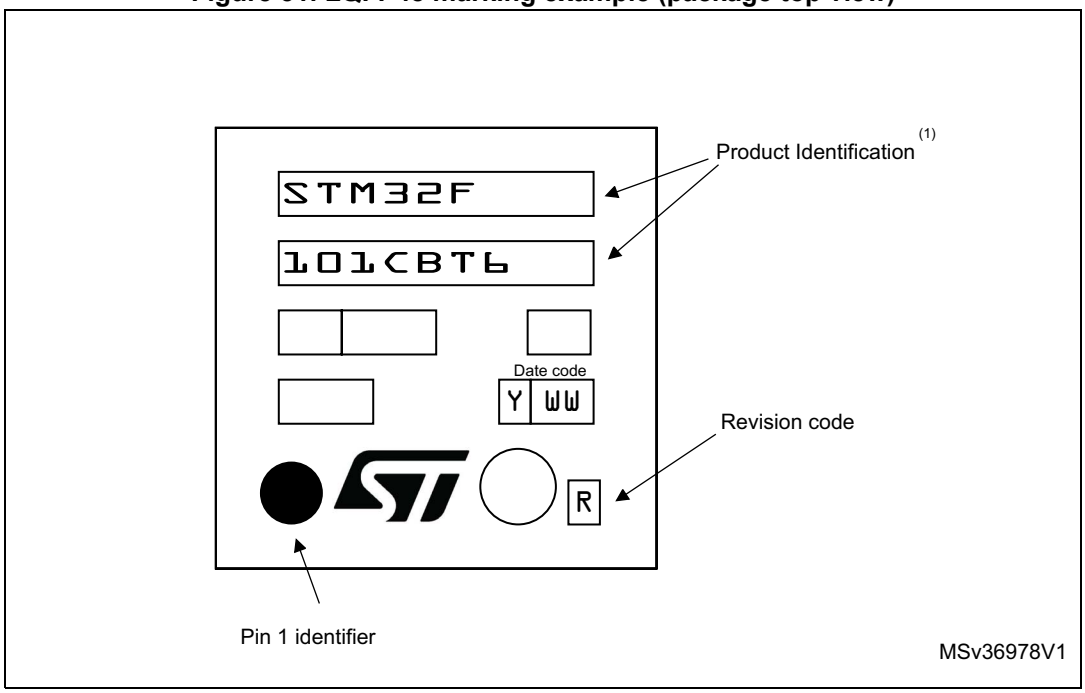


1. Drawing is not to scale.

Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 51. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Apr-2009	11	I/O information clarified *on page 1*. *Figure 8: Memory map* modified. In *Table 4: Medium-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 16*, *Figure 17* and *Figure 18* show typical curves. *Table 19: High-speed external user clock characteristics* and *Table 20: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 23: HSI oscillator characteristics*. Small text changes.
22-Sep-2009	12	*Note 5* updated and *Note 4* added in *Table 4: Medium-density STM32F101xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 11: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 15: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 19: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*. *Figure 28: Recommended NRST pin protection* modified. *Note 1* modified below *Figure 21: Typical application with an 8 MHz crystal*. *Figure 28: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 51*. Jitter added to *Table 26: PLL characteristics*. C_{ADC} and R_{AIN} parameters modified in *Table 41: ADC characteristics*. R_{AIN} max values modified in *Table 42: RAIN max for fADC = 14 MHz*. Small text changes.
20-May-2010	13	Added STM32F101TB devices. Added VFQFPN48 package. Updated note 2 below *Table 38: I2C characteristics* Updated *Figure 29: I2C bus AC waveforms and measurement circuit(1)* Updated *Figure 28: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*

Table 53. Document revision history (continued)

Date	Revision	Changes
19-Apr-2011	14	Updated footnotes below *Table 5: Voltage characteristics on page 32* and *Table 6: Current characteristics on page 33* Updated tw min in *Table 19: High-speed external user clock characteristics on page 45* Updated startup time in *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 48* Added *Section 5.3.12: I/O current injection characteristics* Updated *Section 5.3.13: I/O port characteristics*
15-May-2013	15	Replaced VQFN48 package with UQFN48 in cover page packages, *Table 2: Device features and peripheral counts (STM32F101xx medium-density access line)*, *Figure 7: STM32F101xx medium-density access line UVFQPFN48 pinout*, *Table 4: Medium-density STM32F101xx pin definitions*, *Figure 4: STM32F101xx medium-density access line LQFP64 pinout*, added *Figure 37: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline*, *Table 47: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data*, *Table 52: Ordering information scheme* and updated *Table 51: Package thermal characteristics* Updated 'All GPIOs are high current...' in *Section 2.3.22: GPIOs (general-purpose inputs/outputs)* Updated *Table 4: Medium-density STM32F101xx pin definitions* Corrected Sigma letter in *Section 5.1.1: Minimum and maximum values* Updated *Table 6: Current characteristics* Added 'V_{IN}' in *Table 8: General operating conditions* Removed the first sentence in *Section 5.3.16: Communications interfaces* Updated first sentence in *Output driving current* Added note *5.* in *Table 23: HSI oscillator characteristics* Updated 'V_{IL}' and 'V_{IH}' in *Table 33: I/O static characteristics* Added notes to *Figure 23: Standard I/O input characteristics - CMOS port*, *Figure 24: Standard I/O input characteristics - TTL port*, *Figure 25: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 26: 5 V tolerant I/O input characteristics - TTL port* Updated note *2.* in *Table 44: ADC accuracy* Updated *Figure 29: I2C bus AC waveforms and measurement circuit(1)* Updated note *2.* and *3.*,removed note "the device must internally..." in *Table 38: I2C characteristics* Updated title of *Table 39: SCL frequency (fPCLK1= 36 MHz, VDD_I2C = 3.3 V)*
05-Aug-2013	16	Updated the reference for '$V_{ESD(CDM)}$' in *Table 30: ESD absolute maximum ratings* Corrected 'tf(IO)out' in *Figure 27: I/O AC characteristics definition* Updated *Table 46: UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data*
19-Jun-2015	17	Updated *Section 6.1: Package mechanical data* and *Table 18: Peripheral current consumption*.