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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-VFQFPN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101tbu6

2 Description

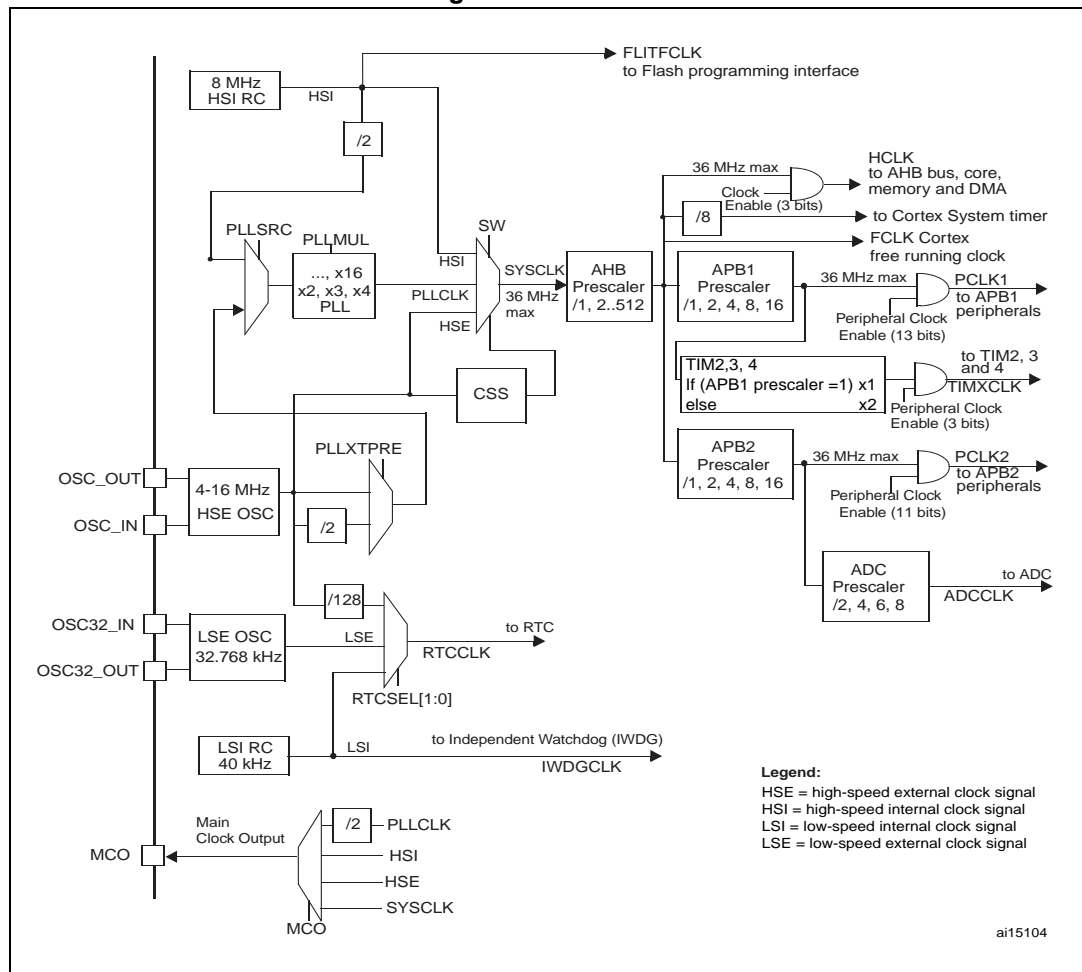
The STM32F101xB and STM32F101x8 medium-density access line family incorporates the high-performance ARM® Cortex® -M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I²Cs, two SPIs, and up to three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F101xx medium-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx medium-density access line family includes devices in four different packages ranging from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx medium-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz or 28 MHz.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are referred to as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F101x8/B devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities and a timer less. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the STM32F101xx family.

The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

Pinout	Memory size						
	Low-density devices		Medium-density devices		High-density devices		
	16 KB Flash	32 KB Flash ⁽¹⁾	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	4 KB RAM	6 KB RAM	10 KB RAM	16 KB RAM	32 KB RAM	48 KB RAM	48 KB RAM
144	-	-	-	-	5 × USARTs 4 × 16-bit timers, 2 × basic timers 3 × SPIs, 2 × I ² Cs, 1 × ADC, 2 × DACs, FSMC (100 and 144 pins)		
100	-	-	3 × USARTs 3 × 16-bit timers 2 × SPIs, 2 × I2Cs, 1 × ADC				
64	2 × USARTs 2 × 16-bit timers 1 × SPI, 1 × I ² C						
48							
36							
					-	-	-
					-	-	-

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There are three synchronizable general-purpose timers embedded in the STM32F101xx medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.23 ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 4. STM32F101xx medium-density access line LQFP64 pinout

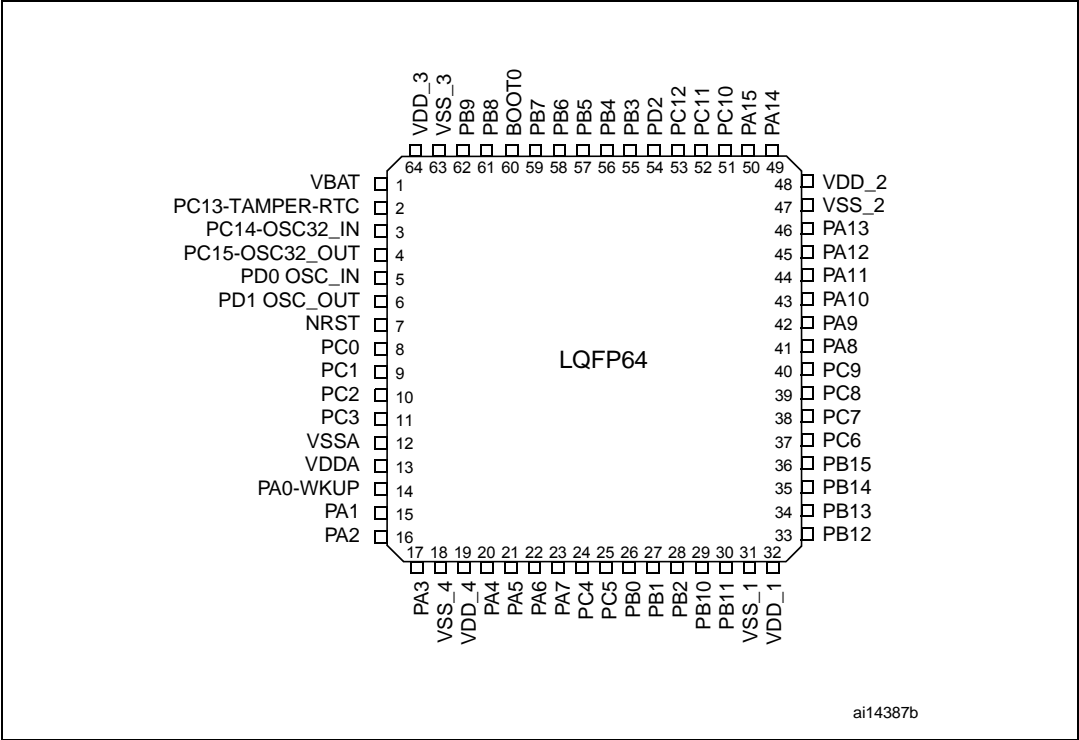


Figure 5. STM32F101xx medium-density access line LQFP48 pinout

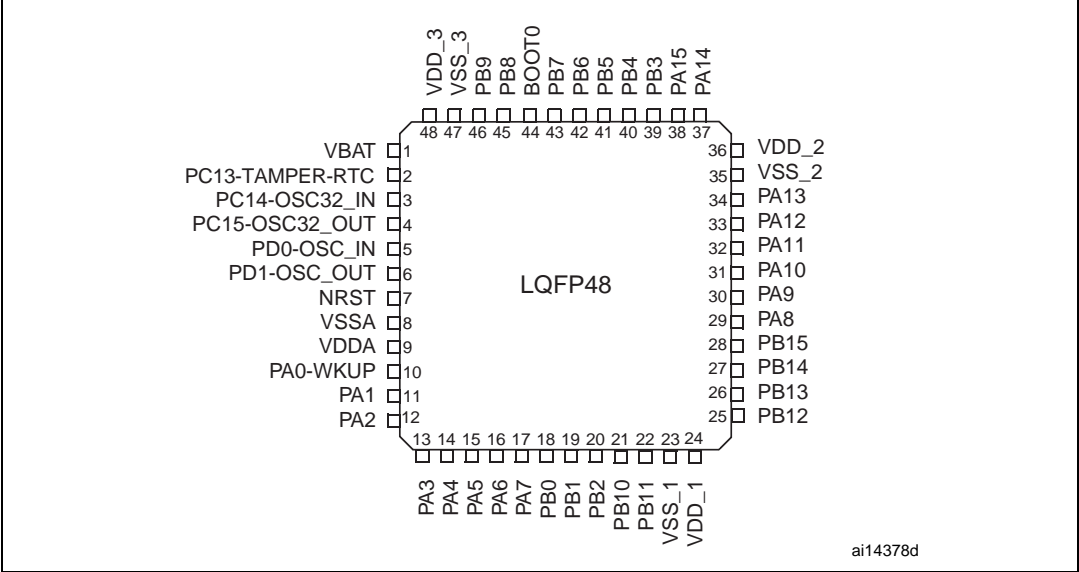


Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type ⁽¹⁾	I / O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽³⁾⁽⁴⁾	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
12	16	25	9	PA2	I/O	-	PA2	USART2_TX ⁽⁸⁾ / ADC_IN2/TIM2_CH3 ⁽⁸⁾	-
13	17	26	10	PA3	I/O	-	PA3	USART2_RX ⁽⁸⁾ / ADC_IN3/TIM2_CH4 ⁽⁸⁾	-
-	18	27	-	V _{SS_4}	S	-	V _{SS_4}	-	-
-	19	28	-	V _{DD_4}	S	-	V _{DD_4}	-	-
14	20	29	11	PA4	I/O	-	PA4	SPI1_NSS ⁽⁸⁾ /ADC_IN4 USART2_CK ⁽⁸⁾	-
15	21	30	12	PA5	I/O	-	PA5	SPI1_SCK ⁽⁸⁾ /ADC_IN5	-
16	22	31	13	PA6	I/O	-	PA6	SPI1_MISO ⁽⁸⁾ /ADC_IN6 TIM3_CH1 ⁽⁸⁾	-
17	23	32	14	PA7	I/O	-	PA7	SPI1_MOSI ⁽⁸⁾ /ADC_IN7 TIM3_CH2 ⁽⁸⁾	-
-	24	33	-	PC4	I/O	-	PC4	ADC_IN14	-
-	25	34	-	PC5	I/O	-	PC5	ADC_IN15	-
18	26	35	15	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3 ⁽⁸⁾	-
19	27	36	16	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4 ⁽⁸⁾	-
20	28	37	17	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	38	-	PE7	I/O	FT	PE7	-	-
-	-	39	-	PE8	I/O	FT	PE8	-	-
-	-	40	-	PE9	I/O	FT	PE9	-	-
-	-	41	-	PE10	I/O	FT	PE10	-	-
-	-	42	-	PE11	I/O	FT	PE11	-	-
-	-	43	-	PE12	I/O	FT	PE12	-	-
-	-	44	-	PE13	I/O	FT	PE13	-	-
-	-	45	-	PE14	I/O	FT	PE14	-	-
-	-	46	-	PE15	I/O	FT	PE15	-	-
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX ⁽⁸⁾	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX ⁽⁸⁾	TIM2_CH4

Figure 17. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at $V_{DD} = 3.3\text{ V}$ and 3.6 V

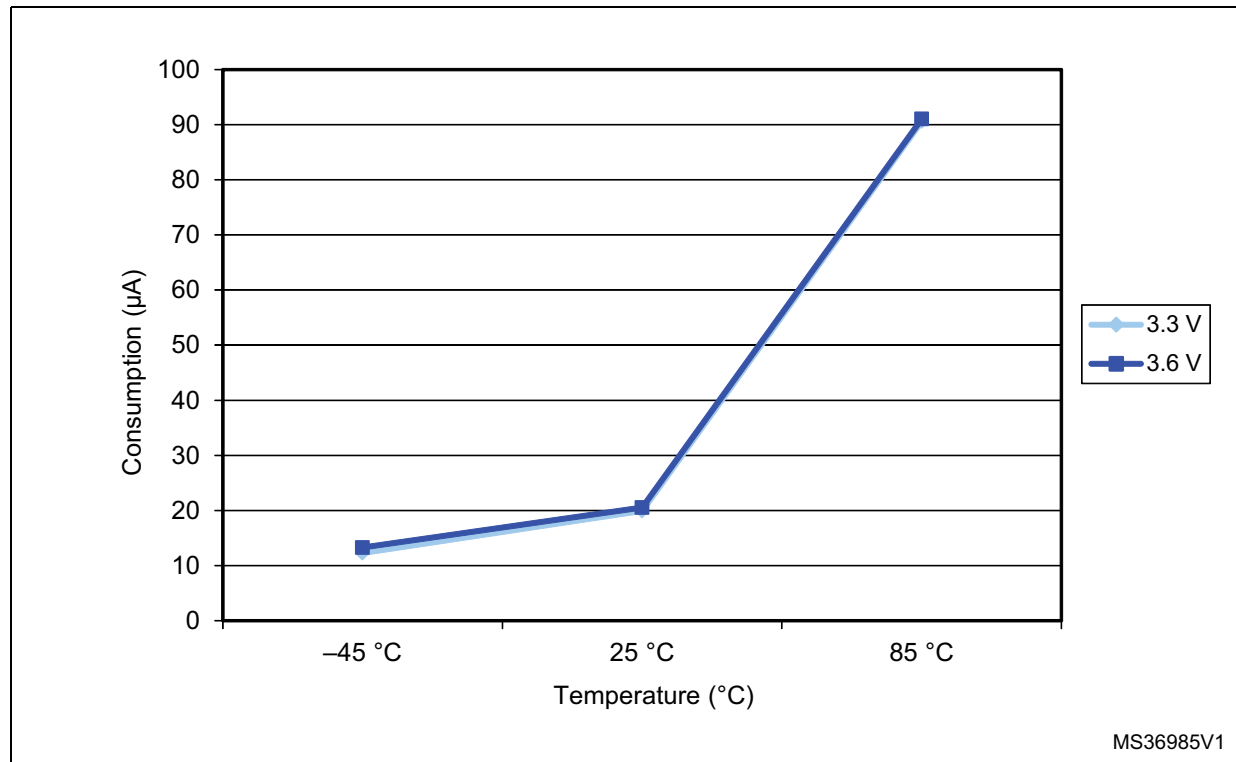


Figure 18. Typical current consumption in Standby mode versus temperature at $V_{DD} = 3.3\text{ V}$ and 3.6 V

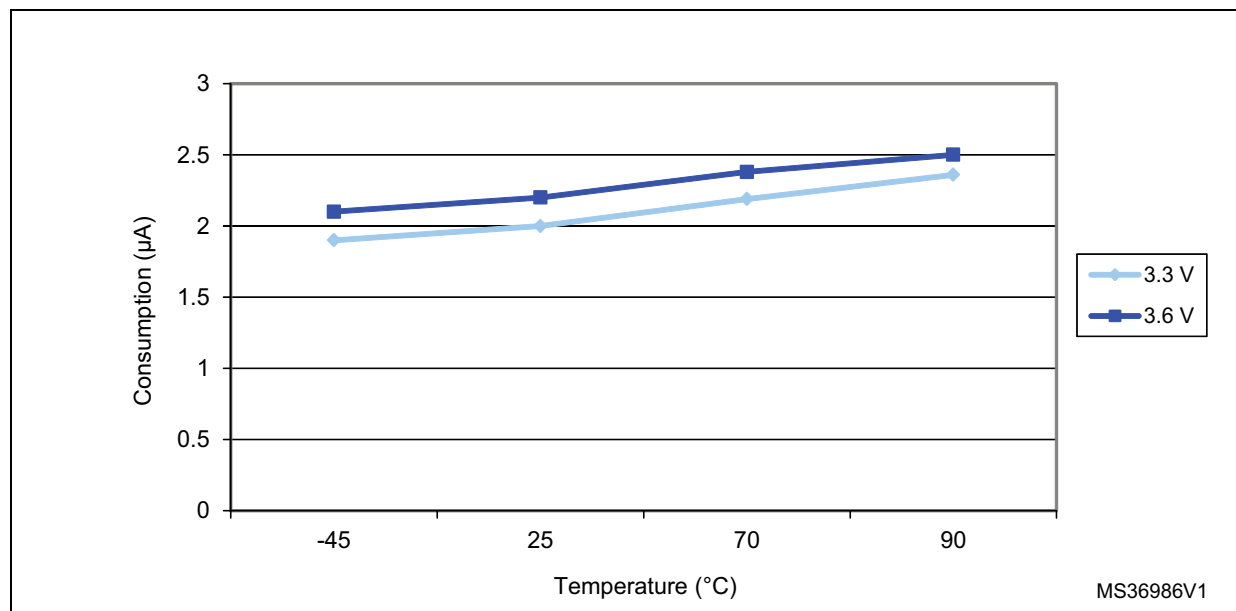


Table 18. Peripheral current consumption

Peripheral		Typical consumption at 25 °C ⁽¹⁾	Unit
AHB (up to 36 MHz)	DMA1	16.53	μA/MHz
	BusMatrix ⁽²⁾	8.33	
APB1 (up to 18 MHz)	APB1-Bridge	10.28	
	TIM2	32.50	
	TIM3	31.39	
	TIM4	31.94	
	SPI2	4.17	
	USART2	12.22	
	USART3	12.22	
	I2C1	10.00	
	I2C2	10.00	
	WWDG	2.50	
	PWR	1.67	
	BKP	2.50	
	IWDG	11.67	
APB2 (up to 36 MHz)	APB2-Bridge	3.75	
	GPIO A	6.67	
	GPIO B	6.53	
	GPIO C	6.53	
	GPIO D	6.53	
	GPIO E	6.39	
	ADC1 ⁽³⁾	17.50	
	SPI1	4.72	
	USART1	11.94	

1. $f_{HCLK} = 36$ MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

2. The BusMatrix is automatically active when at least one master is ON.

3. Specific conditions for ADC: $f_{HCLK} = 28$ MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to '1', the consumption added is equal to 0.65 mA. When the ADC is enabled, a current consumption is added equal to 0.05 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in [Table 19](#) result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

Figure 19. High-speed external clock source AC timing diagram

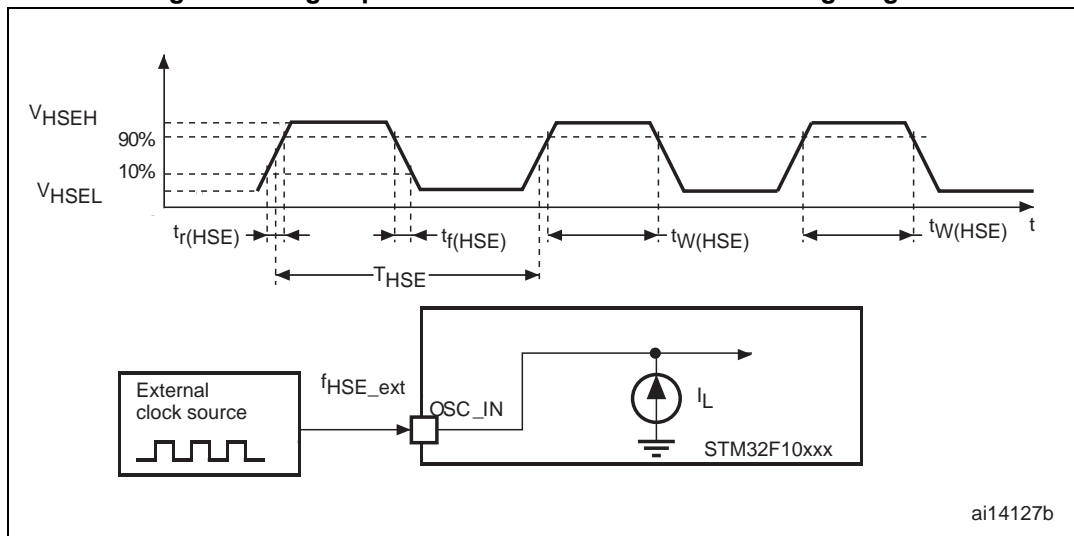
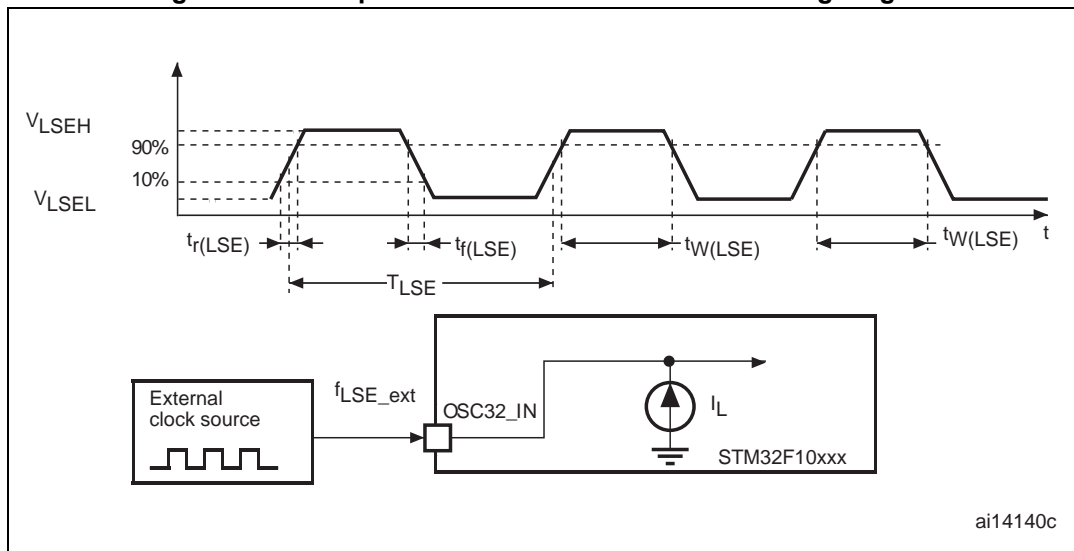


Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 21](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	30	40	60	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.65	1.2	μ A

1. $V_{DD} = 3$ V, $T_A = -40$ to 85 °C unless otherwise specified.

2. Based on characterization, not tested in production.

3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in [Table 25](#) are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wakeup from Sleep mode	1.8	μ s
$t_{WUSTOP}^{(1)}$	Wakeup from Stop mode (regulator in run mode)	3.6	μ s
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}^{(1)}$	Wakeup from Standby mode	50	μ s

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min ⁽¹⁾	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock ⁽²⁾	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

The test results are given in [Table 28](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 36\text{ MHz}$ conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 36\text{ MHz}$ conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBμV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 23](#) and [Figure 24](#) for standard I/Os, and in [Figure 25](#) and [Figure 26](#) for 5 V tolerant I/Os.

Figure 23. Standard I/O input characteristics - CMOS port

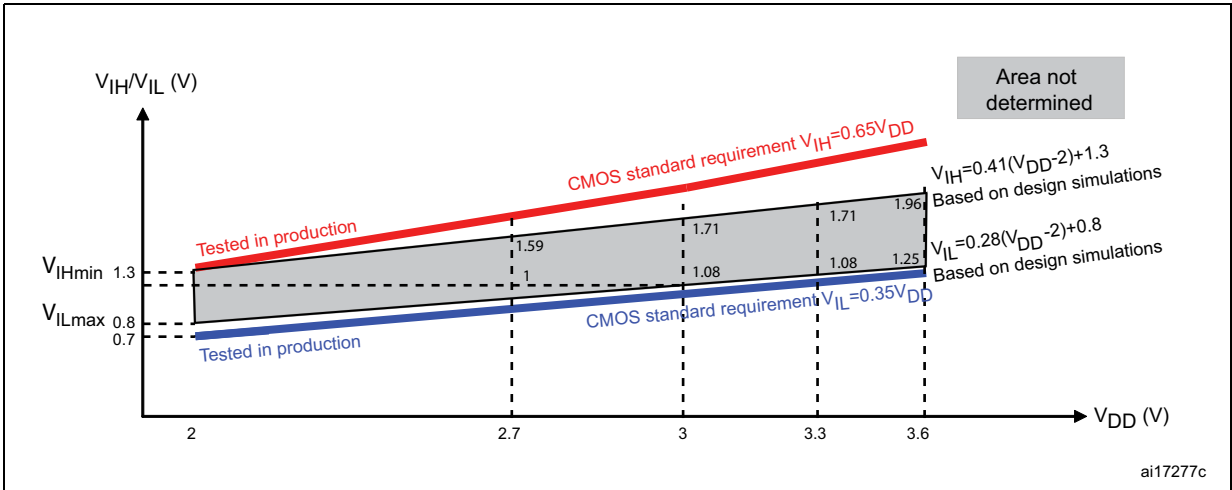
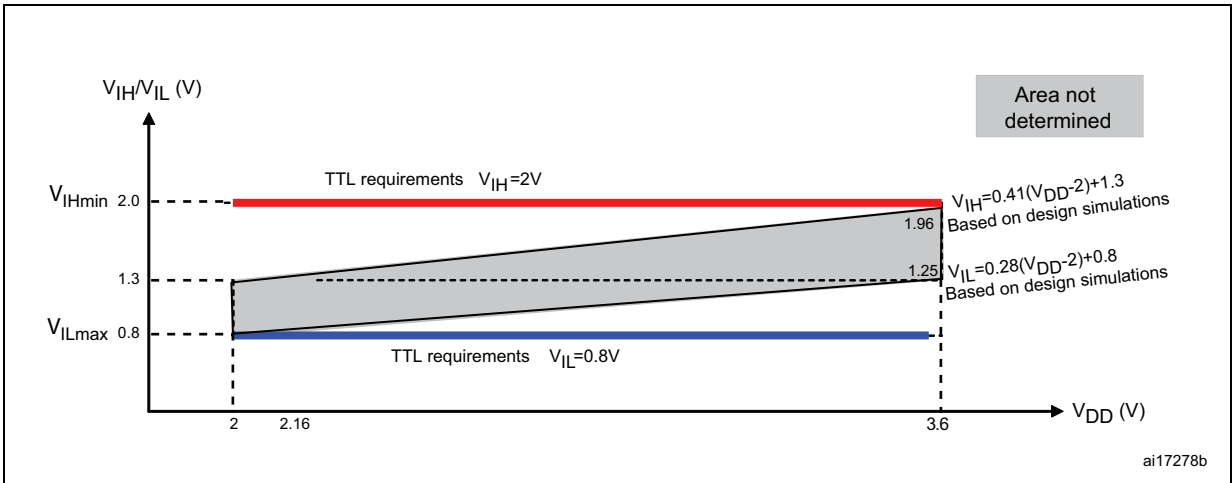


Figure 24. Standard I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 6](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 6](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port ⁽²⁾ , $I_{IO} = +8$ mA, $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port ⁽²⁾ $I_{IO} = +8$ mA $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +20$ mA ⁽⁴⁾ $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-1.3$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	$I_{IO} = +6$ mA ⁽⁴⁾ $2\text{ V} < V_{DD} < 2.7\text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		$V_{DD}-0.4$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 27](#) and [Table 35](#), respectively.

Unless otherwise specified, the parameters given in [Table 35](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

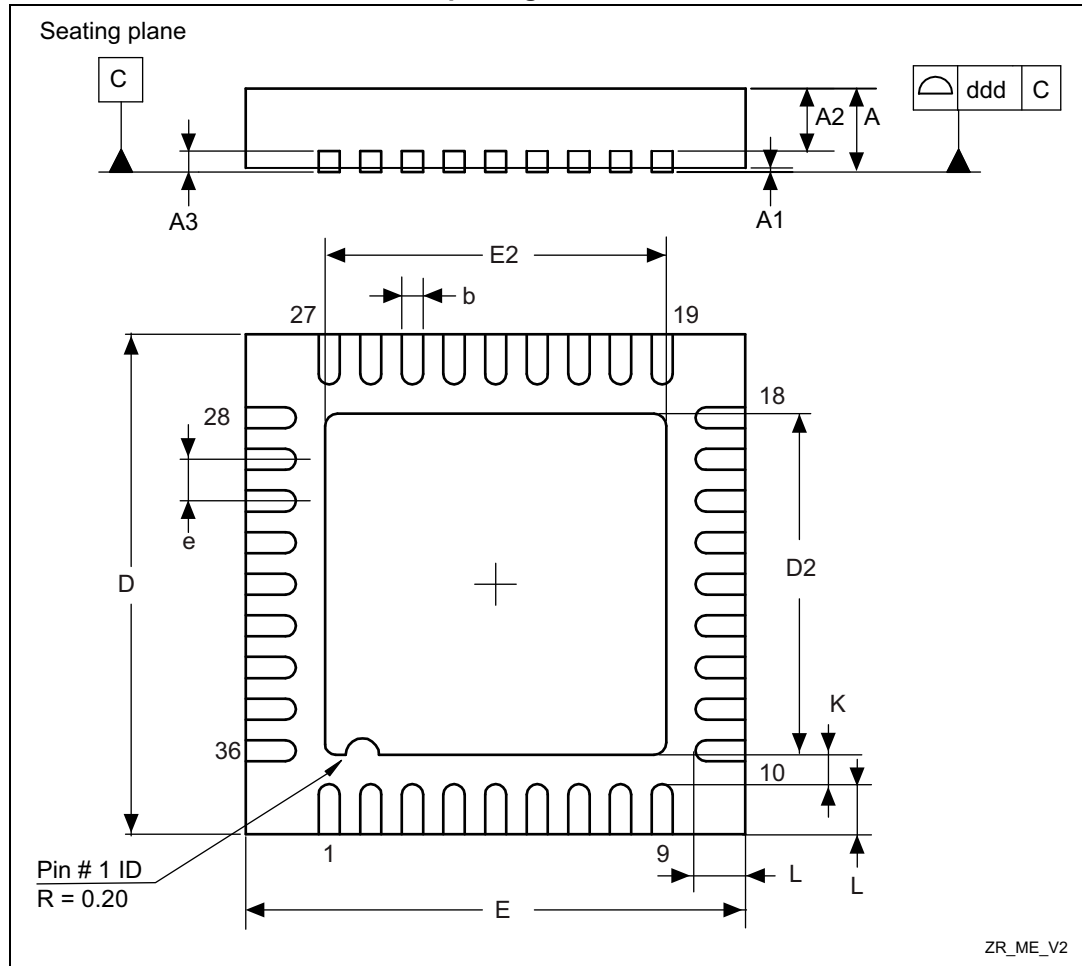
Table 35. I/O AC characteristics⁽¹⁾

MODEx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	10	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		25 ⁽³⁾	
11	$F_{\max(\text{IO})\text{out}}$	Maximum Frequency ⁽²⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	50	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	30	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	20	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 27](#).
3. Guaranteed by design, not tested in production.

6.3 VFQFPN36 package information

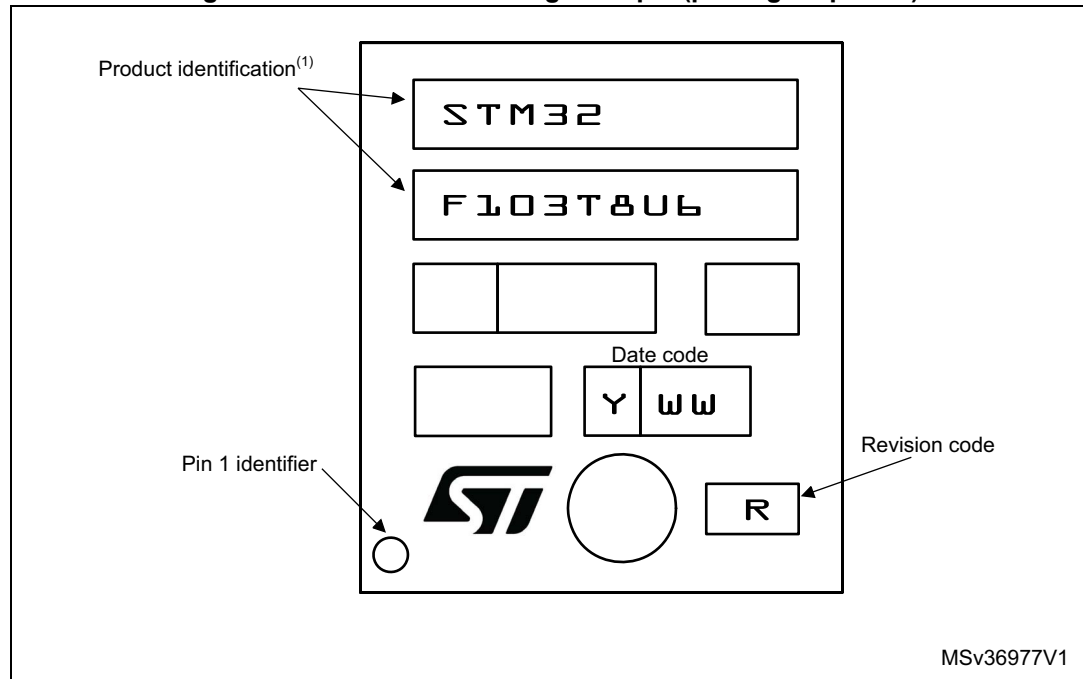
Figure 40. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

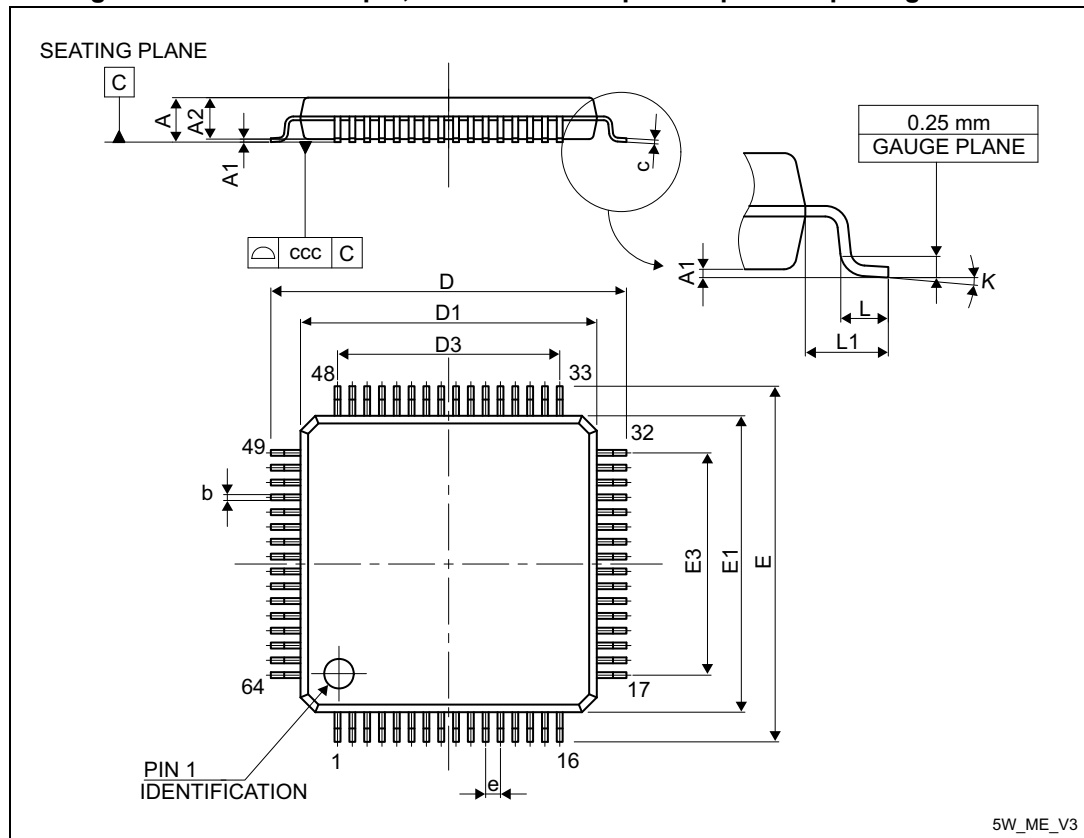
Figure 42. VFQFPN36 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.5 LQFP64 package information

Figure 46. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

8 Revision history

Table 53. Document revision history

Date	Revision	Changes
06-Jun-2007	1	First draft.
20-Jul-07	2	<p>I_{DD} values modified in Table 11: Maximum current consumption in Run and Sleep modes ($T_A = 85\text{ }^{\circ}\text{C}$). V_{BAT} range modified in Power supply schemes. V_{REF+} min value, t_{STAB}, t_{lat} and f_{TRIG} added to Table 41: ADC characteristics. Table 37: TIMx characteristics modified. Note 6 modified and Note 8, Note 5 and Note 7 added below Table 4: Medium-density STM32F101xx pin definitions. Figure 20: Low-speed external clock source AC timing diagram, Figure 11: Power supply scheme, Figure 28: Recommended NRST pin protection and Figure 29: I2C bus AC waveforms and measurement circuit(1) modified. Sample size modified and machine model removed in Electrostatic discharge (ESD). Number of parts modified and standard reference updated in Static latch-up. $25\text{ }^{\circ}\text{C}$ and $85\text{ }^{\circ}\text{C}$ conditions removed and class name modified in Table 31: Electrical sensitivities. $t_{SU(LSE)}$ changed to $t_{SU(LSE)}$ in Table 21: HSE 4-16 MHz oscillator characteristics. In Table 27: Flash memory characteristics, typical endurance added, data retention for $T_A = 25\text{ }^{\circ}\text{C}$ removed and data retention for $T_A = 85\text{ }^{\circ}\text{C}$ added. Note removed below Table 8: General operating conditions. V_{BG} changed to V_{REFINT} in Table 11: Embedded internal reference voltage. I_{DD} max values added to Table 11: Maximum current consumption in Run and Sleep modes ($T_A = 85\text{ }^{\circ}\text{C}$). $I_{DD(HSI)}$ max value added to Table 23: HSI oscillator characteristics. R_{PU} and R_{PD} min and max values added to Table 33: I/O static characteristics. R_{PU} min and max values added to Table 36: NRST pin characteristics (two notes removed). Datasheet title corrected. USB characteristics section removed. Features on page 1 list optimized. Small text changes.</p>

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	8	<p>Small text changes.</p> <p>Power supply supervisor on page 16 modified and V_{DDA} added to Table 8: General operating conditions on page 33.</p> <p>Capacitance modified in Figure 11: Power supply scheme on page 31.</p> <p>Table notes revised in Section 5: Electrical characteristics.</p> <p>Maximum value of $t_{RSTTEMPO}$ modified in Table 10: Embedded reset and power control block characteristics on page 35.</p> <p>Values added to Table 15: Typical and maximum current consumptions in Stop and Standby modes and Table 21: Typical current consumption in Standby mode removed.</p> <p>f_{HSE_ext} modified in Table 19: High-speed external user clock characteristics on page 45. f_{PLL_IN} modified in Table 26: PLL characteristics on page 50.</p> <p>f_{HCLK} corrected in Table 28: EMS characteristics.</p> <p>Minimum SDA and SCL fall time value for Fast mode removed from Table 38: I2C characteristics on page 63, note 1 modified.</p> <p>$t_{h(NSS)}$ modified in Table 40: SPI characteristics on page 65 and Figure 30: SPI timing diagram - slave mode and CPHA = 0 on page 66.</p> <p>C_{ADC} modified in Table 41: ADC characteristics on page 68 and Figure 34: Typical connection diagram using the ADC modified.</p> <p>f_{PCLK2} corrected in Table 43: ADC accuracy - limited test conditions and Table 44: ADC accuracy.</p> <p>Typical T_{S_temp} value removed from Table 45: TS characteristics on page 72.</p> <p>LQFP48 package specifications updated (see Table 50, Table 49 and Table 50).</p> <p>Axx option removed from Table 52: Ordering information scheme on page 92.</p>
24-Jul-2008	9	<p>First page modified: "Up to 2 x I²C interfaces" instead of "1 x I²C interface"</p>
23-Sep-2008	10	<p>STM32F101xx devices with 32 Kbyte Flash memory capacity removed, document updated accordingly.</p> <p>Section 2.2: Full compatibility throughout the family on page 14 updated.</p> <p>Notes modified in Table 4: Medium-density STM32F101xx pin definitions on page 24.</p> <p>Note 2 modified below Table 5: Voltage characteristics on page 32, ΔV_{DDx} min and ΔV_{DDx} min removed.</p> <p>Note 2 added to Table 8: General operating conditions on page 33.</p> <p>Measurement conditions specified in Section 5.3.5: Supply current characteristics on page 36.</p> <p>I_{DD} in standby mode at 85 °C modified in Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 39.</p> <p>General input/output characteristics on page 55 modified.</p> <p>Note added below Table 52: Ordering information scheme.</p> <p>Section 7.1: Future family enhancements removed. Small text changes.</p>