Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101v8t6tr

Contents

List of Figures

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Device features and peripheral counts (STM32F101xx medium-density access line)

Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx		STM32F101Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		10	16	10	16	10	16	10	16
Timers	General -purpose	3		3		3		3	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
12-bit synchronized ADC number of channels		110 channels		110 channels		116 channels		116 channels	
GPIOs		26		37		51		80	
CPU frequency		36 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64		LQFP100	

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There are three synchronizable general-purpose timers embedded in the STM32F101xx medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

Table 4. Medium-density STM32F101xx pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
-	-	1	-	PE2	I/O	FT	PE2	TRACECLK	-
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	-
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	-
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	-
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	-
1	1	6	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	7	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	8	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	9	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
-	-	10	-	V_{SS_5}	S	-	V_{SS_5}	-	-
-	-	11	-	V_{DD_5}	S	-	V_{DD_5}	-	-
5	5	12	2	OSC_IN	I	-	OSC_IN	-	PD0(7)
6	6	13	3	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
7	7	14	4	NRST	I/O	-	NRST	-	-
-	8	15	-	PC0	I/O	-	PC0	ADC_IN10	-
-	9	16	-	PC1	I/O	-	PC1	ADC_IN11	-
-	10	17	-	PC2	I/O	-	PC2	ADC_IN12	-
-	11	18	-	PC3	I/O	-	PC3	ADC_IN13	-
8	12	19	5	V_{SSA}	S	-	V_{SSA}	-	-
-	-	20	-	V_{REF-}	S	-	V_{REF-}	-	-
-	-	21	-	V_{REF+}	S	-	V_{REF+}	-	-
9	13	22	6	V_{DDA}	S	-	V_{DDA}	-	-
10	14	23	7	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS(8)/ ADC_IN0/ TIM2_CH1_ETR(8)	-
11	15	24	8	PA1	I/O	-	PA1	USART2_RTS(8)/ ADC_IN1/TIM2_CH2(8)	-

Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
12	16	25	9	PA2	I/O	-	PA2	USART2_TX(8)/ ADC_IN2/TIM2_CH3(8)	-
13	17	26	10	PA3	I/O	-	PA3	USART2_RX(8)/ ADC_IN3/TIM2_CH4(8)	-
-	18	27	-	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	28	-	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	29	11	PA4	I/O	-	PA4	SPI1_NSS(8)/ADC_IN4 USART2_CK(8)/	-
15	21	30	12	PA5	I/O	-	PA5	SPI1_SCK(8)/ADC_IN5	-
16	22	31	13	PA6	I/O	-	PA6	SPI1_MISO(8)/ADC_IN6 TIM3_CH1(8)	-
17	23	32	14	PA7	I/O	-	PA7	SPI1_MOSI(8)/ADC_IN7 TIM3_CH2(8)	-
-	24	33	-	PC4	I/O	-	PC4	ADC_IN14	-
-	25	34	-	PC5	I/O	-	PC5	ADC_IN15	-
18	26	35	15	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3(8)	-
19	27	36	16	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4(8)	-
20	28	37	17	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	38	-	PE7	I/O	FT	PE7	-	-
-	-	39	-	PE8	I/O	FT	PE8	-	-
-	-	40	-	PE9	I/O	FT	PE9	-	-
-	-	41	-	PE10	I/O	FT	PE10	-	-
-	-	42	-	PE11	I/O	FT	PE11	-	-
-	-	43	-	PE12	I/O	FT	PE12	-	-
-	-	44	-	PE13	I/O	FT	PE13	-	-
-	-	45	-	PE14	I/O	FT	PE14	-	-
-	-	46	-	PE15	I/O	FT	PE15	-	-
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX (8)	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX (8)	TIM2_CH4

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	28.6	mA
			24 MHz	19.9	
			16 MHz	14.7	
			8 MHz	8.6	
		External clock (2), all peripherals Disabled	36 MHz	19.8	
			24 MHz	13.9	
			16 MHz	10.7	
			8 MHz	6.8	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	24	mA
			24 MHz	17.5	
			16 MHz	12.5	
			8 MHz	7.5	
		External clock(2) all peripherals disabled	36 MHz	16	
			24 MHz	11.5	
			16 MHz	8.5	
			8 MHz	5.5	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 15. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

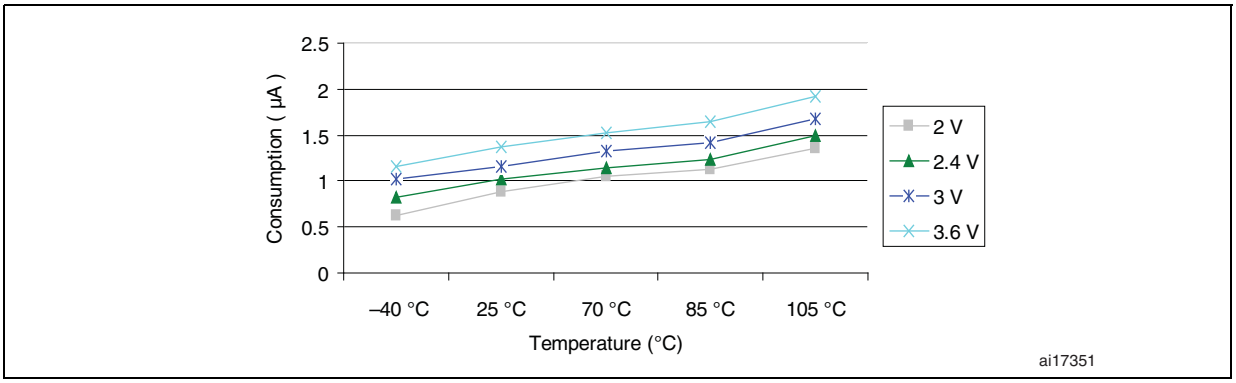


Figure 16. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

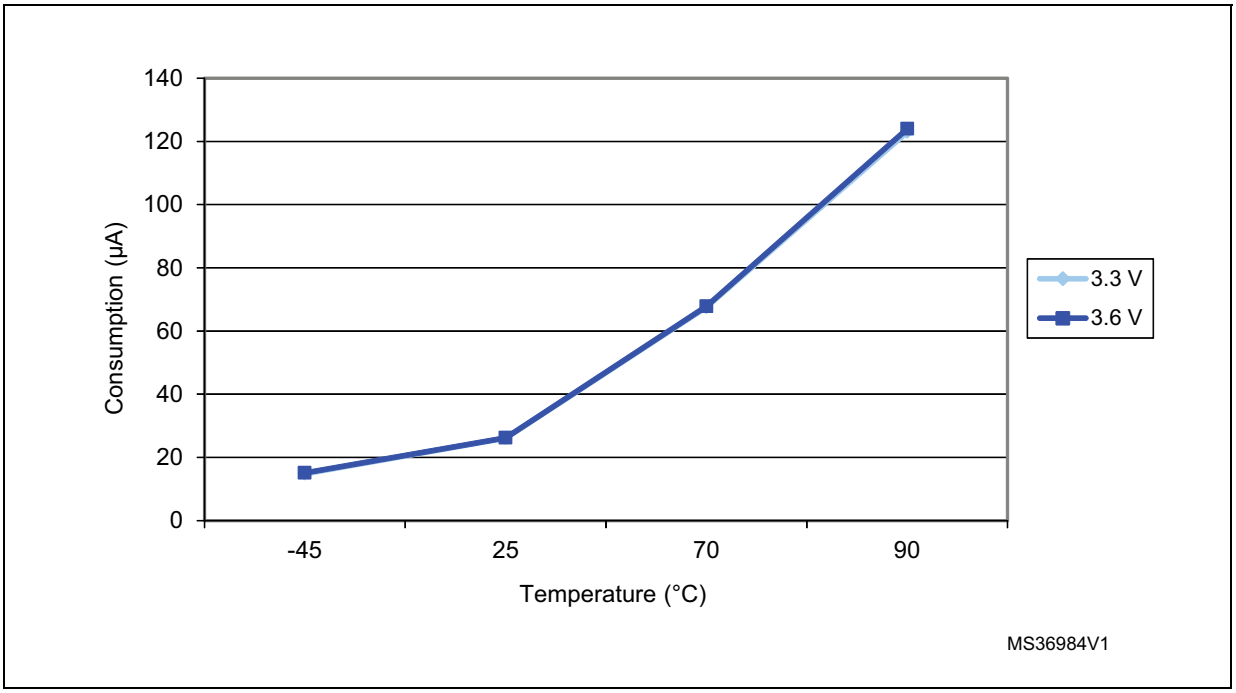


Table 26. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

Table 41. ADC characteristics

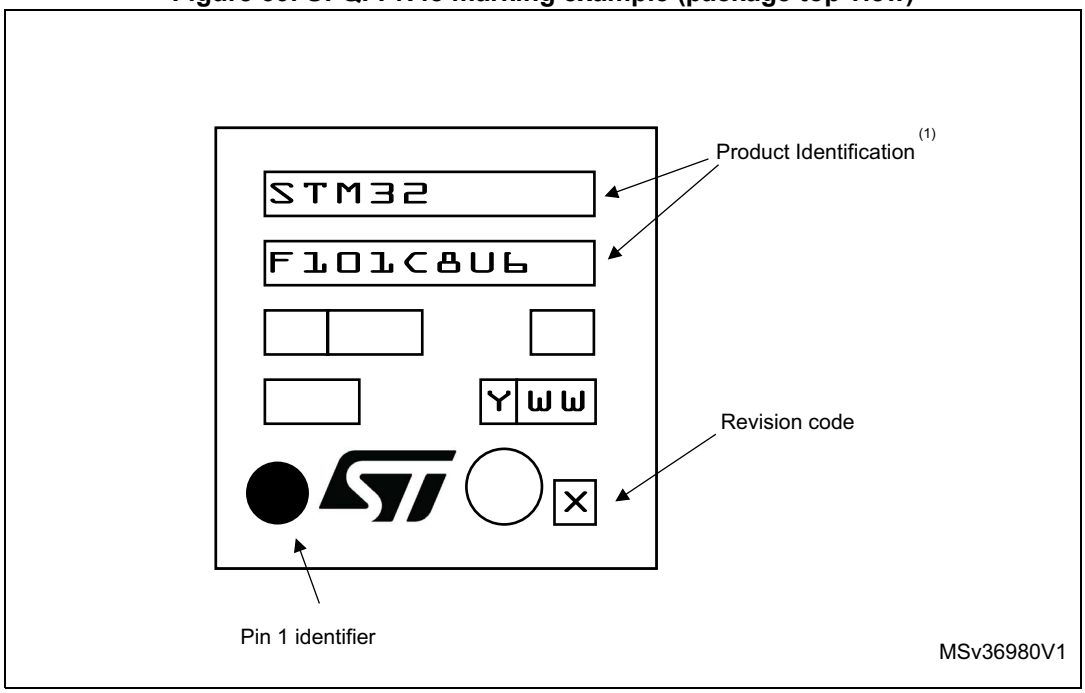
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 42* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin description* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 41*.

Device Marking for UFQFPN48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. UFQFPN48 marking example (package top view)

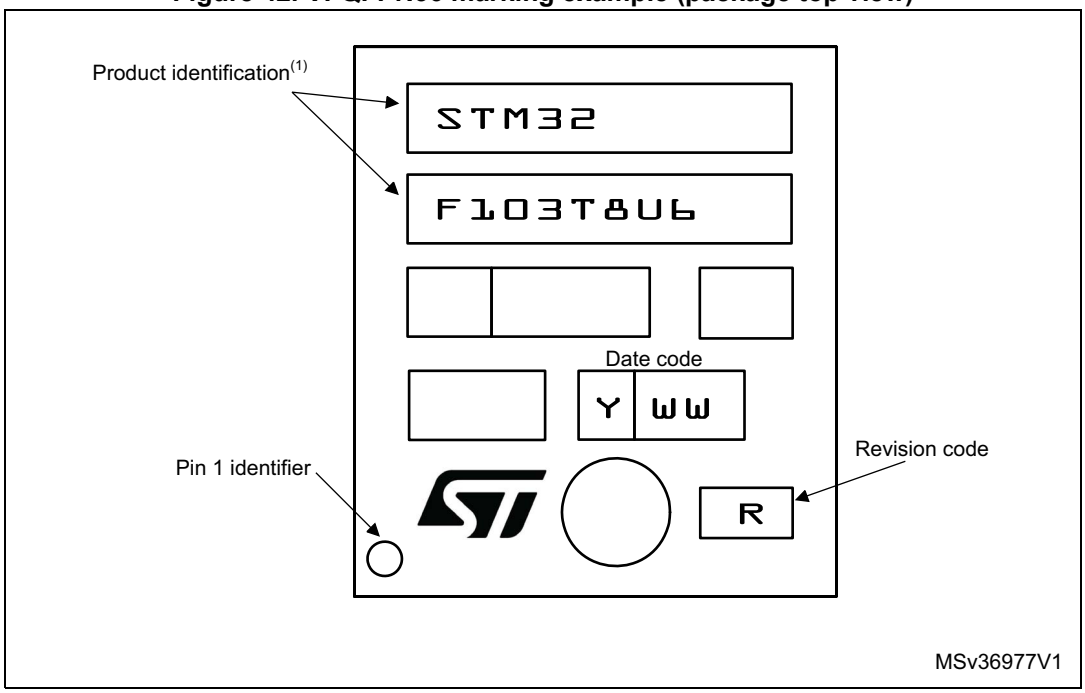


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. VFQFPN36 marking example (package top view)



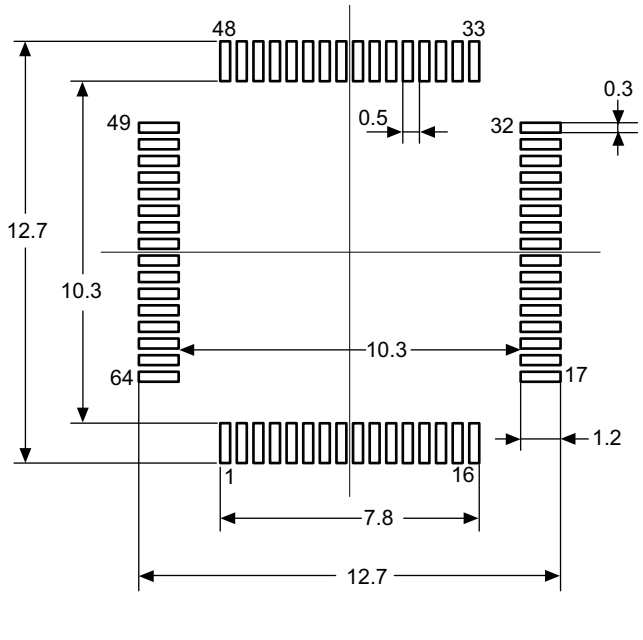
1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 50. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	$V_{ESD(CDM)}$ value added to *Table 30: ESD absolute maximum ratings*. Note added below *Table 10: Embedded reset and power control block characteristics*. and below *Table 21: HSE 4-16 MHz oscillator characteristics*. Note added below *Table 34: Output voltage characteristics* and V_{OH} parameter description modified. *Table 41: ADC characteristics* and *Table 43: ADC accuracy - limited test conditions* modified. *Figure 33: ADC accuracy characteristics* modified. Packages are ECOPACK® compliant. Tables modified in *Section 5.3.5: Supply current characteristics*. ADC and ANTI_TAMPER signal names modified (see *Table 4: Medium-density STM32F101xx pin definitions*). *Table 4: Medium-density STM32F101xx pin definitions* modified. Note 4 removed and values updated in *Table 21: Typical current consumption in Standby mode*. V_{hys} modified in *Table 33: I/O static characteristics*. Updated: *Table 28: EMS characteristics* and *Table 29: EMI characteristics*. t_{VDD} modified in *Table 9: Operating conditions at power-up / power-down*. Typical values modified, note 2 modified and note 3 removed in *Table 25: Low-power mode wakeup timings*. Maximum current consumption *Table 12*, *Table 13* and *Table 14* updated. Values added and notes added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *On-chip peripheral current consumption on page 43* added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). V_{prog} added to *Table 27: Flash memory characteristics*. T_{S_temp} added to *Table 45: TS characteristics*. $T_{S\_vrefint}$ added to *Table 11: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 55*. All I/Os are CMOS and TTL compliant. *Table 4: Medium-density STM32F101xx pin definitions*: table clarified and *Note 7* modified. Internal LSI RC frequency changed from 32 to 40 kHz (see *Table 24: LSI oscillator characteristics*). Values added to *Table 25: Low-power mode wakeup timings*. N_{END} modified in *Table 27: Flash memory characteristics*. Option byte addresses corrected in *Figure 8: Memory map*. ACC_{HSI} modified in *Table 23: HSI oscillator characteristics*. t_{JITTER} removed from *Table 26: PLL characteristics*. *Appendix A: Important notes on page 71* added. Added: *Figure 13*, *Figure 14*, *Figure 16* and *Figure 18*.