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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vbt6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x8 and STM32F101xB medium-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The medium-density STM32F101xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

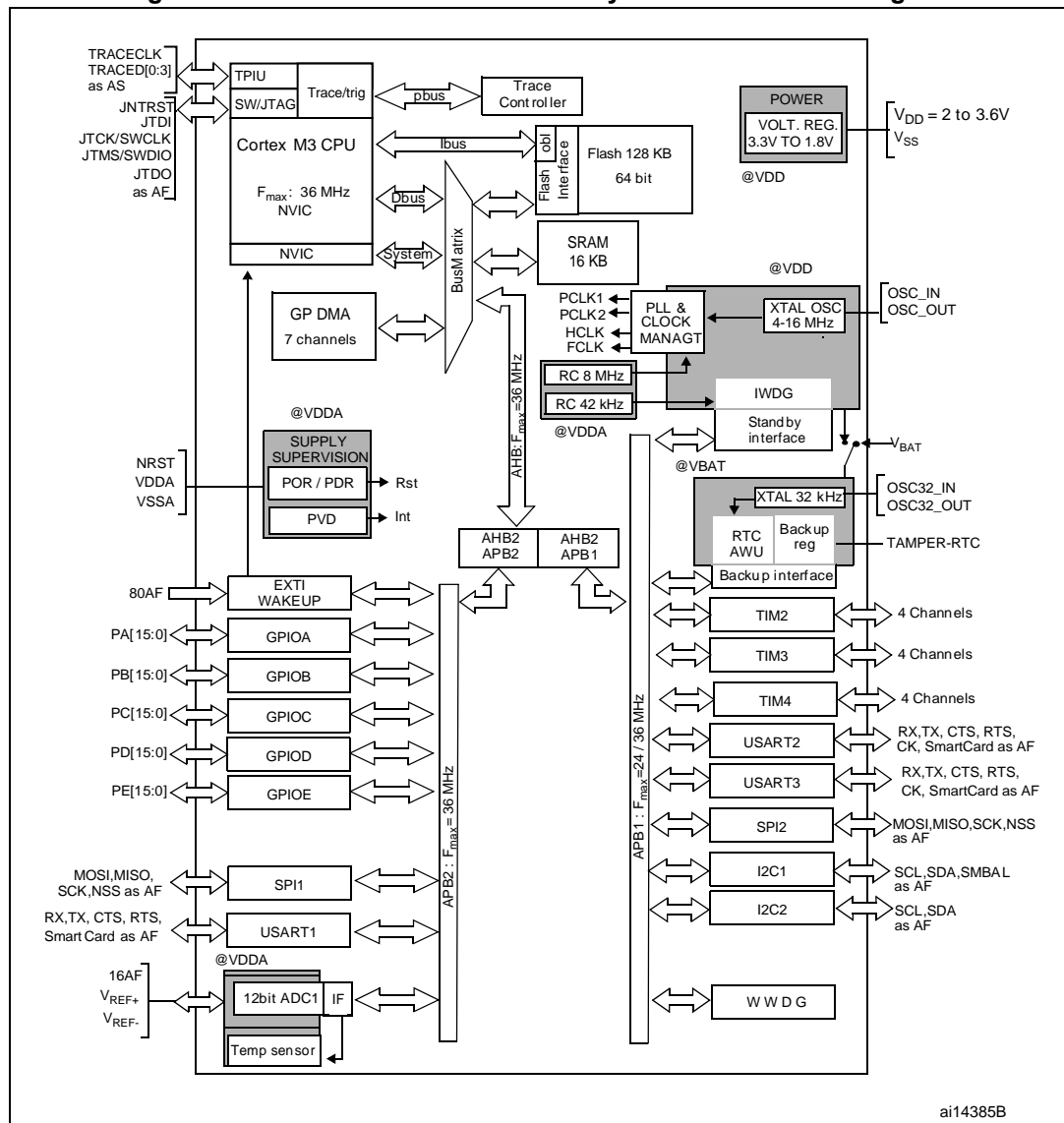
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex® -M3 core please refer to the Cortex® -M3 Technical Reference Manual, available from the www.arm.com website.



Figure 1. STM32F101xx medium-density access line block diagram



1. AF = alternate function on I/O port pin.
2. $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ (junction temperature up to $105\text{ }^{\circ}\text{C}$).

2.3 Overview

2.3.1 ARM® Cortex® -M3 core with embedded Flash and SRAM

The ARM® Cortex® -M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex® -M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xx medium-density access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F101xx medium-density access line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex® -M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general purpose timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There are three synchronizable general-purpose timers embedded in the STM32F101xx medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

Figure 6. STM32F101xx medium-density access line UFQFPN48 pinout

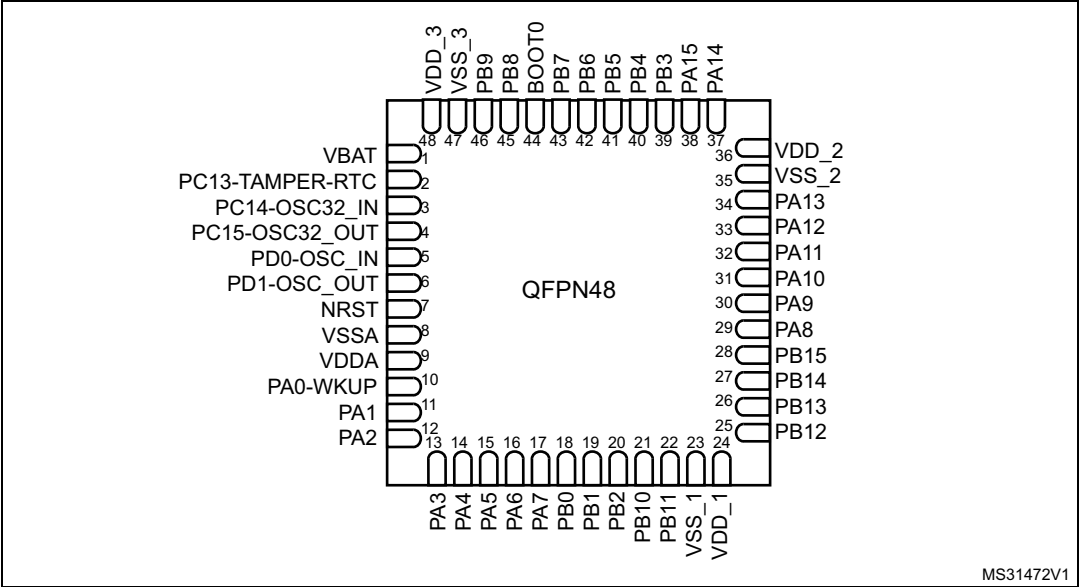


Figure 7. STM32F101xx medium-density access line VFQFPN36 pinout

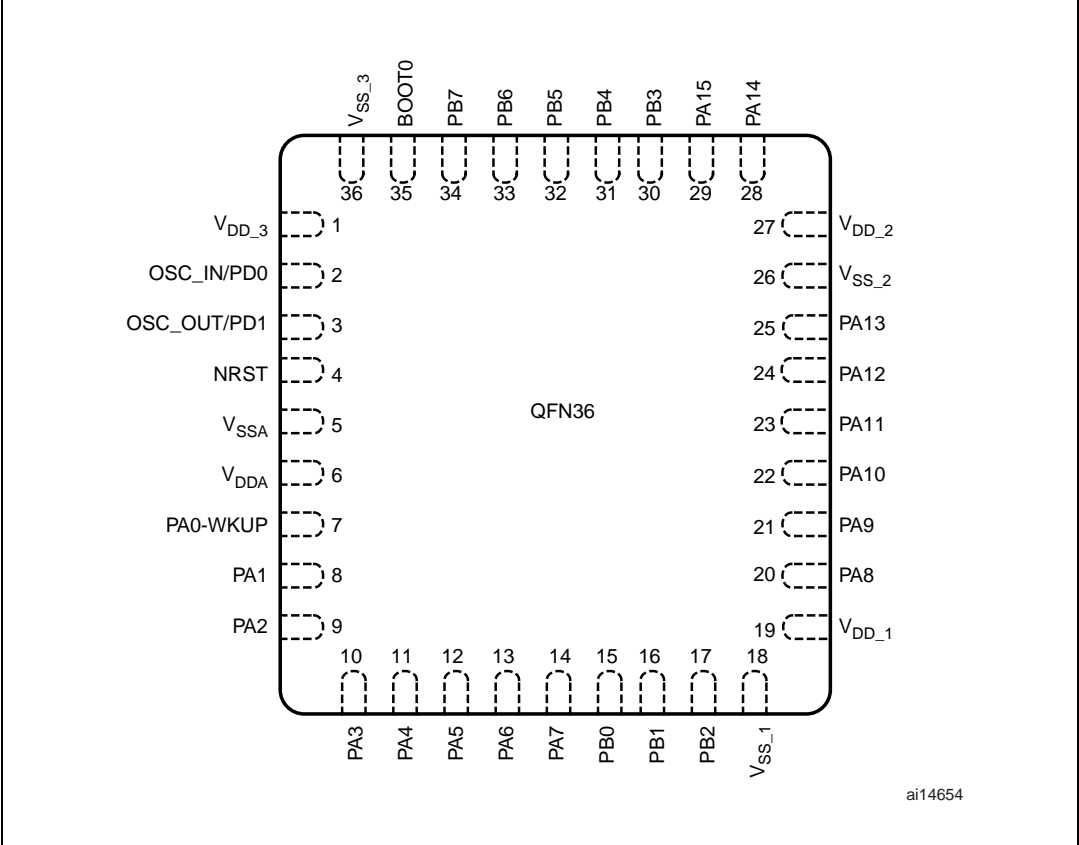


Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type ⁽¹⁾	I / O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽³⁾⁽⁴⁾	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
12	16	25	9	PA2	I/O	-	PA2	USART2_TX ⁽⁸⁾ / ADC_IN2/TIM2_CH3 ⁽⁸⁾	-
13	17	26	10	PA3	I/O	-	PA3	USART2_RX ⁽⁸⁾ / ADC_IN3/TIM2_CH4 ⁽⁸⁾	-
-	18	27	-	V _{SS_4}	S	-	V _{SS_4}	-	-
-	19	28	-	V _{DD_4}	S	-	V _{DD_4}	-	-
14	20	29	11	PA4	I/O	-	PA4	SPI1_NSS ⁽⁸⁾ /ADC_IN4 USART2_CK ⁽⁸⁾	-
15	21	30	12	PA5	I/O	-	PA5	SPI1_SCK ⁽⁸⁾ /ADC_IN5	-
16	22	31	13	PA6	I/O	-	PA6	SPI1_MISO ⁽⁸⁾ /ADC_IN6 TIM3_CH1 ⁽⁸⁾	-
17	23	32	14	PA7	I/O	-	PA7	SPI1_MOSI ⁽⁸⁾ /ADC_IN7 TIM3_CH2 ⁽⁸⁾	-
-	24	33	-	PC4	I/O	-	PC4	ADC_IN14	-
-	25	34	-	PC5	I/O	-	PC5	ADC_IN15	-
18	26	35	15	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3 ⁽⁸⁾	-
19	27	36	16	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4 ⁽⁸⁾	-
20	28	37	17	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	38	-	PE7	I/O	FT	PE7	-	-
-	-	39	-	PE8	I/O	FT	PE8	-	-
-	-	40	-	PE9	I/O	FT	PE9	-	-
-	-	41	-	PE10	I/O	FT	PE10	-	-
-	-	42	-	PE11	I/O	FT	PE11	-	-
-	-	43	-	PE12	I/O	FT	PE12	-	-
-	-	44	-	PE13	I/O	FT	PE13	-	-
-	-	45	-	PE14	I/O	FT	PE14	-	-
-	-	46	-	PE15	I/O	FT	PE15	-	-
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX ⁽⁸⁾	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX ⁽⁸⁾	TIM2_CH4

Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type ⁽¹⁾	I / O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽³⁾⁽⁴⁾	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
46	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4 ⁽⁸⁾	I2C1_SDA
-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	-
-	-	98	-	PE1	I/O	FT	PE1	-	-
47	63	99	36	V _{SS_3}	S	-	V _{SS_3}	-	-
48	64	100	1	V _{DD_3}	S	-	V _{DD_3}	-	-

1. I = input, O = output, S = supply, HiZ= high impedance.

2. FT= 5 V tolerant.

3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 11](#).

4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).

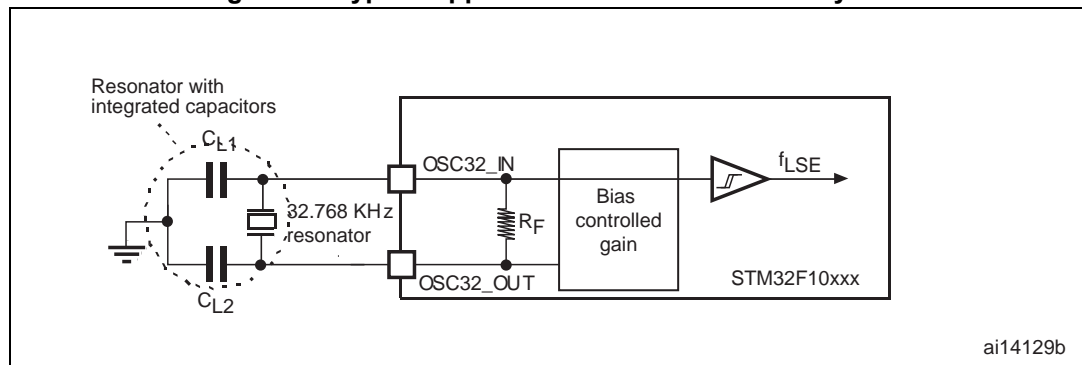
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

7. The pins number 2 and 3 in the VFQFPN36 package, and 5 and 6 in the LQFP48, UFQFPN48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f _{HSI}	Frequency	-		-	8	-	MHz
DuCy _(HSI)	Duty cycle	-		45	-	55	%
ACC _{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register ⁽²⁾		-	-	1 ⁽³⁾	%
		Factory-calibrated (4) (5)	T _A = −40 to 105 °C	−2	-	2.5	%
			T _A = −10 to 85 °C	−1.5	-	2.2	%
			T _A = 0 to 70 °C	−1.3	-	2	%
			T _A = 25 °C	−1.1	-	1.8	%
t _{su(HSI)} ⁽⁴⁾	HSI oscillator startup time	-		1	-	2	μs
I _{DD(HSI)} ⁽⁴⁾	HSI oscillator power consumption	-		-	80	100	μA

1. $V_{DD} = 3.3\text{ V}$, $T_A = -40$ to $105\text{ }^{\circ}\text{C}$ unless otherwise specified.

2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.

3. Guaranteed by design, not tested in production.

4. Based on characterization, not tested in production.

5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	30	40	60	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.65	1.2	μ A

1. $V_{DD} = 3$ V, $T_A = -40$ to 85 °C unless otherwise specified.

2. Based on characterization, not tested in production.

3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in [Table 25](#) are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wakeup from Sleep mode	1.8	μ s
$t_{WUSTOP}^{(1)}$	Wakeup from Stop mode (regulator in run mode)	3.6	μ s
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}^{(1)}$	Wakeup from Standby mode	50	μ s

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min ⁽¹⁾	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock ⁽²⁾	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz

The test results are given in [Table 28](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 28. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 36\text{ MHz}$ conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 36\text{ MHz}$ conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 29. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBμV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 30. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C conforming to JESD22-A114	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 31. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _A = +85 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

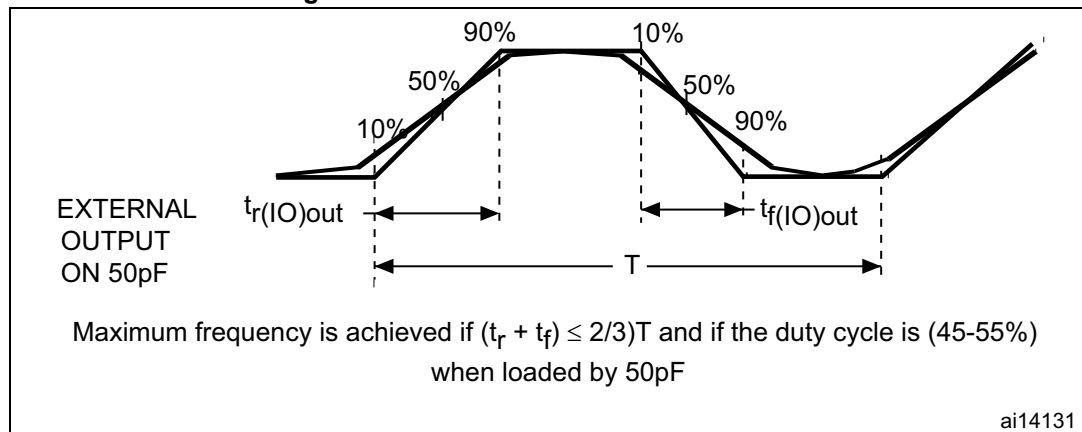
The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 32](#)

Table 32. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I _{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 27. I/O AC characteristics definition



5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 33](#)).

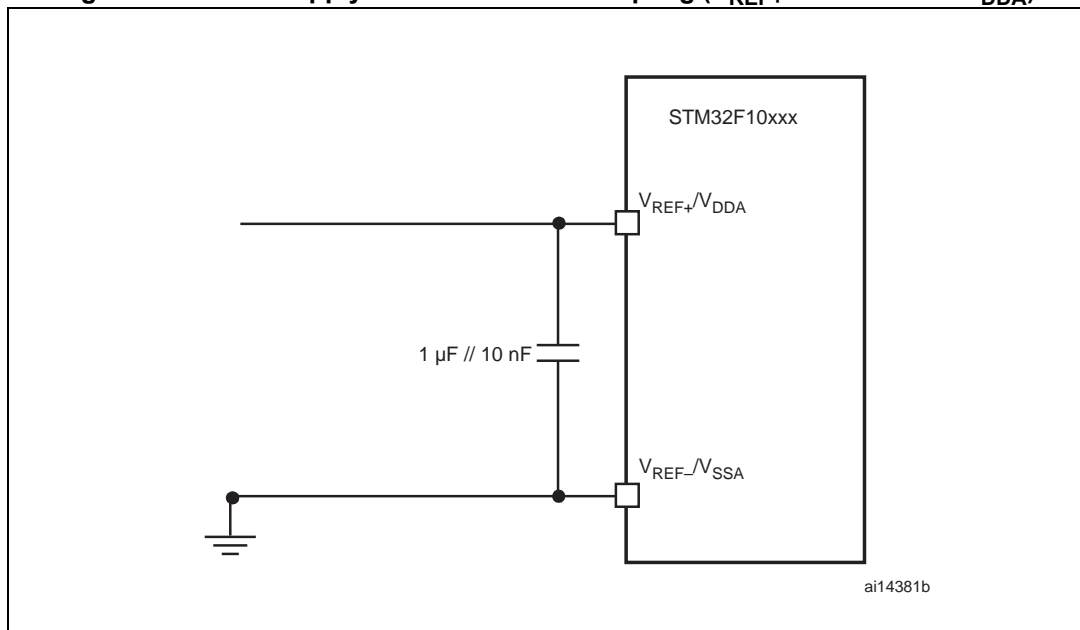
Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	2	-	$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 36. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

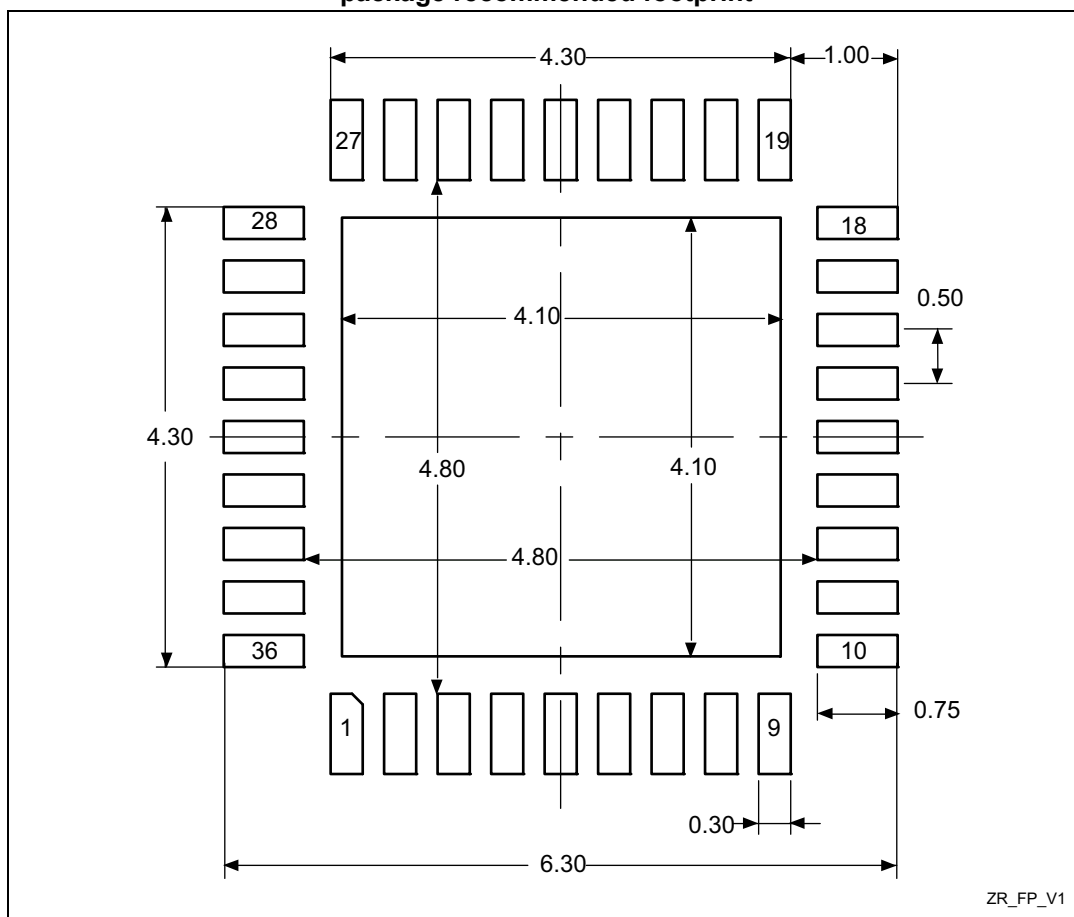
5.3.18 Temperature sensor characteristics

Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.34	1.43	1.52	V
$t_{START}^{(2)}$	Startup time	4	-	10	μs
$T_{S_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	μs

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Figure 41. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.7 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 8: General operating conditions on page 33](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 51. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN 48 - 6 x 6 mm / 0.5 mm pitch	32	
	Thermal resistance junction-ambient VFQFPN 36 - 6 x 6 mm / 0.5 mm pitch	18	

6.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Ordering information scheme

Table 52. Ordering information scheme

Example:	STM32F	101	C	8	T	6	xxx
Device family							
STM32 = ARM-based 32-bit microcontroller							
Product type							
F = general-purpose							
Device subfamily							
101 = access line							
Pin count							
T = 36 pins							
C = 48 pins							
R = 64 pins							
V = 100 pins							
Flash memory size⁽¹⁾							
8 = 64 Kbytes of Flash memory							
B = 128 Kbytes of Flash memory							
Package							
T = LQFP							
U = VFQFPN or UFQFPN							
Temperature range							
6 = Industrial temperature range, –40 to 85 °C.							
Options							
xxx = programmed parts							
TR = tape and real							

1. Although STM32F101x6 devices are not described in this datasheet, orderable part numbers that do not show the A internal code after temperature range code 6 should be referred to this datasheet for the electrical characteristics. The low-density datasheet only covers STM32F101x6 devices that feature the A code.



Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	<p>$V_{ESD(CDM)}$ value added to Table 30: ESD absolute maximum ratings. Note added below Table 10: Embedded reset and power control block characteristics. and below Table 21: HSE 4-16 MHz oscillator characteristics. Note added below Table 34: Output voltage characteristics and V_{OH} parameter description modified. Table 41: ADC characteristics and Table 43: ADC accuracy - limited test conditions modified. Figure 33: ADC accuracy characteristics modified. Packages are ECOPACK® compliant. Tables modified in Section 5.3.5: Supply current characteristics. ADC and ANTI_TAMPER signal names modified (see Table 4: Medium-density STM32F101xx pin definitions). Table 4: Medium-density STM32F101xx pin definitions modified. Note 4 removed and values updated in Table 21: Typical current consumption in Standby mode. V_{hys} modified in Table 33: I/O static characteristics. Updated: Table 28: EMS characteristics and Table 29: EMI characteristics. t_{VDD} modified in Table 9: Operating conditions at power-up / power-down. Typical values modified, note 2 modified and note 3 removed in Table 25: Low-power mode wakeup timings. Maximum current consumption Table 12, Table 13 and Table 14 updated. Values added and notes added in Table 15: Typical and maximum current consumptions in Stop and Standby modes. On-chip peripheral current consumption on page 43 added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see Section 6: Package characteristics). V_{prog} added to Table 27: Flash memory characteristics. T_{S_temp} added to Table 45: TS characteristics. $T_{S_vrefint}$ added to Table 11: Embedded internal reference voltage. Handling of unused pins specified in General input/output characteristics on page 55. All I/Os are CMOS and TTL compliant. Table 4: Medium-density STM32F101xx pin definitions: table clarified and Note 7 modified. Internal LSI RC frequency changed from 32 to 40 kHz (see Table 24: LSI oscillator characteristics). Values added to Table 25: Low-power mode wakeup timings. N_{END} modified in Table 27: Flash memory characteristics. Option byte addresses corrected in Figure 8: Memory map. ACC_{HSI} modified in Table 23: HSI oscillator characteristics. t_{JITTER} removed from Table 26: PLL characteristics. Appendix A: Important notes on page 71 added. Added: Figure 13, Figure 14, Figure 16 and Figure 18.</p>

Table 53. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	<p>Figure 2: Clock tree on page 13 added.</p> <p>CRC added (see CRC (cyclic redundancy check) calculation unit on page 9 and Figure 8: Memory map on page 29 for address).</p> <p>Maximum T_J value given in Table 7: Thermal characteristics on page 33.</p> <p>P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in Table 27: Flash memory characteristics on page 51.</p> <p>I_{DD} modified in Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 39.</p> <p>ACC_{HSI} modified in Table 23: HSI oscillator characteristics on page 49, note 2 removed.</p> <p>t_{RET} modified in Table 27: Flash memory characteristics.</p> <p>$V_{NF(NRST)}$ unit corrected in Table 36: NRST pin characteristics on page 60.</p> <p>Table 40: SPI characteristics on page 65 modified.</p> <p>I_{VREF} added in Table 41: ADC characteristics on page 68.</p> <p>Table 43: ADC accuracy - limited test conditions added. Table 44: ADC accuracy modified.</p> <p>LQFP100 package specifications updated (see Section 6: Package characteristics on page 73).</p> <p>Recommended LQFP100, LQFP64, LQFP48 and VFQFPN36 footprints added (see Figure 44, Figure 47, Figure 50 and Figure 41).</p> <p>Section 6.7: Thermal characteristics on page 90 modified.</p> <p>Appendix A: Important notes removed.</p>
21-Mar-2008	6	<p>Small text changes.</p> <p>In Table 27: Flash memory characteristics:</p> <ul style="list-style-type: none"> – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at $T_A = 55\text{ °C}$ <p>Figure 2: Clock tree corrected. Figure 8: Memory map clarified.</p> <p>V_{25}, Avg_Slope and T_L modified in Table 45: TS characteristics.</p> <p>CRC feature removed.</p>
22-May-2008	7	<p>Section 1: Introduction modified, Section 2.2: Full compatibility throughout the family added. CRC feature added.</p> <p>I_{DD_VBAT} removed from Table 21: Typical current consumption in Standby mode on page 42.</p> <p>Values added to Table 39: SCL frequency ($f_{PCLK1} = 36\text{ MHz}$, $V_{DD_I2C} = 3.3\text{ V}$) on page 64.</p> <p>Figure 30: SPI timing diagram - slave mode and $CPHA = 0$ on page 66 modified. Equation 1 corrected.</p> <p>Section 6.7.2: Evaluating the maximum junction temperature for an application on page 91 added.</p> <p>Axx option added to Table 52: Ordering information scheme on page 92.</p>