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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vbt6tr

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 35*, respectively.

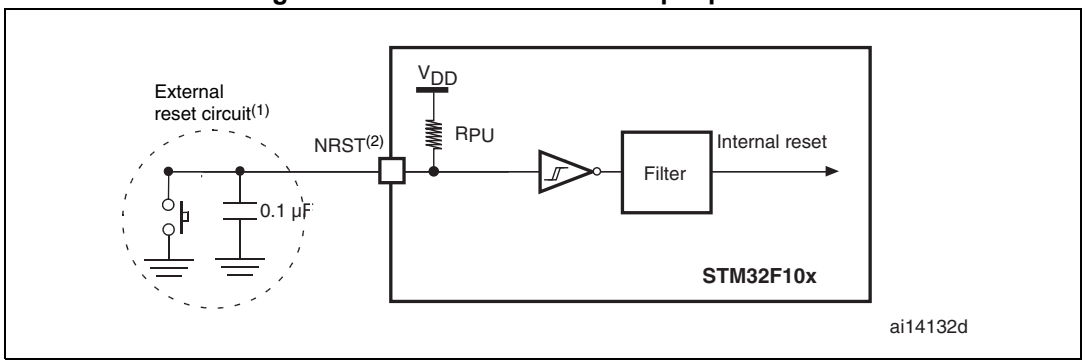
Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 35. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 27*.
3. Guaranteed by design, not tested in production.

Figure 28. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

Figure 30. SPI timing diagram - slave mode and CPHA = 0

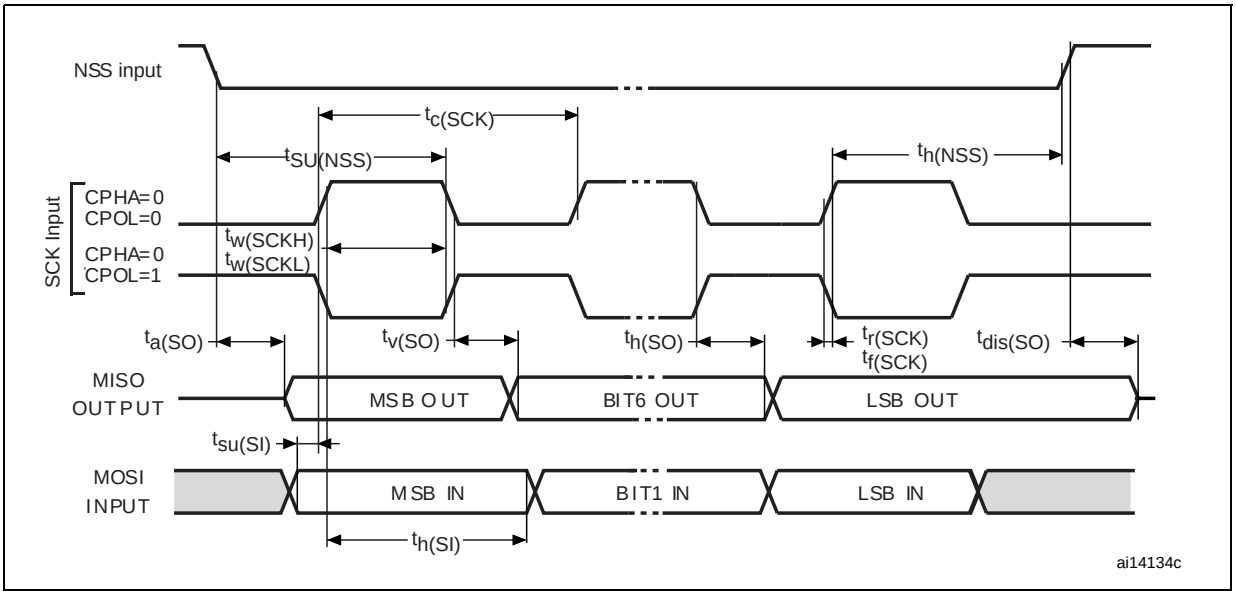
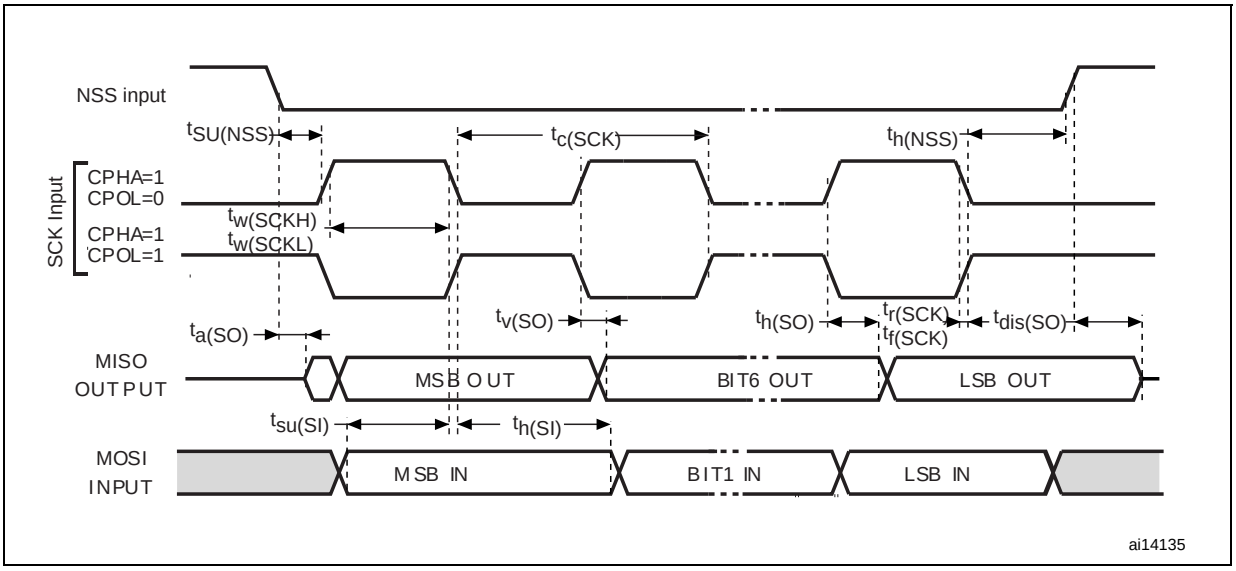
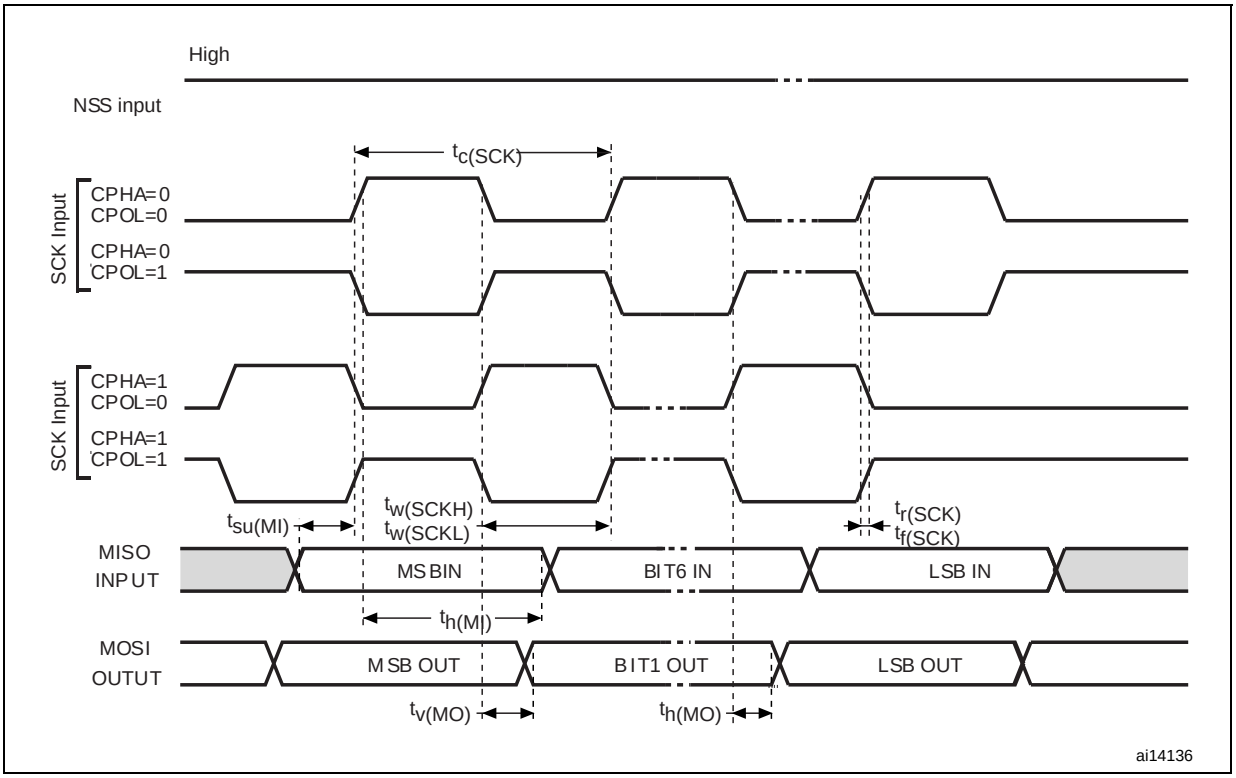


Figure 31. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 32. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

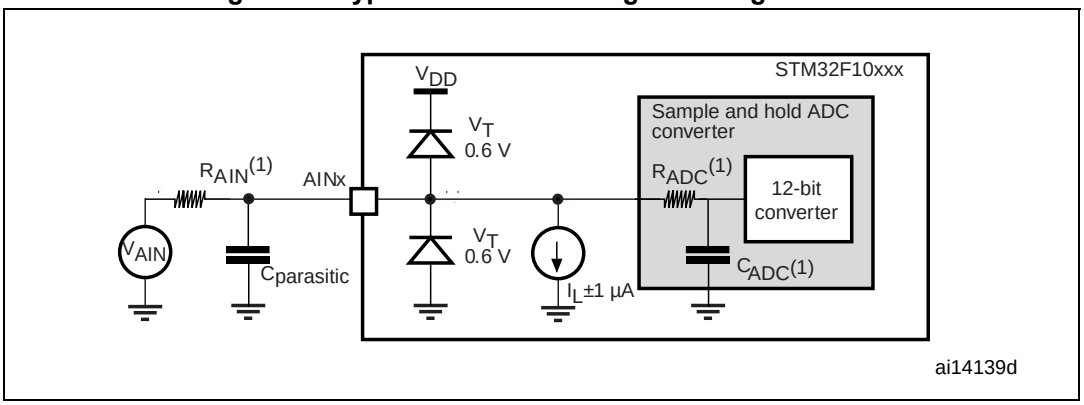
Note: It is recommended to perform a calibration after each power-up.

Table 41. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 42* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin description* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 41*.

Figure 34. Typical connection diagram using the ADC

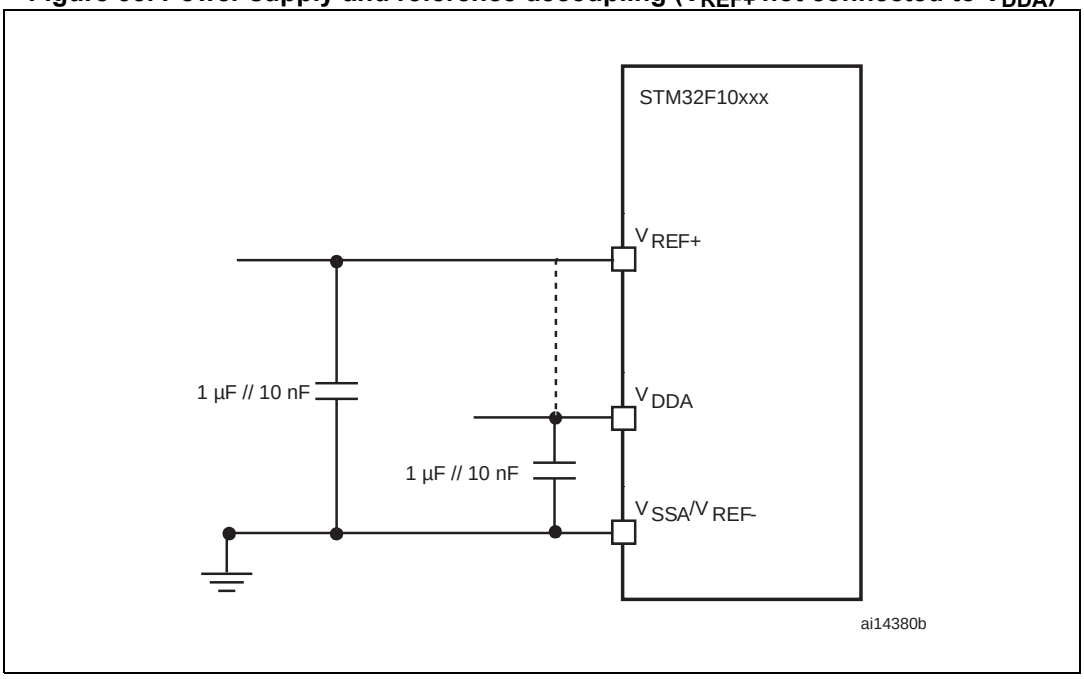


1. Refer to *Table 41* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 35* or *Figure 36*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 35. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

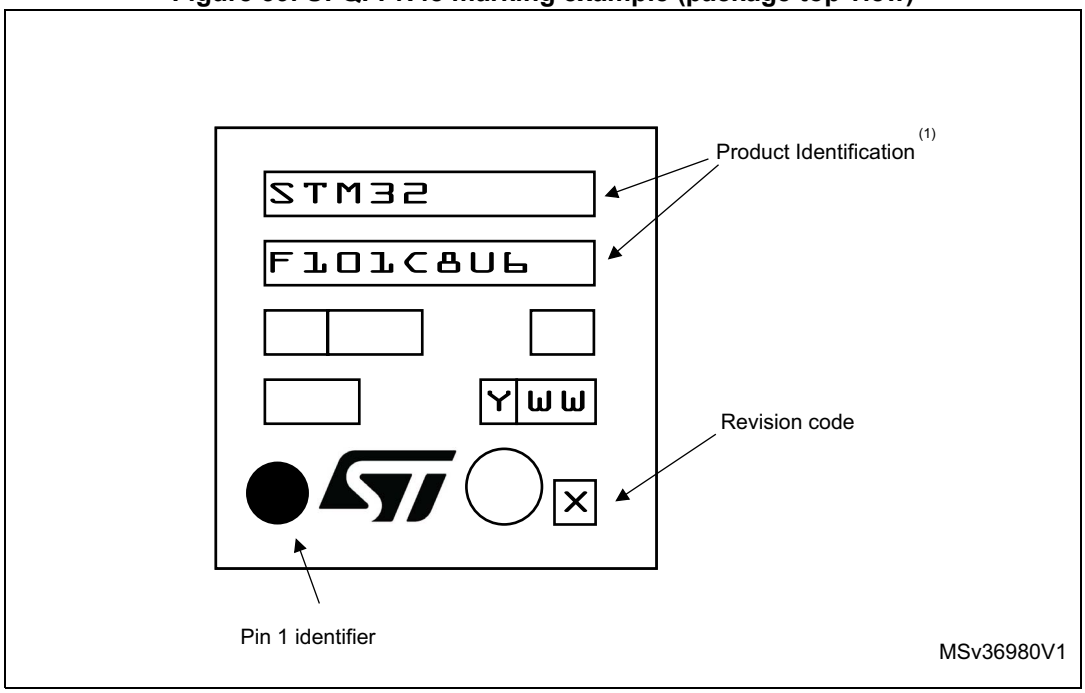


1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Device Marking for UFQFPN48

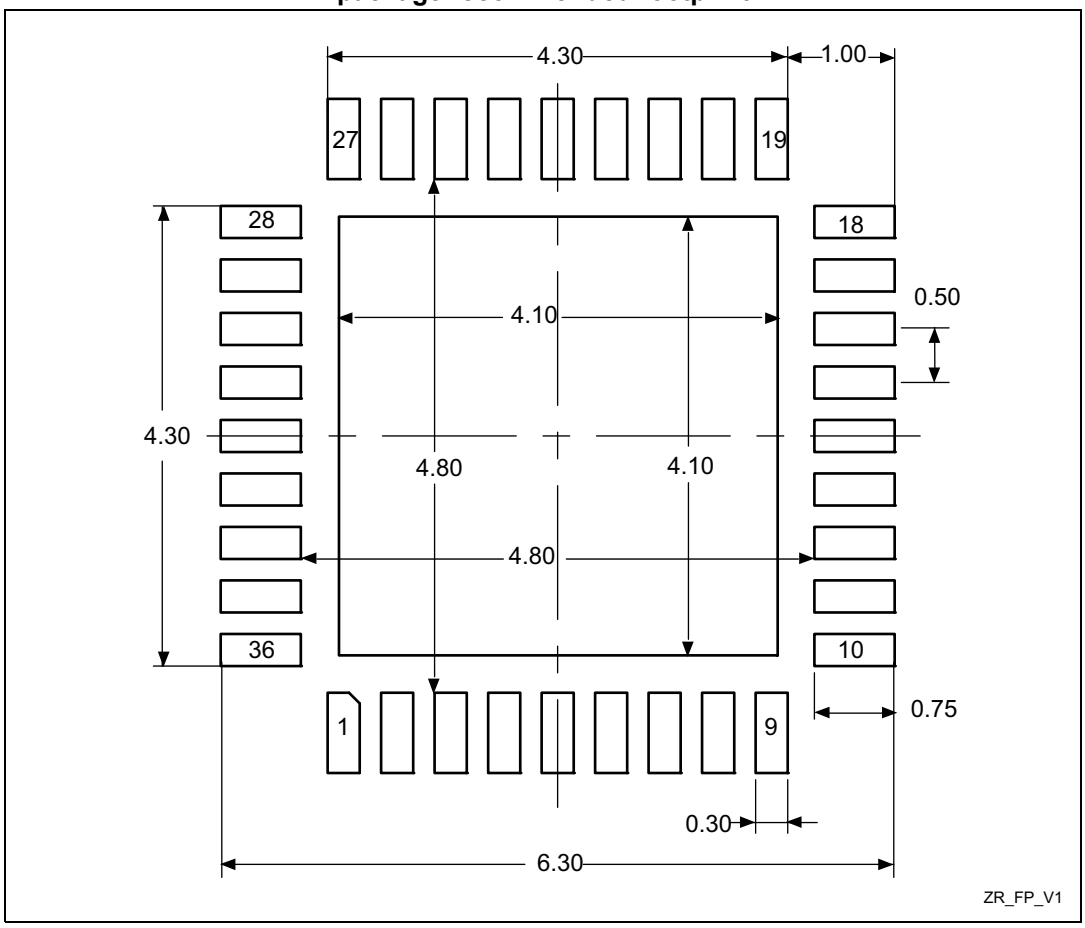
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. UFQFPN48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

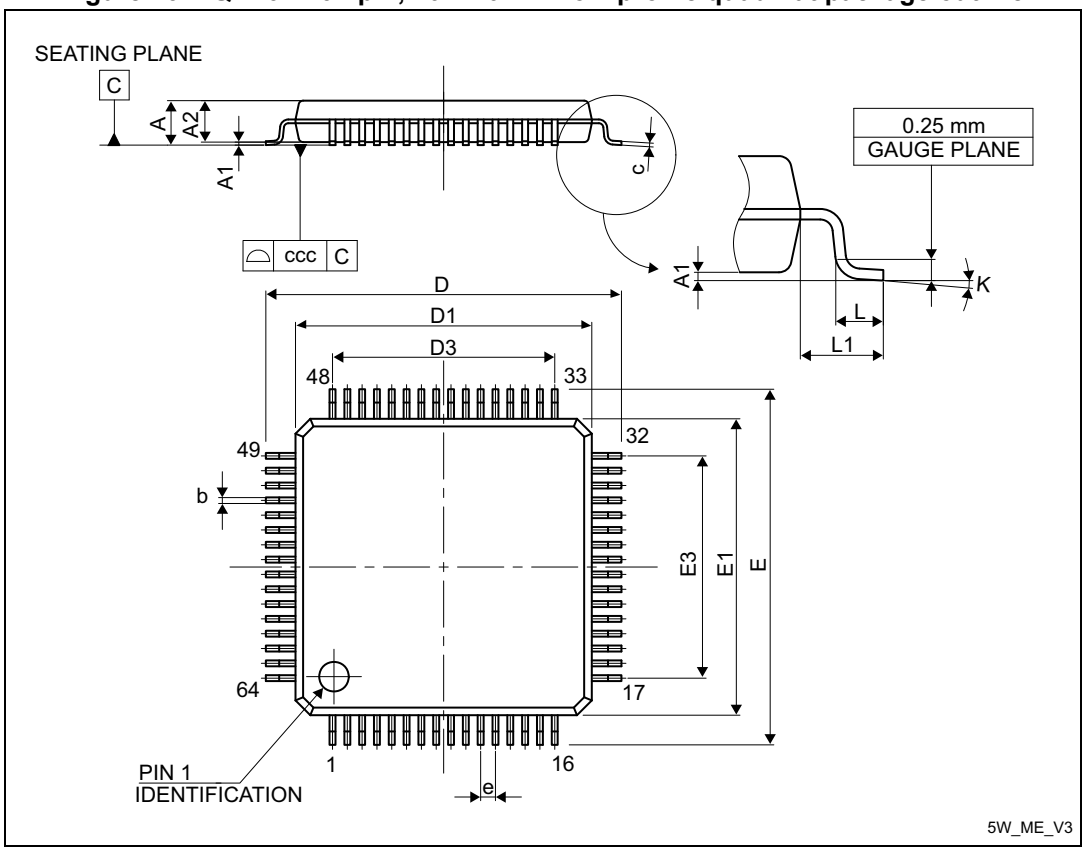
Figure 41. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.5 LQFP64 package information

Figure 46. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

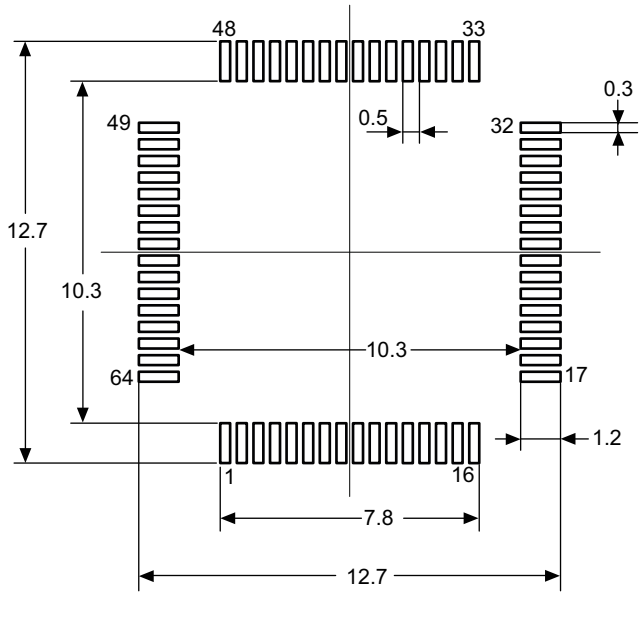
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

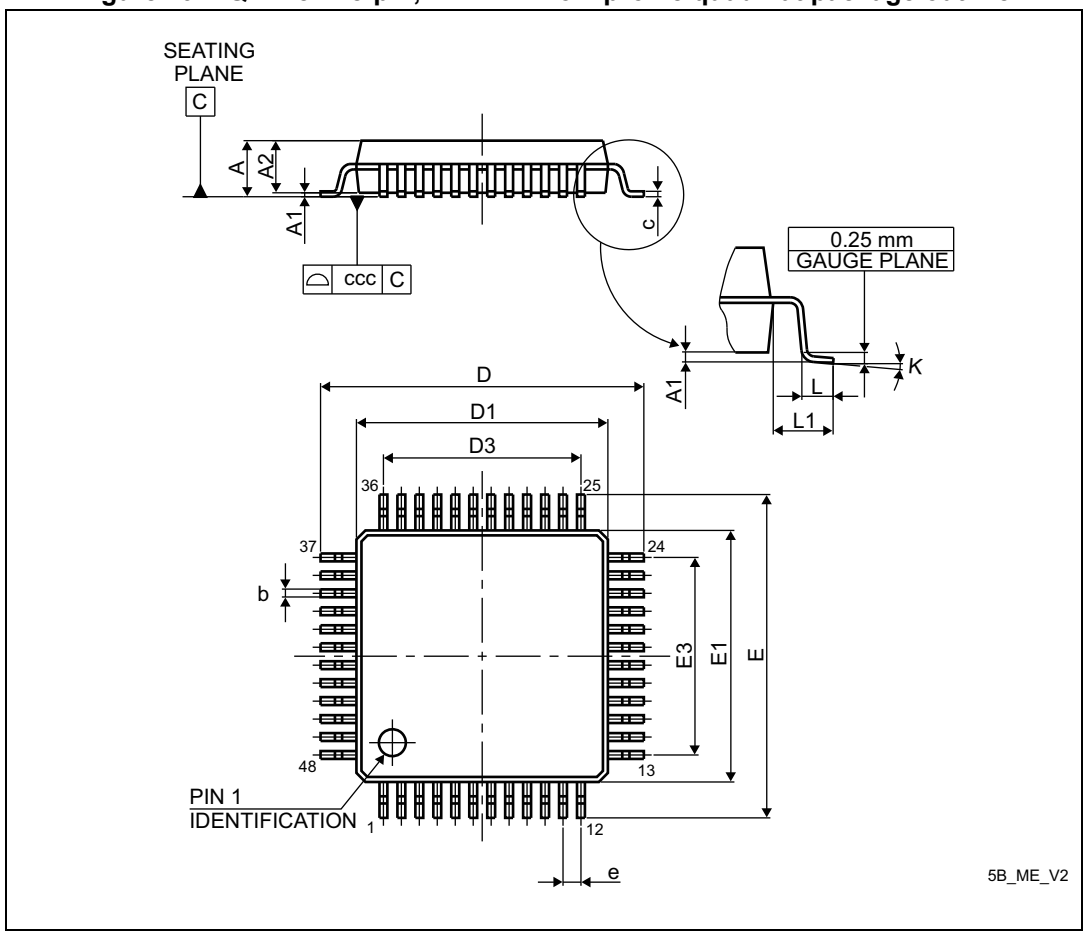
Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.6 LQFP48 package information

Figure 49. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

6.7.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 52: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F101xx junction temperature range.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

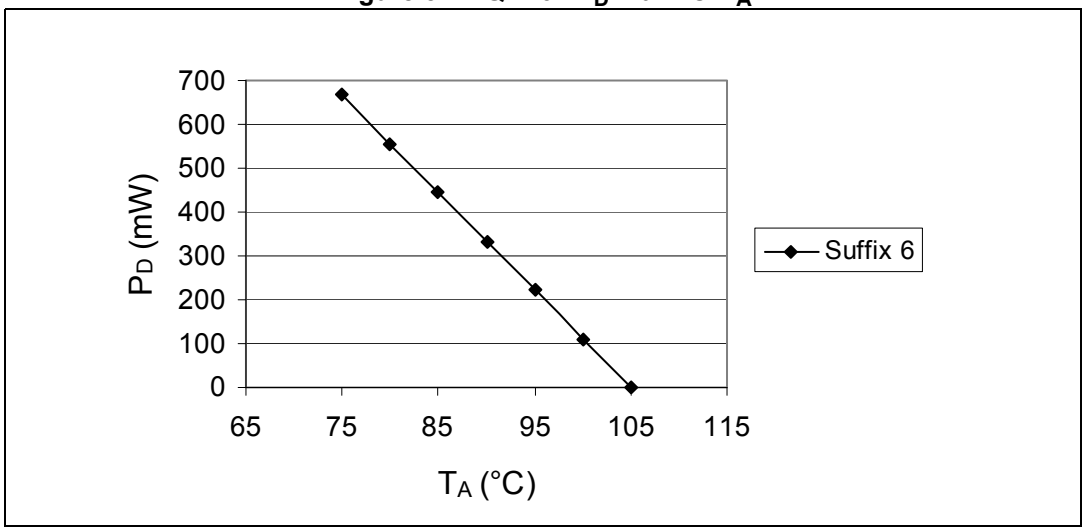
Using the values obtained in *Table 51* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F101xx (–40 < T_J < 105 °C).

Figure 52. LQFP64 P_D max vs. T_A



For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	$V_{ESD(CDM)}$ value added to *Table 30: ESD absolute maximum ratings*. Note added below *Table 10: Embedded reset and power control block characteristics*. and below *Table 21: HSE 4-16 MHz oscillator characteristics*. Note added below *Table 34: Output voltage characteristics* and V_{OH} parameter description modified. *Table 41: ADC characteristics* and *Table 43: ADC accuracy - limited test conditions* modified. *Figure 33: ADC accuracy characteristics* modified. Packages are ECOPACK® compliant. Tables modified in *Section 5.3.5: Supply current characteristics*. ADC and ANTI_TAMPER signal names modified (see *Table 4: Medium-density STM32F101xx pin definitions*). *Table 4: Medium-density STM32F101xx pin definitions* modified. Note 4 removed and values updated in *Table 21: Typical current consumption in Standby mode*. V_{hys} modified in *Table 33: I/O static characteristics*. Updated: *Table 28: EMS characteristics* and *Table 29: EMI characteristics*. t_{VDD} modified in *Table 9: Operating conditions at power-up / power-down*. Typical values modified, note 2 modified and note 3 removed in *Table 25: Low-power mode wakeup timings*. Maximum current consumption *Table 12*, *Table 13* and *Table 14* updated. Values added and notes added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *On-chip peripheral current consumption on page 43* added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). V_{prog} added to *Table 27: Flash memory characteristics*. T_{S_temp} added to *Table 45: TS characteristics*. $T_{S\_vrefint}$ added to *Table 11: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 55*. All I/Os are CMOS and TTL compliant. *Table 4: Medium-density STM32F101xx pin definitions*: table clarified and *Note 7* modified. Internal LSI RC frequency changed from 32 to 40 kHz (see *Table 24: LSI oscillator characteristics*). Values added to *Table 25: Low-power mode wakeup timings*. N_{END} modified in *Table 27: Flash memory characteristics*. Option byte addresses corrected in *Figure 8: Memory map*. ACC_{HSI} modified in *Table 23: HSI oscillator characteristics*. t_{JITTER} removed from *Table 26: PLL characteristics*. *Appendix A: Important notes on page 71* added. Added: *Figure 13*, *Figure 14*, *Figure 16* and *Figure 18*.

Table 53. Document revision history (continued)

Date	Revision	Changes
22-Nov-2007	4	Document status promoted from preliminary data to datasheet. Small text changes. STM32F101CB part number corrected in *Table 1: Device summary*. Number of communication peripherals corrected for STM32F101Tx in *Table 2: Device features and peripheral counts (STM32F101xx medium-density access line)* and Number of GPIOs corrected for LQFP package. *Power supply schemes on page 16* modified. Main function and default alternate function modified for PC14 and PC15 in *Table 4: Medium-density STM32F101xx pin definitions*, *Note 6* added, Remap column added. *Figure 11: Power supply scheme* modified. $V_{DD} – V_{SS}$ ratings modified and *Note 1* modified in *Table 5: Voltage characteristics*. *Note 1* modified in *Table 6: Current characteristics*. *Note 2* added in *Table 10: Embedded reset and power control block characteristics*. 48 and 72 MHz frequencies removed from *Table 12*, *Table 13* and *Table 14*. MCU ‘s operating conditions modified in *Typical current consumption on page 42*. I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. Note added in *Table 16 on page 42* and *Table 17 on page 43*. *Table 18: Peripheral current consumption* modified. *Figure 17: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* added. Note removed below *Figure 30: SPI timing diagram - slave mode and CPHA = 0*. Note added below *Figure 31: SPI timing diagram - slave mode and CPHA = 1(1)*. *Figure 34: Typical connection diagram using the ADC* modified. $t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in *Table 21* and *Table 22*, respectively. Maximum values removed from *Table 25: Low-power mode wakeup timings*. t_{RET} conditions modified in *Table 27: Flash memory characteristics*. Conditions modified in *Table 28: EMS characteristics*. Impedance size specified in *A.4: Voltage glitch on ADC input 0 on page 71*. Small text changes in *Table 34: Output voltage characteristics*. *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)* updated. Details on unused pins removed from *General input/output characteristics on page 55*. *Table 40: SPI characteristics* updated. Notes added and I_{lkg} removed in *Table 41: ADC characteristics*. Note added in *Table 42* and *Table 45*. *Note 3* and *Note 2* added below *Table 43: ADC accuracy - limited test conditions*. Avg_Slope and V_{25} modified in *Table 45: TS characteristics*. Θ_{JA}value for VFQFPN36 package added in *Table 51: Package thermal characteristics*. *I2C interface characteristics on page 62* modified. Order codes replaced by *Section 7: Ordering information scheme*.

Table 53. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	*Figure 2: Clock tree on page 13* added. CRC added (see *CRC (cyclic redundancy check) calculation unit on page 9* and *Figure 8: Memory map on page 29* for address). Maximum T_J value given in *Table 7: Thermal characteristics on page 33*. P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in *Table 27: Flash memory characteristics on page 51*. I_{DD} modified in *Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 39*. ACC_{HSI} modified in *Table 23: HSI oscillator characteristics on page 49*, note 2 removed. t_{RET} modified in *Table 27: Flash memory characteristics*. $V_{NF(NRST)}$ unit corrected in *Table 36: NRST pin characteristics on page 60*. *Table 40: SPI characteristics on page 65* modified. I_{VREF} added in *Table 41: ADC characteristics on page 68*. *Table 43: ADC accuracy - limited test conditions* added. *Table 44: ADC accuracy* modified. LQFP100 package specifications updated (see *Section 6: Package characteristics on page 73*). Recommended LQFP100, LQFP64, LQFP48 and VFQFPN36 footprints added (see *Figure 44*, *Figure 47*, *Figure 50* and *Figure 41*). *Section 6.7: Thermal characteristics on page 90* modified. *Appendix A: Important notes* removed.
21-Mar-2008	6	Small text changes. In *Table 27: Flash memory characteristics*: – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at T_A = 55 °C *Figure 2: Clock tree* corrected. *Figure 8: Memory map* clarified. V_{25}, Avg_Slope and T_L modified in *Table 45: TS characteristics*. CRC feature removed.
22-May-2008	7	*Section 1: Introduction* modified, *Section 2.2: Full compatibility throughout the family* added. CRC feature added. I_{DD_VBAT} removed from *Table 21: Typical current consumption in Standby mode on page 42*. Values added to *Table 39: SCL frequency (fPCLK1= 36 MHz, VDD_I2C = 3.3 V) on page 64*. *Figure 30: SPI timing diagram - slave mode and CPHA = 0 on page 66* modified. *Equation 1* corrected. *Section 6.7.2: Evaluating the maximum junction temperature for an application on page 91* added. Axx option added to *Table 52: Ordering information scheme on page 92*.

Table 53. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	8	Small text changes. *Power supply supervisor on page 16* modified and V_{DDA} added to *Table 8: General operating conditions on page 33*. Capacitance modified in *Figure 11: Power supply scheme on page 31*. Table notes revised in *Section 5: Electrical characteristics*. Maximum value of $t_{RSTTEMPO}$ modified in *Table 10: Embedded reset and power control block characteristics on page 35*. Values added to *Table 15: Typical and maximum current consumptions in Stop and Standby modes* and *Table 21: Typical current consumption in Standby mode* removed. f_{HSE_ext} modified in *Table 19: High-speed external user clock characteristics on page 45*. f_{PLL_IN} modified in *Table 26: PLL characteristics on page 50*. f_{HCLK} corrected in *Table 28: EMS characteristics*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 38: I2C characteristics on page 63*, note 1 modified. $t_{h(NSS)}$ modified in *Table 40: SPI characteristics on page 65* and *Figure 30: SPI timing diagram - slave mode and CPHA = 0 on page 66*. C_{ADC} modified in *Table 41: ADC characteristics on page 68* and *Figure 34: Typical connection diagram using the ADC* modified. f_{PCLK2} corrected in *Table 43: ADC accuracy - limited test conditions* and *Table 44: ADC accuracy*. Typical T_{S_temp} value removed from *Table 45: TS characteristics on page 72*. LQFP48 package specifications updated (see *Table 50*, *Table 49* and *Table 50*). Axx option removed from *Table 52: Ordering information scheme on page 92*.
24-Jul-2008	9	First page modified: “Up to 2 x I²C interfaces” instead of “1 x I²C interface”
23-Sep-2008	10	STM32F101xx devices with 32 Kbyte Flash memory capacity removed, document updated accordingly. *Section 2.2: Full compatibility throughout the family on page 14* updated. Notes modified in *Table 4: Medium-density STM32F101xx pin definitions on page 24*. *Note 2* modified below *Table 5: Voltage characteristics on page 32*, $\lvert\Delta V_{DDx}\rvert$ min and $\lvert\Delta V_{DDx}\rvert$ min removed. *Note 2* added to *Table 8: General operating conditions on page 33*. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 36*. I_{DD} in standby mode at 85 °C modified in *Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 39*. *General input/output characteristics on page 55* modified. Note added below *Table 52: Ordering information scheme*. *Section 7.1: Future family enhancements* removed. Small text changes.