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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865lti-058">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865lti-058</a>

### 4.3.1 Instruction Set Summary

#### 4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. [Table 4-1](#) lists the different arithmetic instructions.

**Table 4-1. Arithmetic Instructions**

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

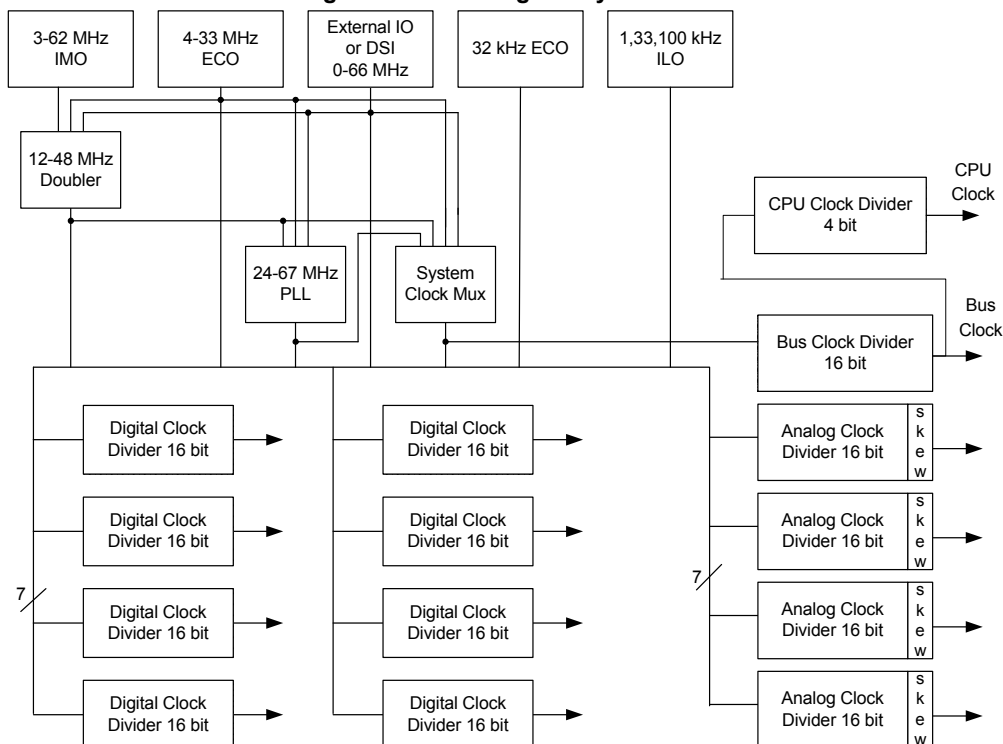
#### 4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. [Table 4-2](#) shows the list of logical instructions and their description.

**Table 4-2. Logical Instructions**

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3

**Figure 6-1. Clocking Subsystem**



### 6.1.1 Internal Oscillators

#### 6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its  $\pm 1$ -percent accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from  $\pm 1$  percent at 3 MHz, up to  $\pm 7$  percent at 62 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency (see PLL). The IMO provides clock outputs at 3, 6, 12, 24, 48, and 62 MHz.

#### 6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works for input frequency ranges of 6 to 24 MHz (providing 12 to 48 MHz at the output). It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin). The doubler is typically used to clock the USB.

#### 6.1.1.3 PLL

The PLL allows low-frequency, high-accuracy clocks to be multiplied to higher frequencies. This is a trade off between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250  $\mu$ s (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low-power modes.

#### 6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low-power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz. The 1-kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low-power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

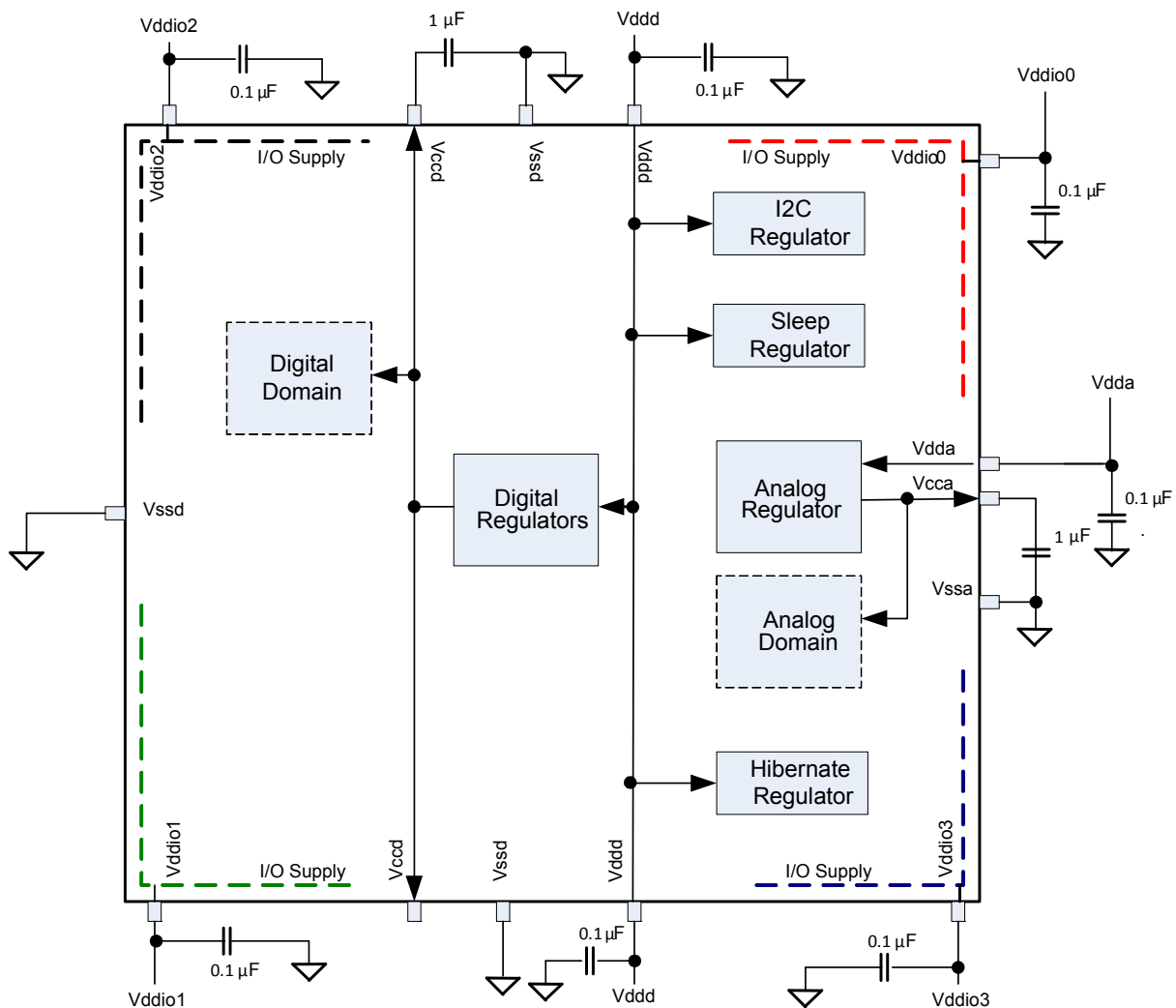
The central timewheel is a 1-kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled, except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low-power mode. Firmware can reset the central timewheel. Systems that require accurate timing should use the RTC capability instead of the central timewheel.

The 100-kHz clock (CLK100K) works as a low-power system clock to run the CPU. It can also generate time intervals such as fast sleep intervals using the fast timewheel. The fast timewheel is a 100-kHz, 5-bit counter clocked by the ILO that can also be used to wake the system. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic wakeups of the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached.

## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled Vdda, Vddd, and Vddiox, respectively. It also includes two internal 1.8-V regulators that provide the digital (Vccd) and analog (Vcca) supplies for the internal core logic. The output pins of the regulators (Vccd and Vcca) and the Vddio pins must have capacitors connected as shown in [Figure 6-4](#). The two Vccd pins must be shorted together, with as short a trace as possible, and connected to a 1-μF ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I<sup>2</sup>C regulator, and a hibernate regulator.

**Figure 6-4. PSoC Power System**



**Note** The two Vccd pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in [Figure 2-6](#) on page 10.

voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. The converter can be configured to provide low-power, low-current regulation in the standby mode. The external 32-kHz crystal can be used to generate inductor boost pulses on the rising and falling edge of the clock when the output voltage is less than the programmed value. This is called automatic thump mode (ATM).

The boost typically draws 200  $\mu$ A in active mode and 12  $\mu$ A in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize the total chip power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

**Table 6-4. Chip and Boost Power Modes Compatibility**

Chip Power Modes	Boost Power Modes
Chip – Active mode	Boost can be operated in either active or standby mode.
Chip – Sleep mode	Boost can be operated in either active or standby mode. However, it is recommended to operate boost in standby mode for low-power consumption
Chip – Hibernate mode	Boost can only be operated in active mode. However, it is recommended not to use boost in chip hibernate mode due to high current consumption in boost active mode

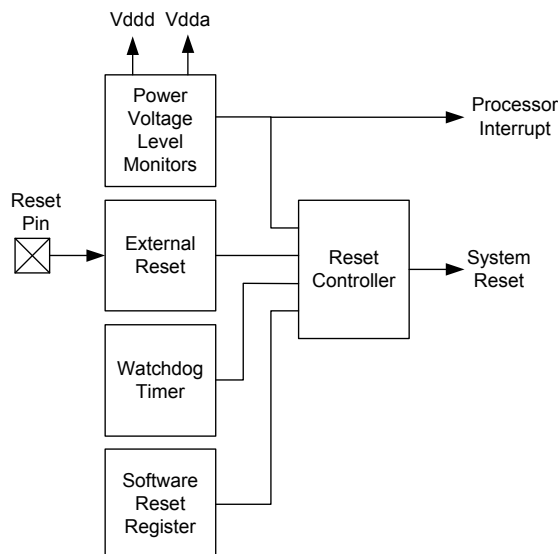
If the boost converter is not used in a given application, tie the Vbat, Vssb, and Vboost pins to ground and leave the Ind pin unconnected.

### 6.3 Reset

CY8C38 has multiple internal and external reset sources available. The reset sources are:

- **Power source monitoring** – The analog and digital power voltages, Vdda, Vddd, Vcca, and Vccd are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- **External** – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to Vddio1. Vddd, Vdda, and Vddio1 must all have voltage applied before the part comes out of reset.
- **Watchdog timer** – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- **Software** – The device can be reset under program control.

**Figure 6-7. Resets**



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register holds the source of the most recent reset or power voltage monitoring interrupt. The program may examine this register to detect and report exception conditions. This register is cleared after a power-on reset.

#### 6.3.1 Reset Sources

##### 6.3.1.1 Power Voltage Level Monitors

###### ■ IPOR – Initial power-on reset

At initial power on, IPOR monitors the power voltages V<sub>DDP</sub> and V<sub>DDA</sub>, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

To save power the IPOR circuit is disabled when the internal digital supply is stable. Voltage supervision is then handed off to the precise low voltage reset (PRES) circuit. When the voltage is high enough for PRES to release, the IMO starts.

###### ■ PRES – Precise low voltage reset

This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

■ **ALVI, DLVI, AHVI – Analog/digital low voltage interrupt, analog high voltage interrupt**

Interrupt circuits are available to detect when V<sub>DDA</sub> and V<sub>DDD</sub> go outside a voltage range. For AHVI, V<sub>DDA</sub> is compared to a fixed trip level. For ALVI and DLVI, V<sub>DDA</sub> and V<sub>DDD</sub> are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

**Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt**

Interrupt	Supply	Normal Voltage Range	Available Trip Settings	Accuracy
DLVI	V <sub>DDD</sub>	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
ALVI	V <sub>DDA</sub>	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
AHVI	V <sub>DDA</sub>	1.71 V–5.5 V	5.75 V	±2%

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

**6.3.1.2 Other Reset Sources**

■ **XRES – External reset**

PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

■ **SRES – Software reset**

A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

Another register bit exists to disable this function.

■ **DRES – Digital logic reset**

A logic signal can be routed from the UDBs or other digital peripheral source through the DSI to the Configurable XRES pin, P1[2], to generate a hardware-controlled reset. The pin must be placed in XRES mode. The response to a DRES is the same as after an IPOR reset.

■ **WRES – Watchdog timer reset**

The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

**Note** IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

**Note**

14. GPIOs with opamp outputs are not recommended for use with CapSense.

**6.4 I/O System and Routing**

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the V<sub>DDIO</sub> pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense<sup>[14]</sup>, and LCD segment drive, while SIO pins are used for voltages in excess of V<sub>DDA</sub> and for programmable output voltages.

■ **Features supported by both GPIO and SIO:**

- User programmable port reset state
- Separate I/O supplies and voltages for up to four groups of I/O
- Digital peripherals use DSI to connect the pins
- Input or output or both for CPU and DMA
- Eight drive modes
- Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
- Dedicated port interrupt vector for each port
- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis

■ **Additional features only provided on the GPIO pins:**

- LCD segment drive on LCD equipped devices
- CapSense<sup>[14]</sup>
- Analog input and output capability
- Continuous 100 µA clamp current capability
- Standard drive strength down to 1.7 V

■ **Additional features only provided on SIO pins:**

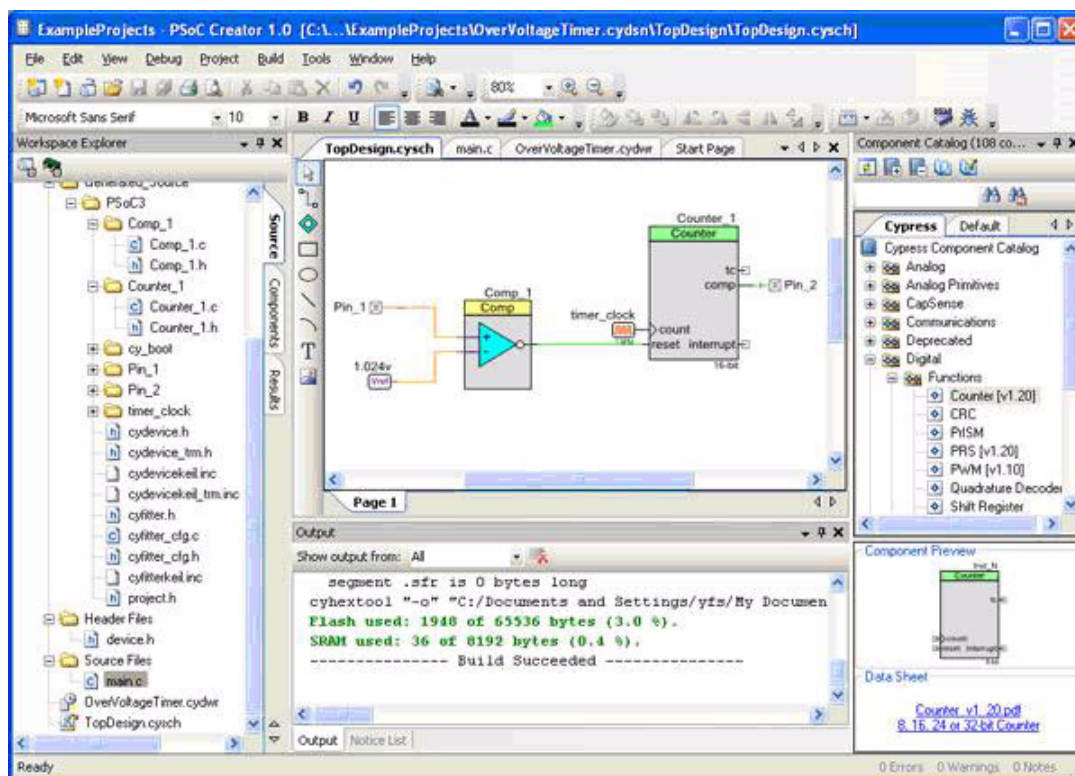
- Higher drive strength than GPIO
- Hot swap capability (5 V tolerance at any operating V<sub>DD</sub>)
- Programmable and regulated high input and output drive levels down to 1.2 V
- No analog input, CapSense, or LCD capability
- Over voltage tolerance up to 5.5 V
- SIO can act as a general purpose analog comparator

■ **USBIO features:**

- Full speed USB 2.0 compliant I/O
- Highest drive strength for general purpose use
- Input, output, or both for CPU and DMA
- Input, output, or both for digital peripherals
- Digital output (CMOS) drive mode
- Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

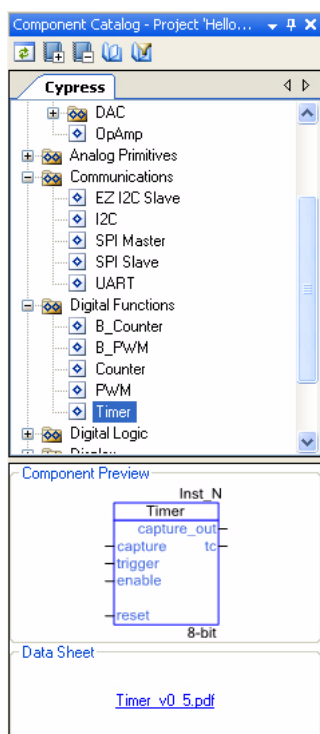


**Figure 7-2. PSoC Creator Framework**



#### 7.1.4.2 Component Catalog

**Figure 7-3. Component Catalog**

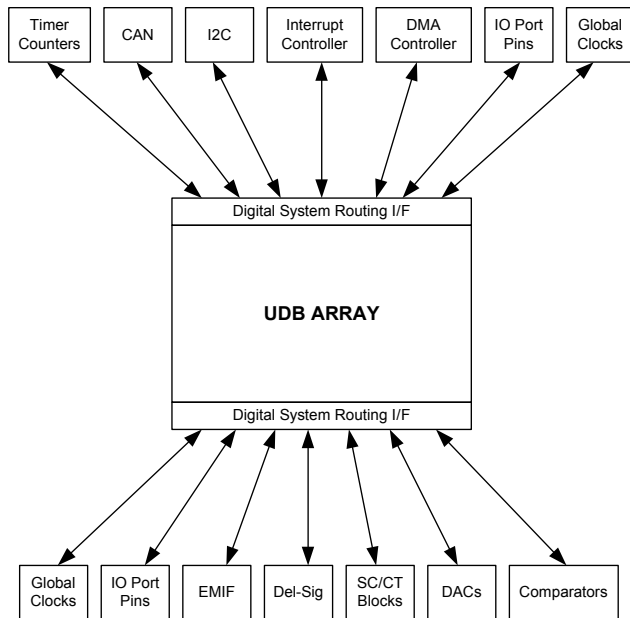


The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I<sup>2</sup>C, USB, and CAN. See [Example Peripherals](#) on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

#### 7.1.4.3 Design Reuse

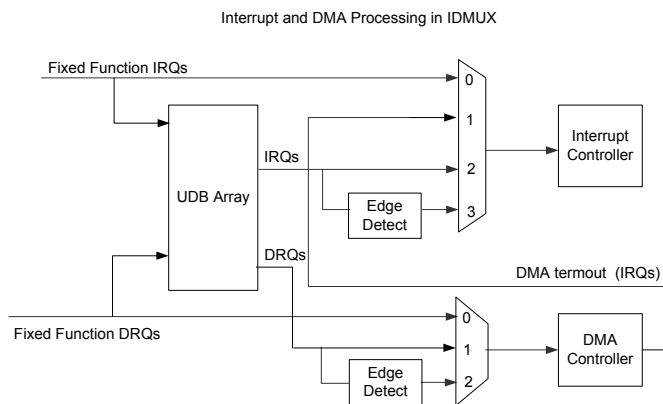
The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

**Figure 7-13. Digital System Interconnect**



Interrupt and DMA routing is very flexible in the CY8C38 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-14 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

**Figure 7-14. Interrupt and DMA Processing in the IDMUX**



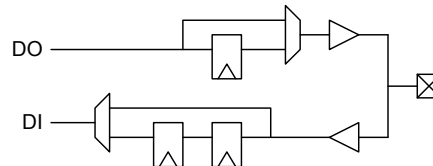
#### 7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

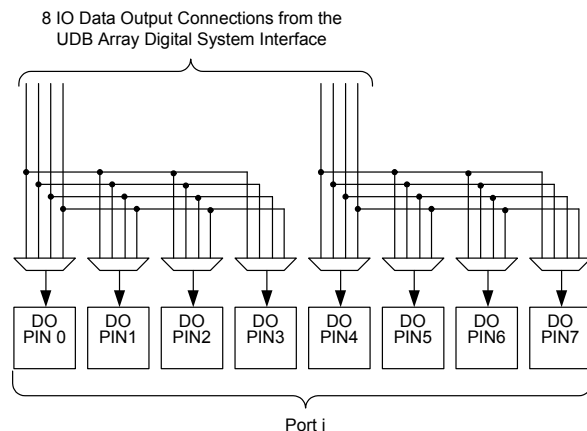
When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be

single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the system clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

**Figure 7-15. I/O Pin Synchronization Routing**

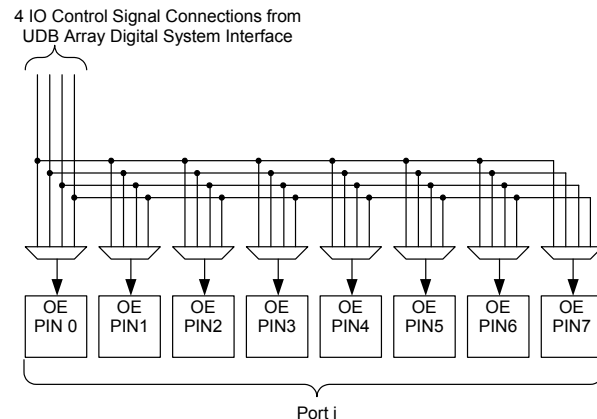


**Figure 7-16. I/O Pin Output Connectivity**



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

**Figure 7-17. I/O Pin Output Enable Connectivity**





**Pin Connection Diagram for STM32F769I-DT**

**Legend:**

- Switch Resistance: Small (~870 Ohms) (○), Large (~200 Ohms) (●)
- Mux Group: Ind, Vssb, Vbat, Vboost, Vssd, XRES

**Notes:**

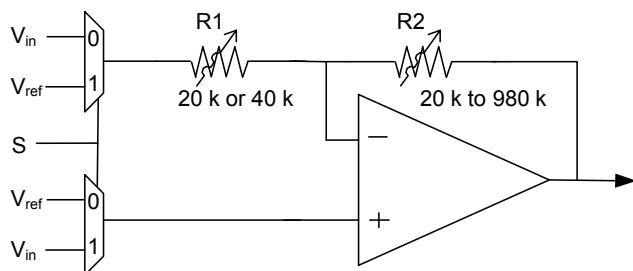
- \* Denotes pins on all packages
- LCD signals are not shown.

**Rev #51**

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

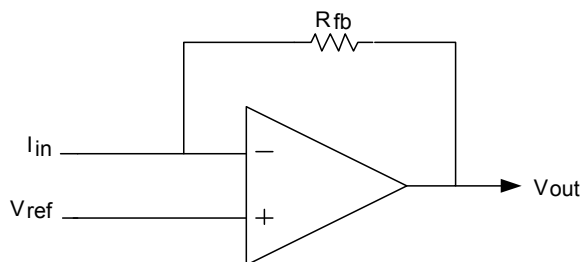
#### 8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current  $I_{in}$ , the output voltage is  $I_{in} \times R_{fb} + V_{REF}$ , where  $V_{REF}$  is the value placed on the non inverting input. The feedback resistor  $R_{fb}$  is programmable between 20 K $\Omega$  and 1 M $\Omega$  through a configuration register. Table 8-4 shows the possible values of  $R_{fb}$  and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal $R_{fb}$ (K $\Omega$ )
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the  $V_{REF}$  TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

## 8.6 LCD Direct Drive

The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane  $\times$  46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

### 9.3 Debug Features

Using the JTAG or SWD interface, the CY8C38 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Debug operations are possible while the device is reset, or in low-power modes
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C38 compatible with other popular third-party tools (for example, ARM / Keil)

### 9.4 Trace Features

The CY8C38 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

### 9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

### 9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect

firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

### 9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 18). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

#### Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

#### 11.4.2 SIO

**Table 11-11. SIO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and Vddd, see Section 11.2.1	–	–	5.5	V
Vinref	Input voltage reference (Differential input mode)		0.5	–	$0.52 \times V_{DDIO}$	V
Voutref	Output voltage reference (Regulated output mode)					
		$V_{DDIO} > 3.7$	1	–	$V_{DDIO} - 1$	V
		$V_{DDIO} < 3.7$	1	–	$V_{DDIO} - 0.5$	V
V <sub>IH</sub>	Input voltage high threshold					
	GPIO mode	CMOS input	$0.7 \times V_{DDIO}$	–	–	V
	Differential input mode <sup>[30]</sup>	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V <sub>IL</sub>	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	$0.3 \times V_{DDIO}$	V
	Differential input mode <sup>[30]</sup>	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V <sub>OH</sub>	Output voltage high					
	Unregulated mode	$I_{OH} = 4 \text{ mA}$ , $V_{DDIO} = 3.3 \text{ V}$	$V_{DDIO} - 0.4$	–	–	V
	Regulated mode <sup>[30]</sup>	$I_{OH} = 1 \text{ mA}$	SIO_ref – 0.65	–	SIO_ref + 0.2	V
	Regulated mode <sup>[30]</sup>	$I_{OH} = 0.1 \text{ mA}$	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V <sub>OL</sub>	Output voltage low					
		$V_{DDIO} = 3.30 \text{ V}$ , $I_{OL} = 25 \text{ mA}$	–	–	0.8	V
		$V_{DDIO} = 1.80 \text{ V}$ , $I_{OL} = 4 \text{ mA}$	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I <sub>IL</sub>	Input leakage current (Absolute value) <sup>[31]</sup>					
	$V_{IH} \leq V_{DDIO}$	25 °C, Vddsio = 3.0 V, $V_{IH} = 3.0 \text{ V}$	–	–	14	nA
	$V_{IH} > V_{DDIO}$	25 °C, Vddsio = 0 V, $V_{IH} = 3.0 \text{ V}$	–	–	10	μA
C <sub>IN</sub>	Input Capacitance <sup>[31]</sup>		–	–	7	pF
V <sub>H</sub>	Input voltage hysteresis (Schmitt-Trigger) <sup>[31]</sup>	Single ended mode (GPIO mode)	–	40	–	mV
		Differential mode	–	35	–	mV
Idiode	Current through protection diode to V <sub>SSIO</sub>		–	–	100	μA

**Table 11-12. SIO AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in fast strong mode (90/10%) <sup>[31]</sup>	Clod = 25 pF, $V_{DDIO} = 3.3 \text{ V}$	–	–	12	ns
TfallF	Fall time in fast strong mode (90/10%) <sup>[31]</sup>	Clod = 25 pF, $V_{DDIO} = 3.3 \text{ V}$	–	–	12	ns
TriseS	Rise time in slow strong mode (90/10%) <sup>[31]</sup>	Clod = 25 pF, $V_{DDIO} = 3.0 \text{ V}$	–	–	75	ns
TfallS	Fall time in slow strong mode (90/10%) <sup>[31]</sup>	Clod = 25 pF, $V_{DDIO} = 3.0 \text{ V}$	–	–	60	ns

**Notes**

30. See Figure 6-9 on page 30 and Figure 6-12 on page 33 for more information on SIO reference.

31. Based on device characterization (Not production tested).

**Table 11-12. SIO AC Specifications (continued)**

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	3.3 V < V <sub>DDIO</sub> < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	33	MHz
	1.71 V < V <sub>DDIO</sub> < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	16	MHz
	3.3 V < V <sub>DDIO</sub> < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	5	MHz
	1.71 V < V <sub>DDIO</sub> < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	4	MHz
	3.3 V < V <sub>DDIO</sub> < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V <sub>DDIO</sub> < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V <sub>DDIO</sub> < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V <sub>DDIO</sub> ≤ 5.5 V	90/10% V <sub>DDIO</sub>	–	–	66	MHz

#### 11.4.3 USBIO

For operation in GPIO mode, the standard range for V<sub>DD</sub> applies, see [Device Level Specifications](#) on page 60.

**Table 11-13. USBIO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to V <sub>ss</sub> , internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to V <sub>ss</sub> , internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	I <sub>OH</sub> = 4 mA, V <sub>DD</sub> ≥ 3 V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I <sub>OL</sub> = 4 mA, V <sub>DD</sub> ≥ 3 V	–	–	0.3	V
Vdi	Differential input sensitivity	[(D+) – (D–)]	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C <sub>IN</sub>	USB transceiver input capacitance	–	–	–	20	pF
I <sub>IL</sub>	Input leakage current (absolute value)	25 °C, V <sub>DD</sub> = 3.0 V	–	–	2	nA



**Table 11-14. USBIO AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\text{ V} \leq V_{\text{DDD}} \leq 5.5\text{ V}$	–	–	20	MHz
		$V_{\text{DDD}} = 1.71\text{ V}$	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% $V_{\text{DDD}}$	$V_{\text{DDD}} > 3\text{ V}$ , 25 pF load	–	–	12	ns
		$V_{\text{DDD}} = 1.71\text{ V}$ , 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% $V_{\text{DDD}}$	$V_{\text{DDD}} > 3\text{ V}$ , 25 pF load	–	–	12	ns
		$V_{\text{DDD}} = 1.71\text{ V}$ , 25 pF load	–	–	40	ns

**Table 11-15. USB Driver AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	$V_{\text{USB}_5}$ , $V_{\text{USB}_3.3}$ , see <a href="#">USB DC Specifications</a> on page 93	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

#### 11.4.4 XRES

**Table 11-16. XRES DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{\text{IH}}$	Input voltage high threshold		$0.7 \times V_{\text{DDIO}}$	–	–	V
$V_{\text{IL}}$	Input voltage low threshold		–	–	$0.3 \times V_{\text{DDIO}}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k $\Omega$
$C_{\text{IN}}$	Input capacitance <sup>[32]</sup>		–	3	–	pF
$V_{\text{H}}$	Input voltage hysteresis (Schmitt-Trigger) <sup>[32]</sup>		–	100	–	mV
Idiode	Current through protection diode to $V_{\text{DDIO}}$ and $V_{\text{SSIO}}$		–	–	100	$\mu\text{A}$

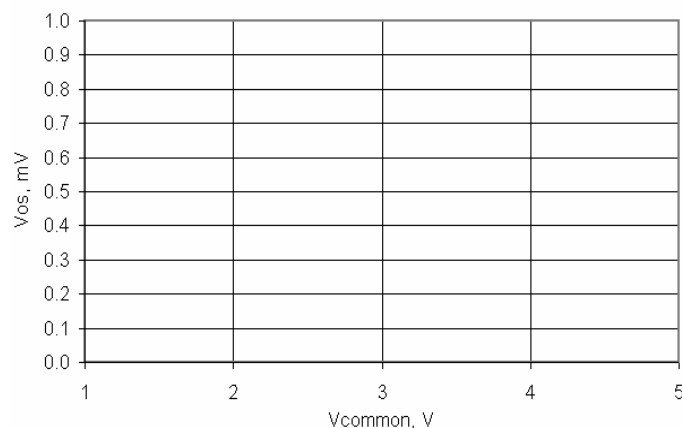
**Table 11-17. XRES AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>RESET</sub>	Reset pulse width		1	–	–	$\mu\text{s}$

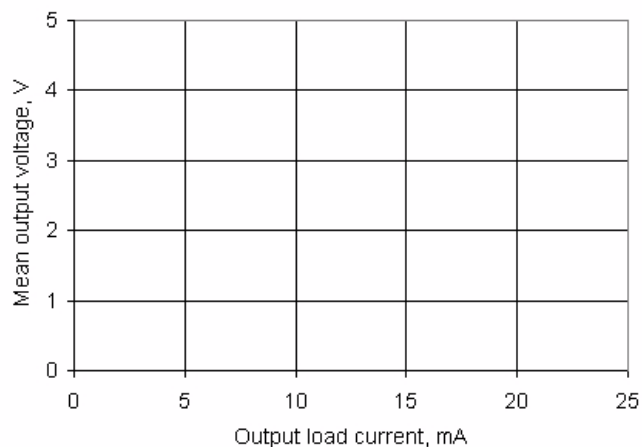
**Note**

32. Based on device characterization (Not production tested).

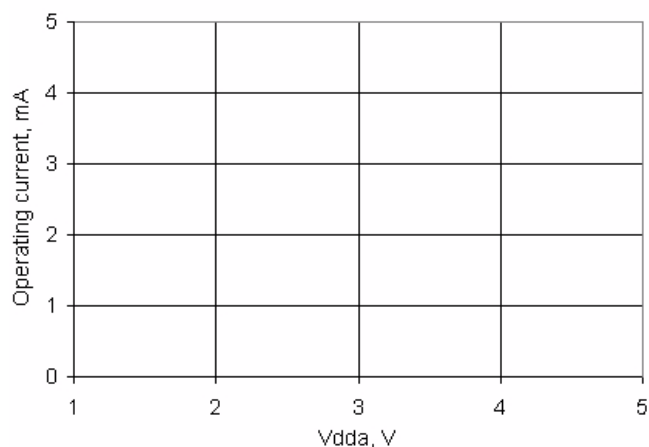
**Figure 11-4. Opamp Voffset vs Common Mode Voltage and Temperature, Power Mode = High**



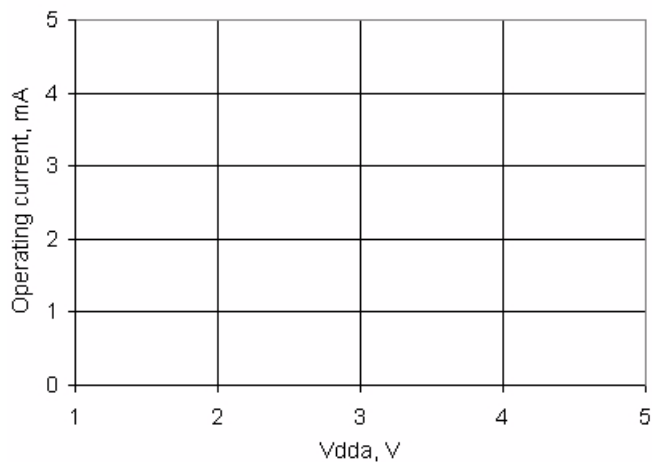
**Figure 11-5. Opamp Output Voltage vs Load Current and Temperature, 25 °C, Vdda = 5V**



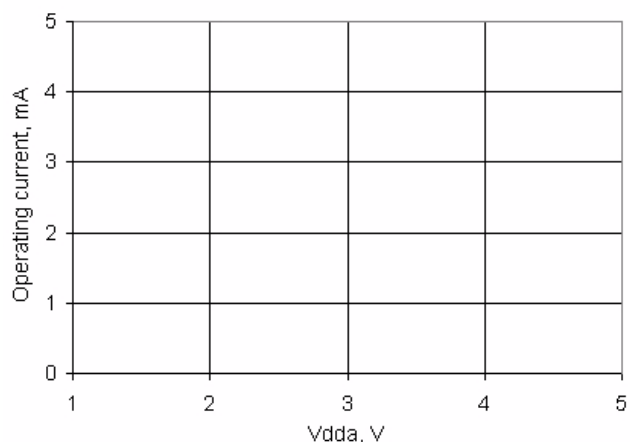
**Figure 11-6. Opamp Operating Current vs Vdda, Power Mode = Minimum**



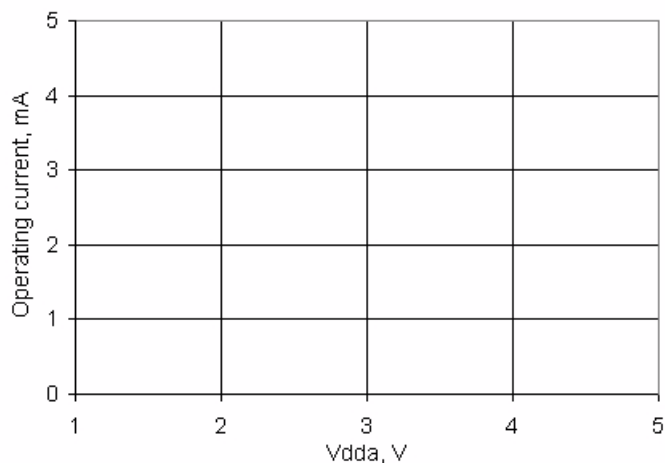
**Figure 11-7. Opamp Operating Current vs Vdda, Power Mode = Low**



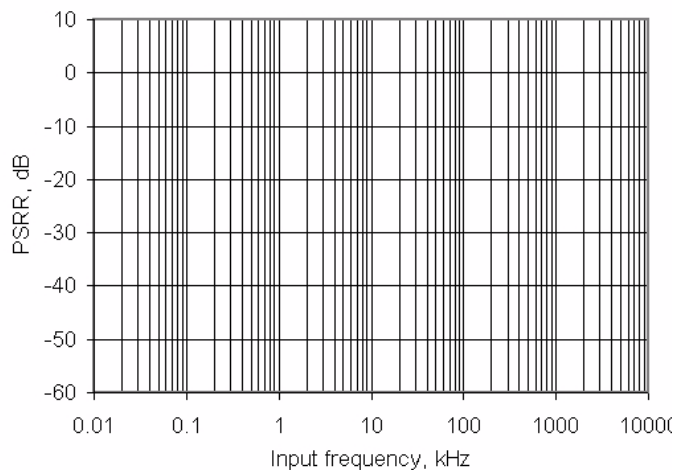
**Figure 11-8. . Opamp Operating Current vs Vdda, Power Mode = Medium**



**Figure 11-9. Opamp Operating Current vs Vdda, Power Mode = High**



**Figure 11-16. Opamp PSRR vs Frequency**



## 11.8 PSoC System Resources

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.8.1 POR with Brown Out

For brown out detect in regulated mode,  $V_{DD}$  and  $V_{DDA}$  must be  $\geq 2.0\text{ V}$ . Brown out detect is not available in externally regulated mode.

**Table 11-67. Precise Power On Reset (PRES) with Brown Out DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
<b>Precise POR (PPOR)</b>						
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

**Table 11-68. Power On Reset (POR) with Brown Out AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	$\mu\text{s}$

### 11.8.2 Voltage Monitors

**Table 11-69. Voltage Monitors DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

**Table 11-70. Voltage Monitors AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time		–	–	1	$\mu\text{s}$



## 11.9 Clocking

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.9.1 32 kHz External Crystal

**Table 11-75. 32 kHz External Crystal DC Specifications<sup>[49]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
I <sub>CC</sub>	Operating current	Low-power mode	–	0.25	1.0	μA
CL	External crystal capacitance		–	6	–	pF
DL	Drive level		–	–	1	μW

**Table 11-76. 32 kHz External Crystal AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T <sub>ON</sub>	Startup time	High power mode	–	1	–	s

### 11.9.2 Internal Main Oscillator

**Table 11-77. IMO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	62.6 MHz		–	–	600	μA
	48 MHz		–	–	500	μA
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	μA
	24 MHz – non USB mode		–	–	300	μA
	12 MHz		–	–	200	μA
	6 MHz		–	–	180	μA
	3 MHz		–	–	150	μA

**Table 11-78. IMO AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO</sub>	IMO frequency stability (with factory trim)					
	62.6 MHz		–7	–	7	%
	48 MHz		–5	–	5	%
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz		–1	–	1	%
	Startup time <sup>[49]</sup>	From enable (during normal system operation) or wakeup from low-power state	–	–	12	μs

**Note**

49. Based on device characterization (Not production tested).

### 11.9.6 Phase-Locked Loop

**Table 11-83. PLL DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
I <sub>DD</sub>	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	μA
		In = 3 MHz, Out = 24 MHz	–	200	–	μA

**Table 11-84. PLL AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
F <sub>plin</sub>	PLL input frequency <sup>[51]</sup>		1	–	48	MHz
	PLL intermediate frequency <sup>[52]</sup>	Output of prescaler	1	–	3	MHz
F <sub>plout</sub>	PLL output frequency <sup>[51]</sup>		24	–	67	MHz
	Lock time at startup		–	–	250	μs
J <sub>period-rms</sub>	Jitter (rms) <sup>[53]</sup>		–	–	250	ps

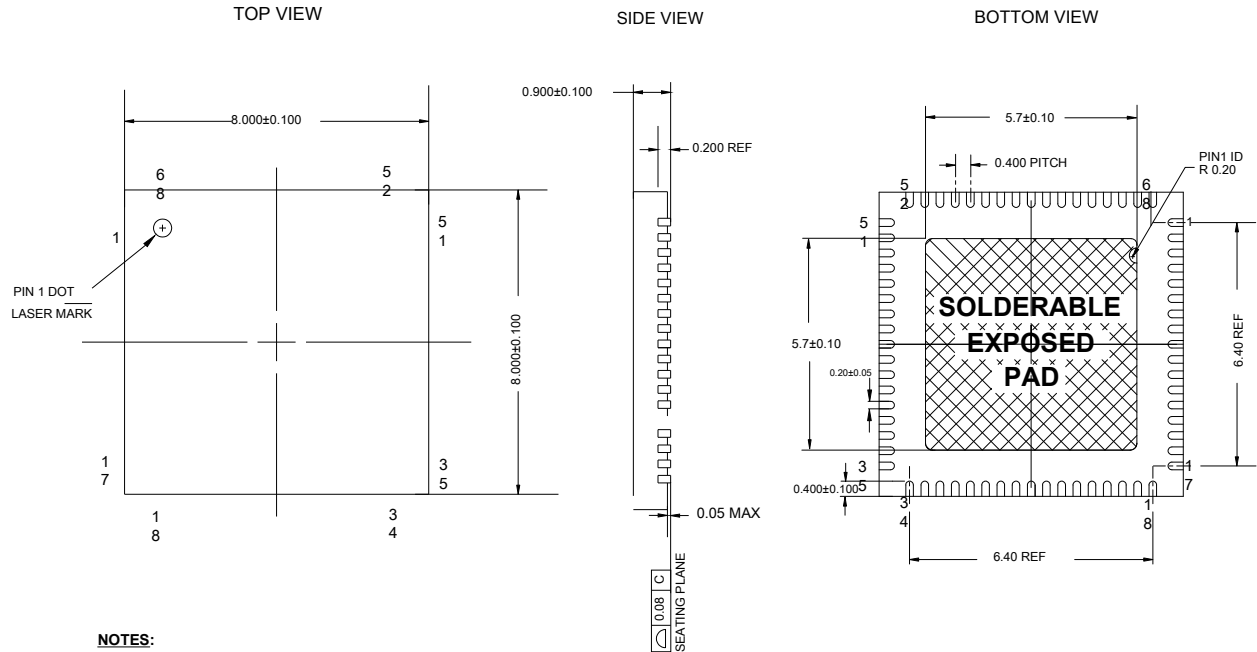
#### Notes

51. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.

52. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

53. Based on device characterization (Not production tested).

Figure 13-3. 68-pin QFN 8×8 with 0.4 mm Pitch Package Outline (Sawn Version)



001-09618 °C

Figure 13-4. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline

