



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3865pvi-063

1. Architectural Overview

Introducing the CY8C38 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C38 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

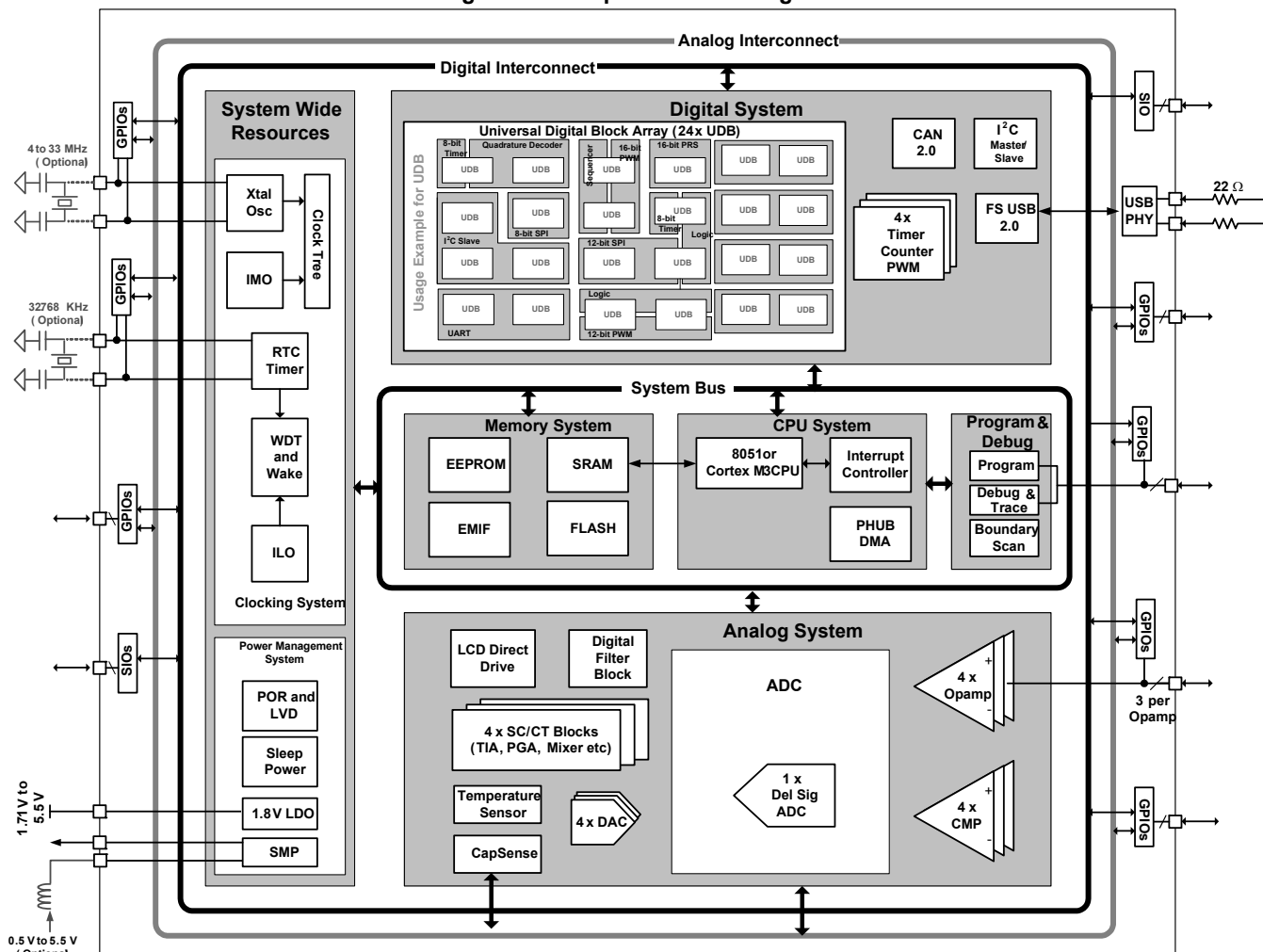


Figure 1-1 illustrates the major components of the CY8C38 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C38 family these blocks can include four 16-bit timers, counters, and PWM blocks; I²C slave, master, and multimaster; FS USB; and Full CAN 2.0b.

It also contains a separate, very low-power internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in real-time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C38 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, or 5.0 V \pm 10%, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5 V. This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the Vboost pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1- μ A sleep mode with RTC. In the second mode, the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

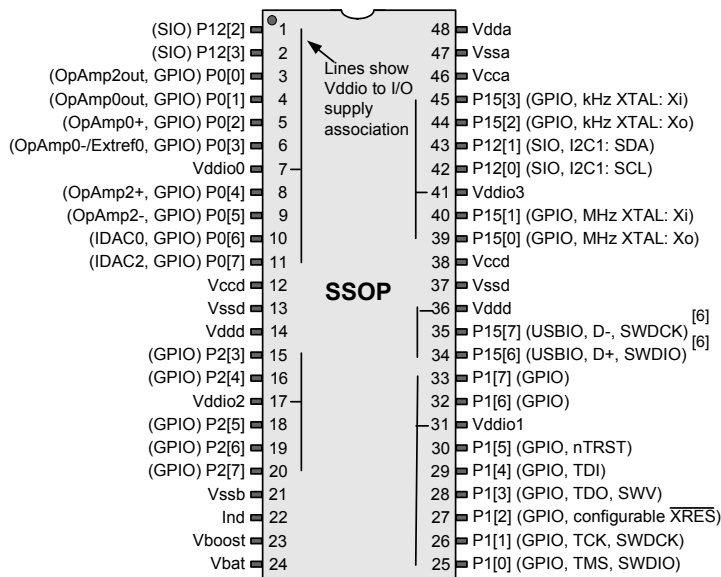
The details of the PSoC power modes are covered in the [“Power System”](#) section on page 24 of this datasheet.

PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for ‘printf’ style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data trace memory for debug. Details of the programming, test, and debugging interfaces are discussed in the [“Programming, Debug Interfaces, Resources”](#) section on page 56 of this datasheet.

2. Pinouts

The Vddio pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in [Figure 2-1](#) through [Figure 2-4](#). Using the Vddio pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each Vddio may sink up to 100 mA total to its associated I/O pins and opamps. On the 68-pin and 100-pin devices each set of Vddio associated pins may sink up to 100 mA. The 48-pin device may sink up to 100 mA total for all Vddio0 plus Vddio2 associated I/O pins and 100 mA total for all Vddio1 plus Vddio3 associated I/O pins.

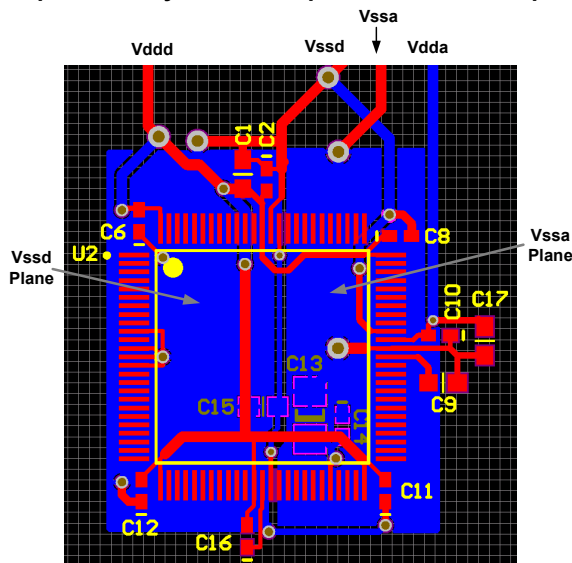
Figure 2-1. 48-pin SSOP Part Pinout



Note

- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3

Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp1out, OpAmp2out, OpAmp3out

High current output of uncommitted opamp^[12].

Extref0, Extref1

External reference input to the analog system.

OpAmp0-, OpAmp1-, OpAmp2-, OpAmp3-

Inverting input to uncommitted opamp.

OpAmp0+, OpAmp1+, OpAmp2+, OpAmp3+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense^[12].

I2C0: SCL, I2C1: SCL

I²C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I²C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I²C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I²C SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 33-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV.

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

Note

12. GPIOs with opamp outputs are not recommended for use with CapSense.

Table 4-2. Logical Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed

addressing mode. [Table 4-3](#) lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. [Table 4-4](#) lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source.

Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I ² C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	Reserved	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]

5. Memory

5.1 Static RAM

CY8C38 SRAM is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See [Memory Map](#) on page 19. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

Flash is read in units of rows; each row is 9 bytes wide with 8 bytes of data and 1 byte of ECC data. When a row is read, the data bytes are copied into an 8-byte instruction buffer. The CPU fetches its instructions from this buffer, for improved CPU performance.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I²C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. [Table 5-1](#) lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a bootloader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the [“Device Security”](#) section on page 57). For more information about how to take full advantage of the security features in PSoC, see the [PSoC 3 TRM](#).

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as ‘unbreakable’. Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

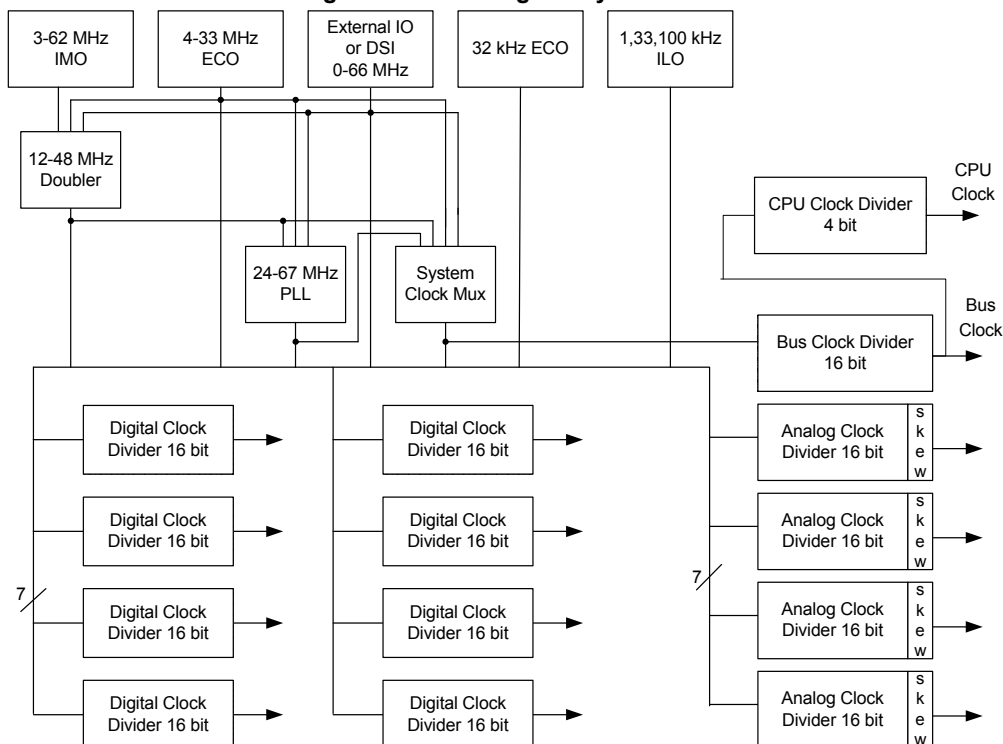
5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C38 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

5.5 External Memory Interface

CY8C38 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. [Figure 5-1](#) is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C38 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See [“xdata Space”](#) section on page 21. The memory can be 8 or 16 bits wide.

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its ± 1 -percent accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ± 1 percent at 3 MHz, up to ± 7 percent at 62 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency (see PLL). The IMO provides clock outputs at 3, 6, 12, 24, 48, and 62 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works for input frequency ranges of 6 to 24 MHz (providing 12 to 48 MHz at the output). It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 PLL

The PLL allows low-frequency, high-accuracy clocks to be multiplied to higher frequencies. This is a trade off between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 μ s (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low-power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low-power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz. The 1-kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low-power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1-kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled, except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low-power mode. Firmware can reset the central timewheel. Systems that require accurate timing should use the RTC capability instead of the central timewheel.

The 100-kHz clock (CLK100K) works as a low-power system clock to run the CPU. It can also generate time intervals such as fast sleep intervals using the fast timewheel. The fast timewheel is a 100-kHz, 5-bit counter clocked by the ILO that can also be used to wake the system. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic wakeups of the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached.

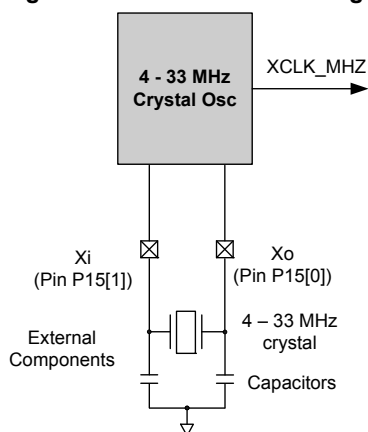
The 33-kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768-kHz ECO clock with no need for a crystal.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 33 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see PLL). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

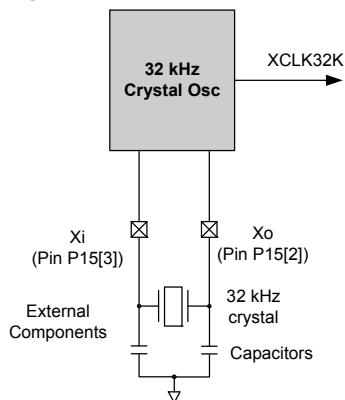


6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. The converter can be configured to provide low-power, low-current regulation in the standby mode. The external 32-kHz crystal can be used to generate inductor boost pulses on the rising and falling edge of the clock when the output voltage is less than the programmed value. This is called automatic thump mode (ATM).

The boost typically draws 200 μ A in active mode and 12 μ A in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize the total chip power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

Table 6-4. Chip and Boost Power Modes Compatibility

Chip Power Modes	Boost Power Modes
Chip – Active mode	Boost can be operated in either active or standby mode.
Chip – Sleep mode	Boost can be operated in either active or standby mode. However, it is recommended to operate boost in standby mode for low-power consumption
Chip – Hibernate mode	Boost can only be operated in active mode. However, it is recommended not to use boost in chip hibernate mode due to high current consumption in boost active mode

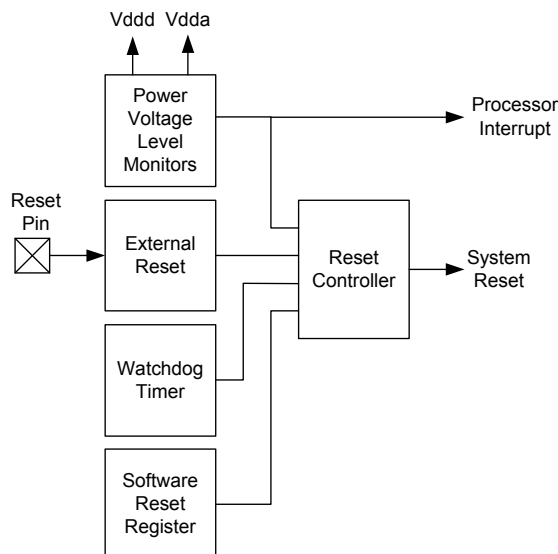
If the boost converter is not used in a given application, tie the Vbat, Vssb, and Vboost pins to ground and leave the Ind pin unconnected.

6.3 Reset

CY8C38 has multiple internal and external reset sources available. The reset sources are:

- **Power source monitoring** – The analog and digital power voltages, Vdda, Vddd, Vcca, and Vccd are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- **External** – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to Vddio1. Vddd, Vdda, and Vddio1 must all have voltage applied before the part comes out of reset.
- **Watchdog timer** – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- **Software** – The device can be reset under program control.

Figure 6-7. Resets



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register holds the source of the most recent reset or power voltage monitoring interrupt. The program may examine this register to detect and report exception conditions. This register is cleared after a power-on reset.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

■ IPOR – Initial power-on reset

At initial power on, IPOR monitors the power voltages V_{DDP} and V_{DDA}, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

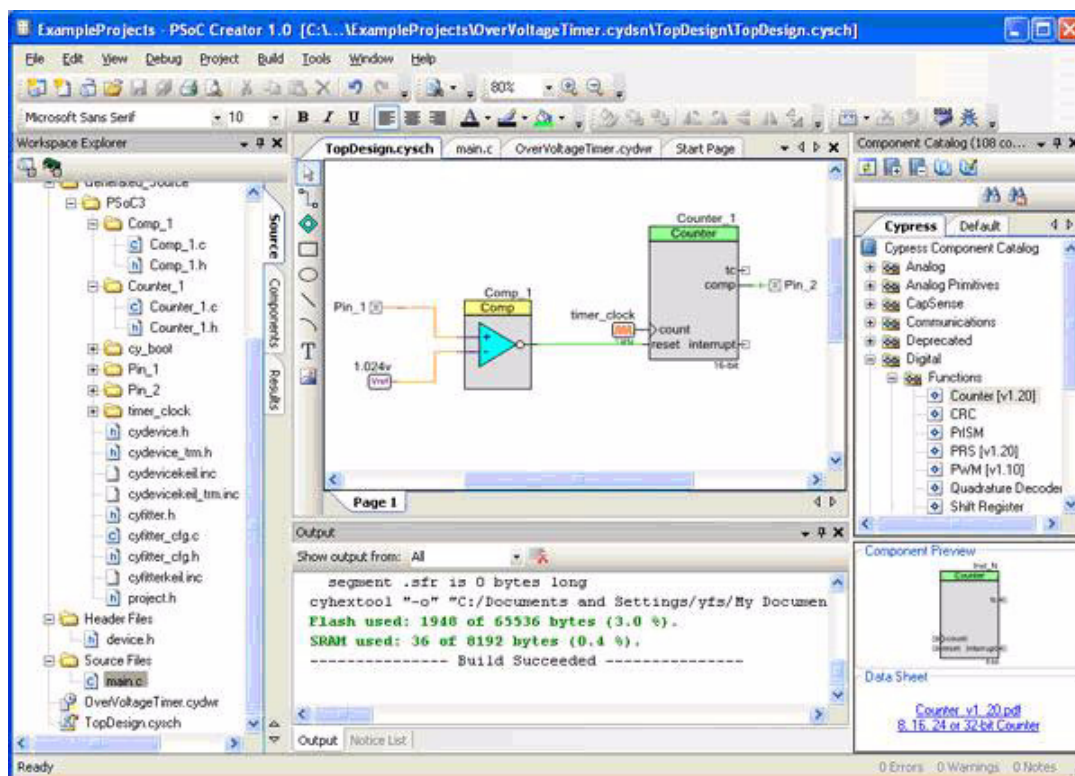
To save power the IPOR circuit is disabled when the internal digital supply is stable. Voltage supervision is then handed off to the precise low voltage reset (PRES) circuit. When the voltage is high enough for PRES to release, the IMO starts.

■ PRES – Precise low voltage reset

This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

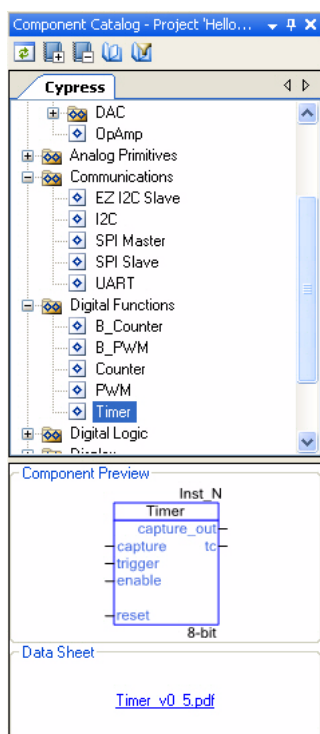
In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I²C, USB, and CAN. See [Example Peripherals](#) on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

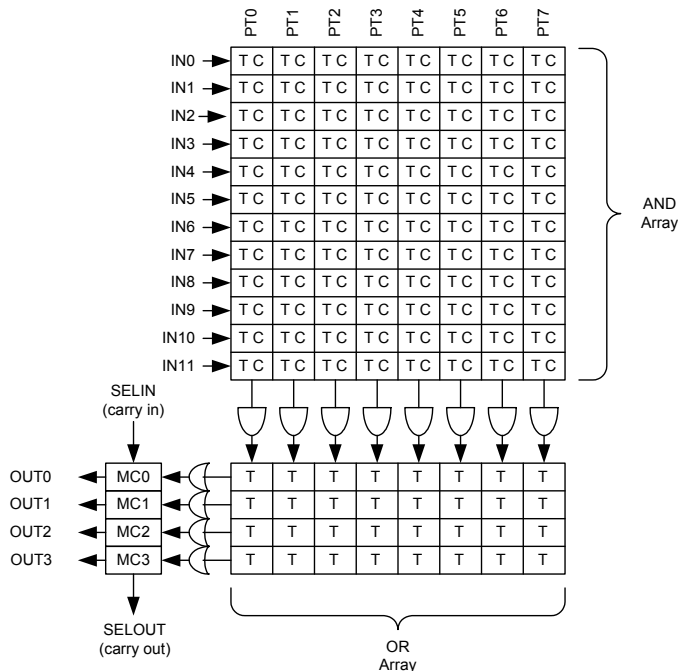
The main component blocks of the UDB are:

- **PLD blocks** – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- **Datapath module** – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- **Status and control module** – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- **Clock and reset module** – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-7. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-7. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

Figure 11-6. Opamp Operating Current vs Vdda, Power Mode = Minimum

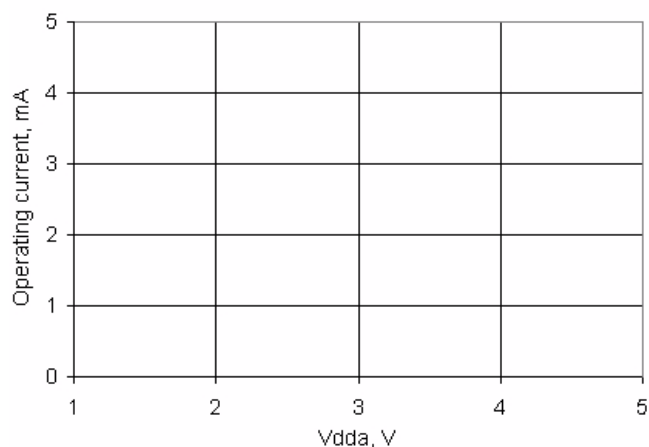


Figure 11-7. Opamp Operating Current vs Vdda, Power Mode = Low

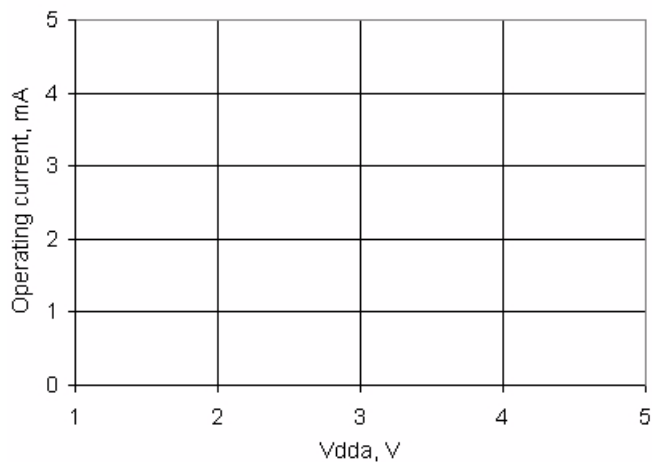


Figure 11-8. . Opamp Operating Current vs Vdda, Power Mode = Medium

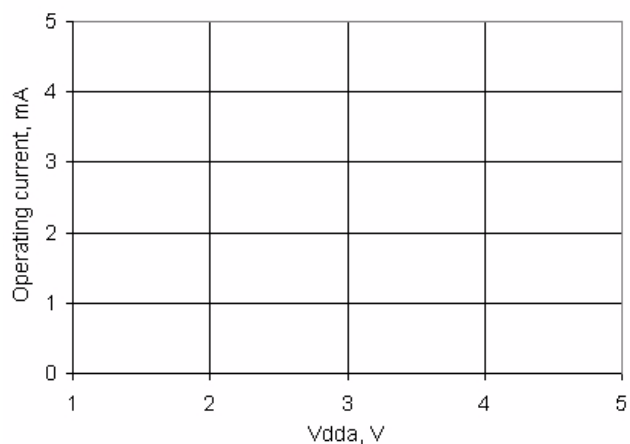


Figure 11-9. Opamp Operating Current vs Vdda, Power Mode = High

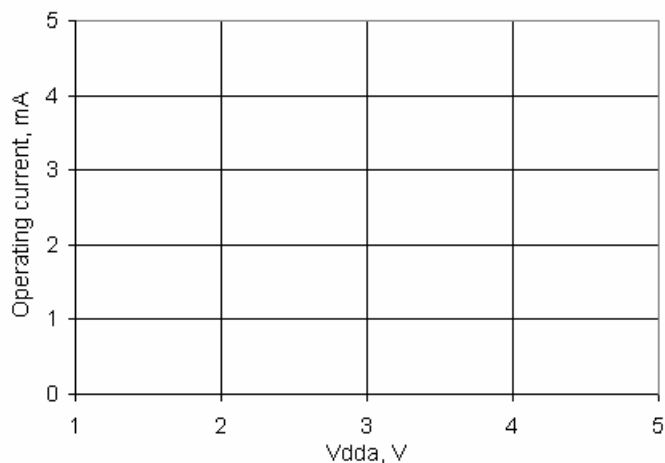


Table 11-22. Delta-sigma ADC Sample Rates, Range = ± 1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-17. Delta-sigma ADC I_{DD} vs sps, Range = ± 1.024 V

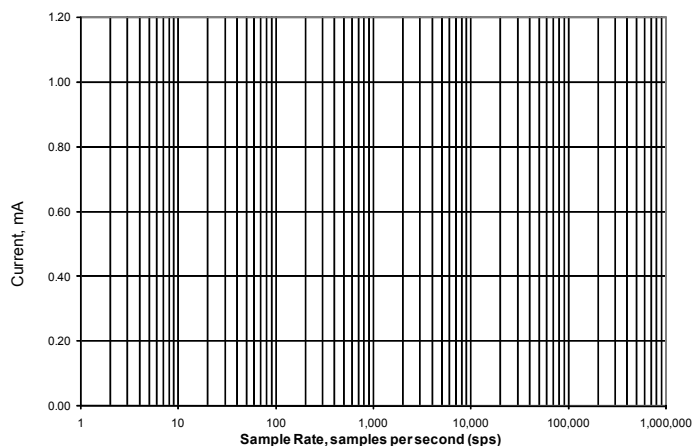


Figure 11-18. Delta-sigma ADC INL at Maximum Sample Rate

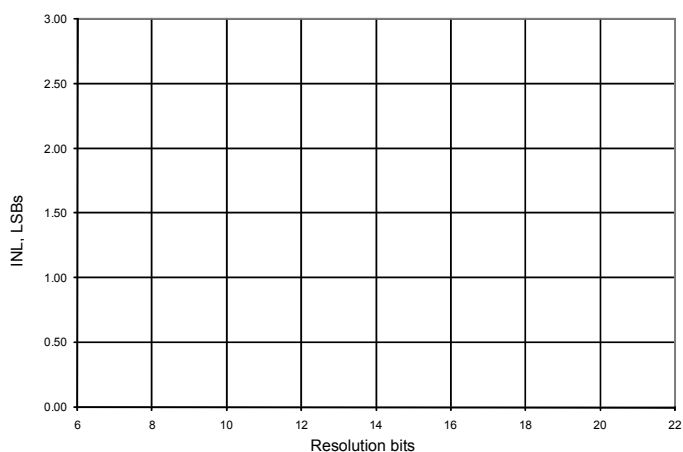


Figure 11-39. VDAC Full Scale Error vs Temperature, 1 V Mode

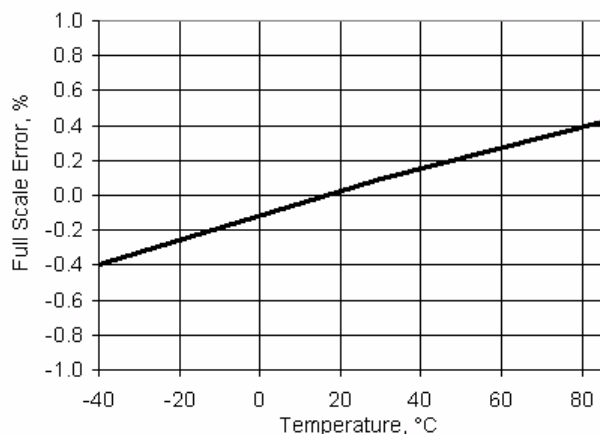


Figure 11-40. VDAC Full Scale Error vs Temperature, 4 V Mode

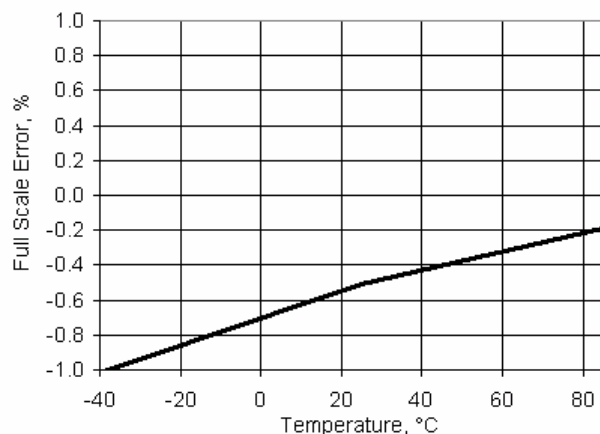


Figure 11-41. VDAC Operating Current vs Temperature, 1V Mode, Slow Mode

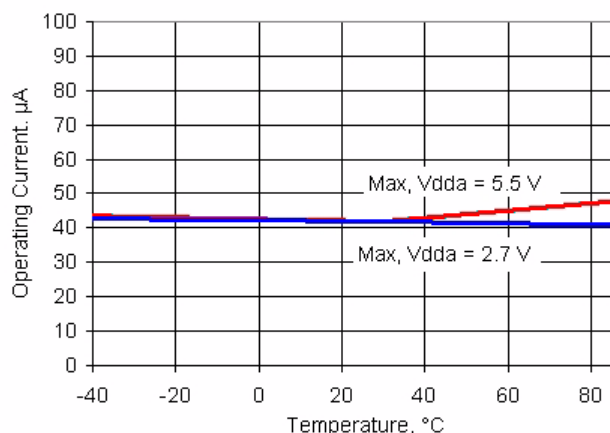


Figure 11-42. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode

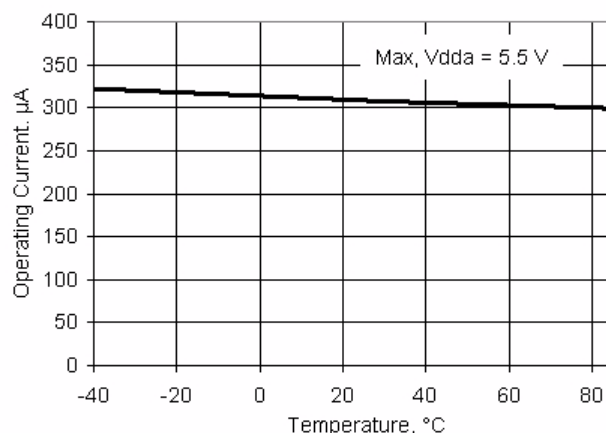


Table 11-32. VDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
T _{settleP}	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	3.2	µs
T _{settleN}	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	3	µs

11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component datasheet in PSoC Creator for full electrical specifications and APIs.

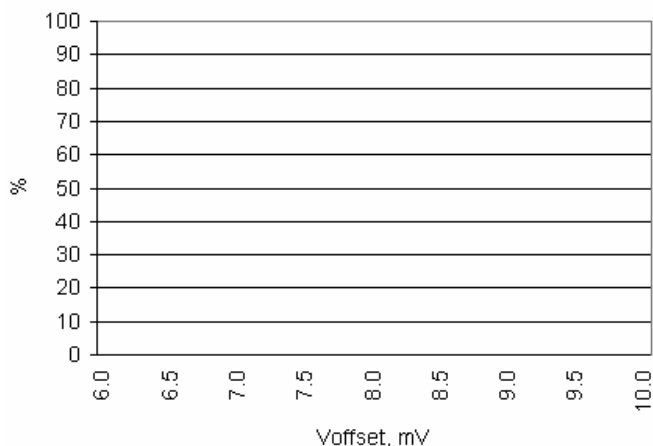
Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-37. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{in}	Input voltage range	Power mode = minimum	V _{ssa}	–	V _{dda}	V
V _{os}	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
TCV _{os}	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge ₁	Gain error, gain = 1		–	–	±0.15	%
Ge ₁₆	Gain error, gain = 16		–	–	±2.5	%
Ge ₅₀	Gain error, gain = 50		–	–	±5	%
V _{onl}	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
C _{in}	Input capacitance		–	–	7	pF
V _{oh}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	V _{DDA} – 0.15	–	–	V
V _{ol}	Output voltage swing	Power mode = high, gain = 1, R _{load} = 100 kΩ to V _{DDA} / 2	–	–	V _{SSA} + 0.15	V
V _{src}	Output voltage under load	I _{load} = 250 µA, V _{dda} ≥ 2.7V, power mode = high	–	–	300	mV
I _{dd}	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Figure 11-43. V_{offset} Histogram, 1000 Samples, V_{dda} = 5 V



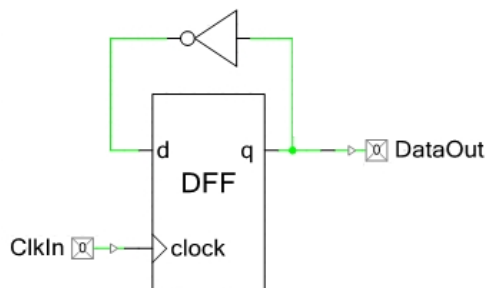
11.6.8 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-54. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F _{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67	MHz
F _{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67	MHz
F _{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67	MHz
PLD Performance						
F _{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67	MHz
Clock to Output Performance						
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-47.	25 °C, V _{ddd} ≥ 2.7 V	–	20	25	ns
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-47.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-47. Clock to Output Performance



11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{SRAM}	SRAM operating frequency		DC	–	67	MHz

11.7.5 External Memory Interface

Figure 11-48. Asynchronous Read Cycle Timing

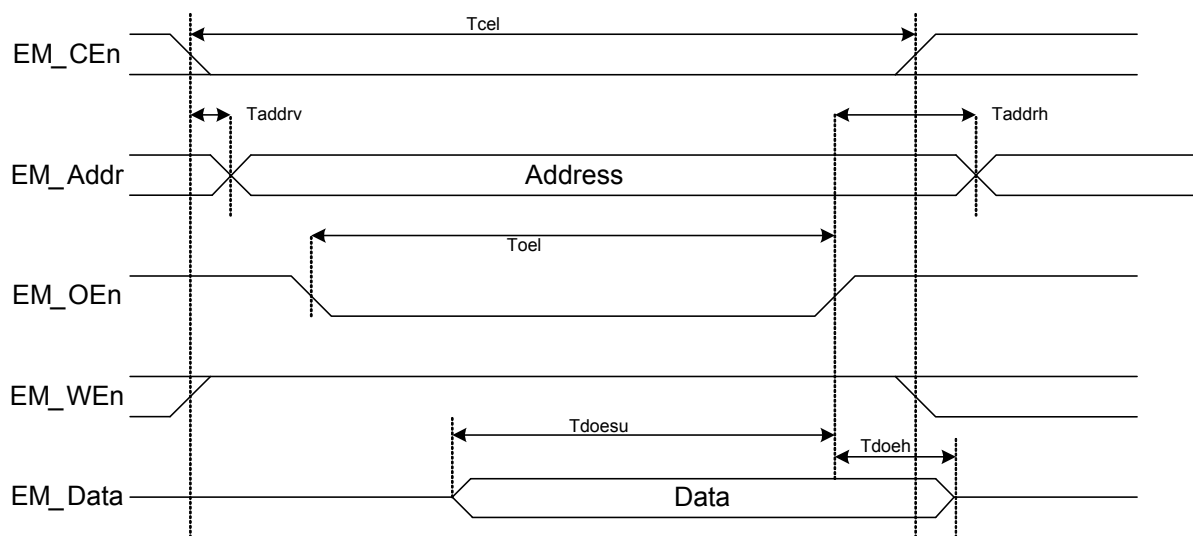


Figure 11-51. Synchronous Write Cycle Timing

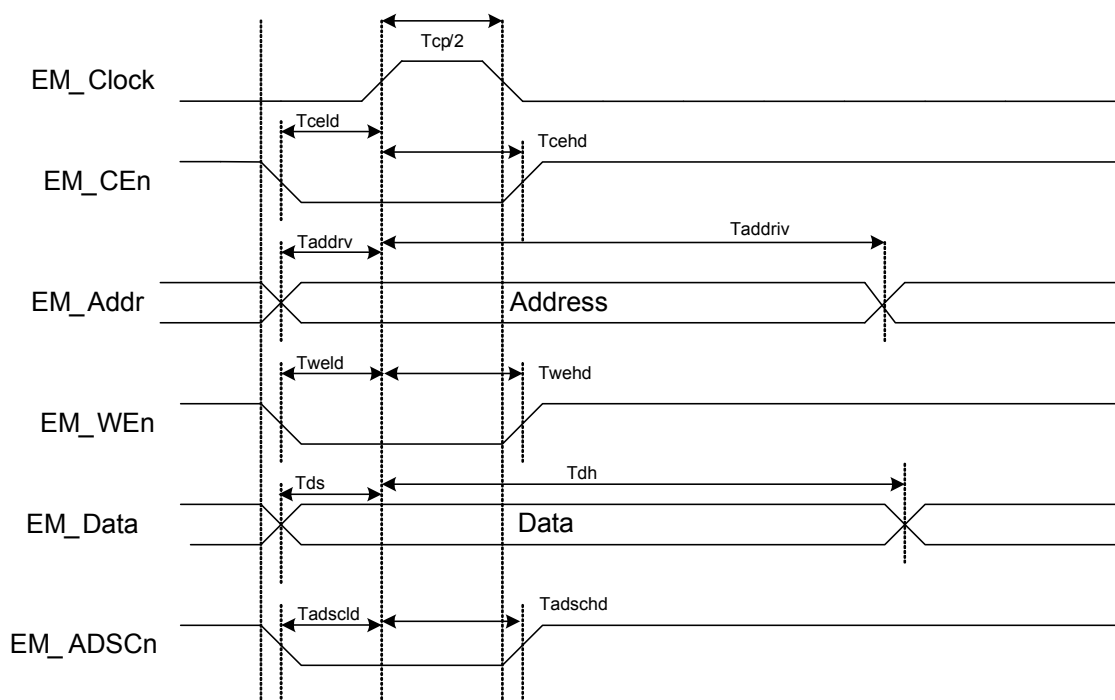


Table 11-66. Synchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock Period ^[45]	V _{dda} ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Tweld	EM_WEn low to EM_Clock high		5	–	–	nS
Twehd	EM_Clock high to EM_WEn high		T/2 – 5	–	–	nS
Tds	Data valid before EM_Clock high		5	–	–	nS
Tdh	Data invalid after EM_Clock high		T	–	–	nS
Tadscl	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note

45. Limited by GPIO output frequency, see [Table 11-10](#) on page 65.

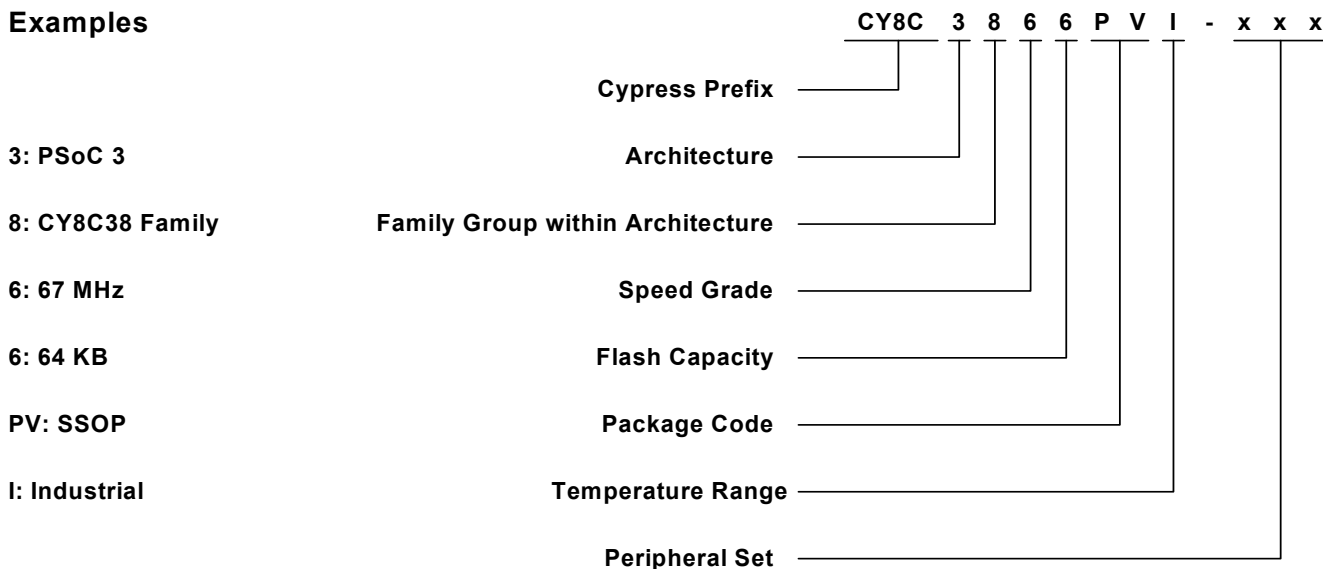
12.1 Part Numbering Conventions

PSoc 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
 - 3: PSoC 3
 - 5: PSoC 5
- b: Family group within architecture
 - 4: CY8C34 family
 - 6: CY8C36 family
 - 8: CY8C38 family
- c: Speed grade
 - 4: 48 MHz
 - 6: 67 MHz
- d: Flash capacity
 - 4: 16 KB
 - 5: 32 KB
 - 6: 64 KB
- ef: Package code
 - Two character alphanumeric
 - AX: TQFP
 - LT: QFN
 - PV: SSOP
- g: Temperature range
 - C: commercial
 - I: industrial
 - A: automotive
- xxx: Peripheral set
 - Three character numeric
 - No meaning is associated with these three characters.

Examples



All devices in the PSoC 3 CY8C38 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high-level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®)
Document Number: 001-11729

*K	2903576	04/01/2010	MKEA	<p>Updated Vb pin in PCB Schematic.</p> <p>Updated Tstartup parameter in AC Specifications table.</p> <p>Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table.</p> <p>Updated I_{CC} parameter in LCD Direct Drive DC Specs table.</p> <p>In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz.</p> <p>Updated I_{OUT} parameter in LCD Direct Drive DC Specs table.</p> <p>Updated Table 6-2 and Table 6-3.</p> <p>Added bullets on CapSense in page 1; added CapSense column in Section 12.</p> <p>Removed some references to footnote [1].</p> <p>Changed INC_Rn cycles from 3 to 2 (Table 4-1).</p> <p>Added footnote in PLL AC Specification table.</p> <p>Added PLL intermediate frequency row with footnote in PLL AC Specs table.</p> <p>Added UDBs subsection under 11.6 Digital Peripherals.</p> <p>Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9.</p> <p>Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1.</p> <p>Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DD} pins.</p> <p>Updated boost converter section (6.2.2).</p> <p>Updated Tstartup values in Table 11-3.</p> <p>Removed IPOR rows from Table 11-68.</p> <p>Updated 6.3.1.1, Power Voltage Level Monitors.</p> <p>Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash.</p> <p>Updated V_{REF} specs in Table 11-21.</p> <p>Updated IDAC uncompensated gain error in Table 11-25.</p> <p>Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 11-72. Removed other line in table.</p> <p>Added sentence to last paragraph of section 6.1.1.3.</p> <p>Updated T_{RESP}, high and low-power modes, in Table 11-24.</p> <p>Updated f_{TCK} values in Table 11-73 and f_{SWDCK} values in Table 11-74.</p> <p>Updated SNR condition in Table 11-20.</p> <p>Corrected unit of measurement in Table 11-21.</p> <p>Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3.</p> <p>Added 1.71 V ≤ V_{DD} < 3.3 V, SWD over USBIO pins value to Table 11-74.</p> <p>Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1.</p> <p>Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR).</p> <p>Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1.</p> <p>Changed I_{DD} values on page 1, page 5, and Table 11-2.</p> <p>Changed resume time value in Section 6.2.1.3.</p> <p>Changed ESD HBM value in Table 11-1.</p> <p>Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20.</p> <p>Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22.</p> <p>Changed V_{IOFF} values and changed CMRR value in Table 11-23.</p> <p>Changed INL max value in Table 11-27.</p> <p>Added max value to the Quiescent current specs in Tables 11-29 and 11-31.</p> <p>Changed occurrences of "Block" to "Row" and deleted the "ECC not included" footnote in Table 11-57.</p> <p>Changed max response time value in Tables 11-69 and 11-71.</p> <p>Changed the Startup time in Table 11-79.</p> <p>Added condition to intermediate frequency row in Table 11-85.</p> <p>Added row to Table 11-69.</p> <p>Added brown out note to Section 11.8.1.</p>
----	---------	------------	------	--